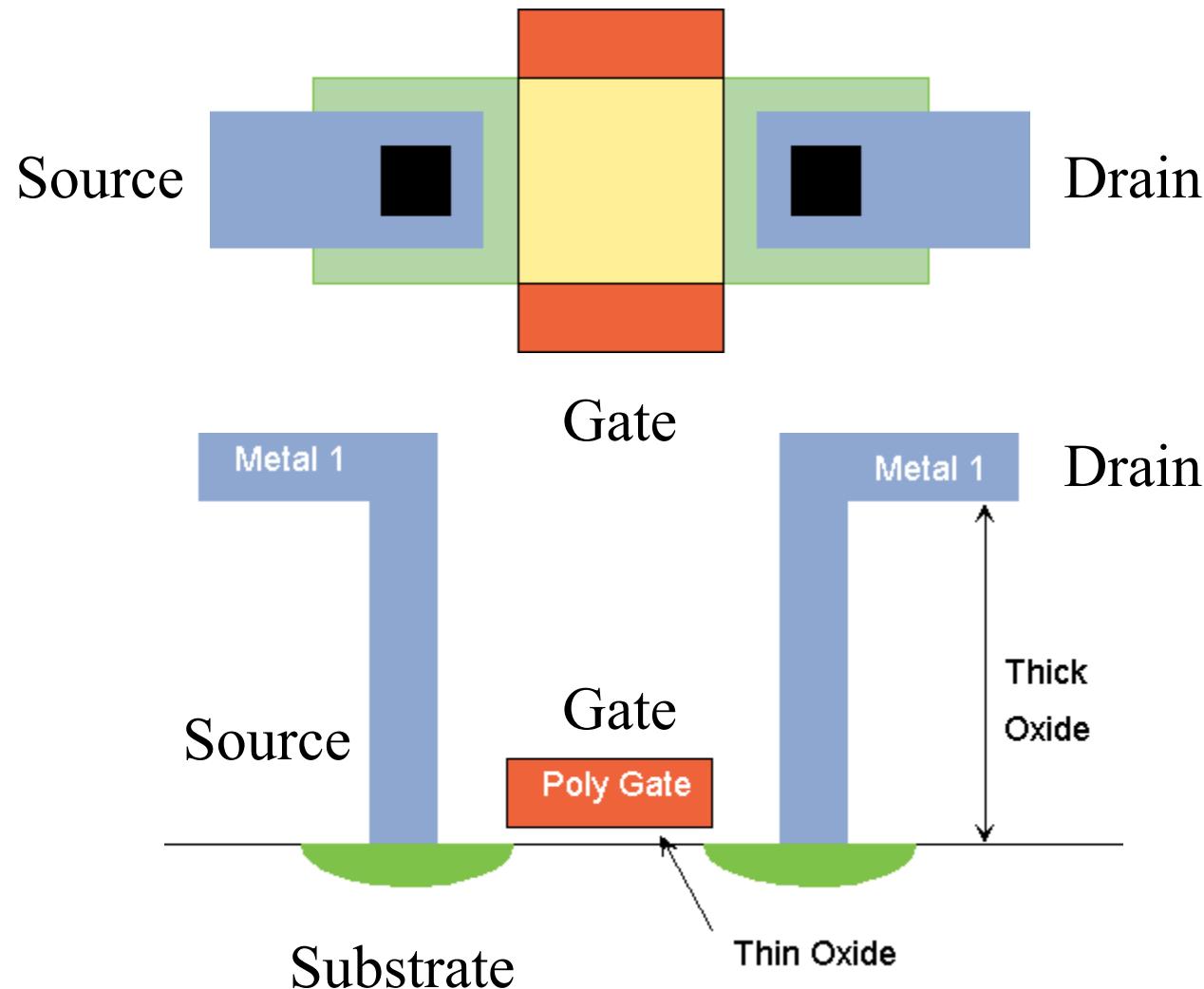


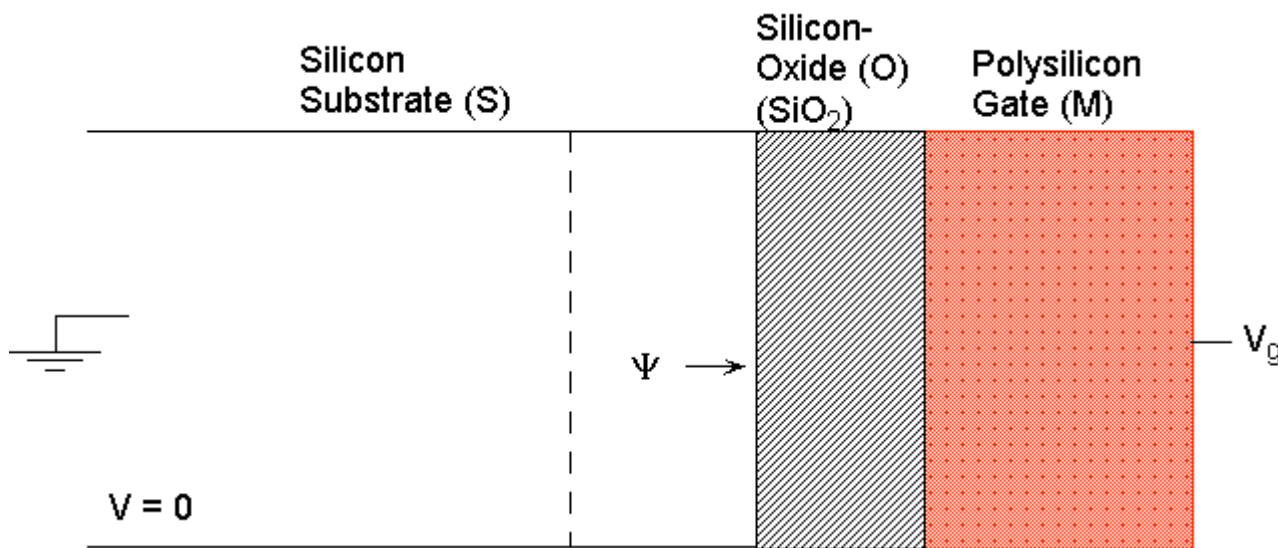
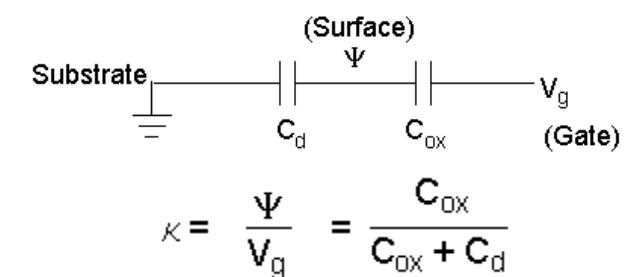
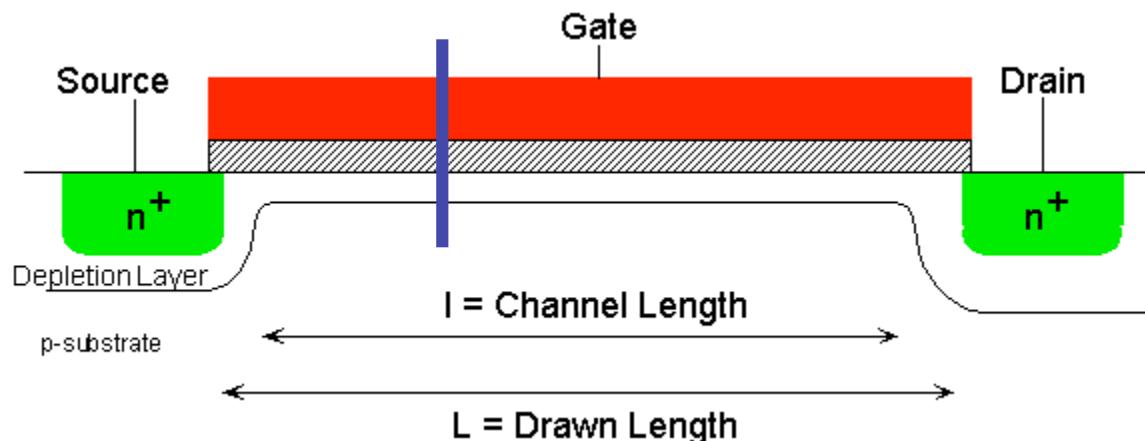
MOSFET Overview

Paul Hasler

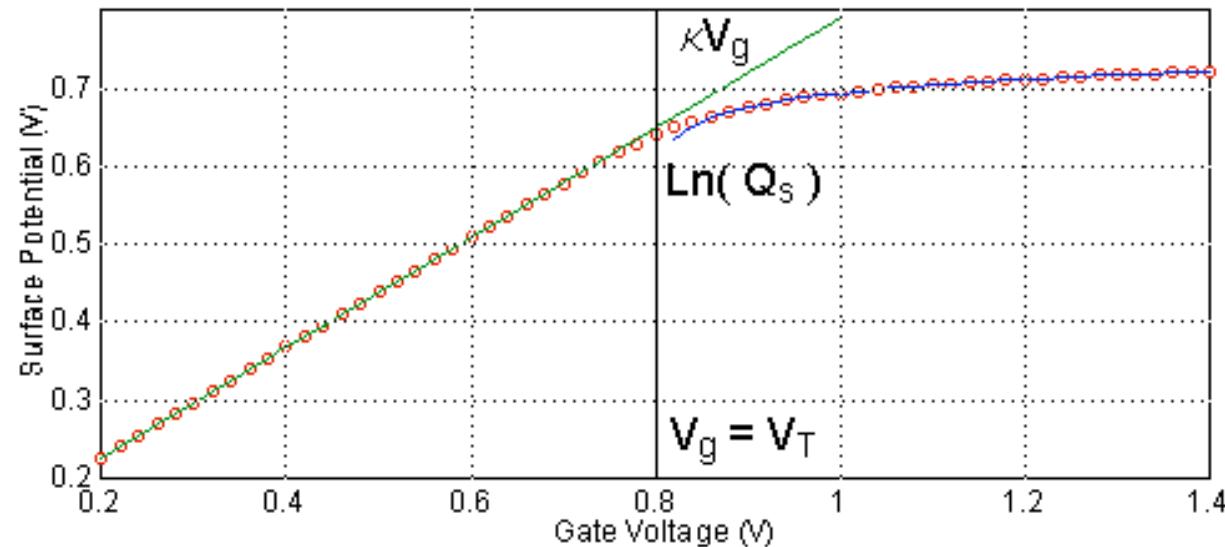
A MOSFET Transistor



MOS Capacitor Picture



MOS-Capacitor Regions



Surface potential moving from depletion to inversion

$$Q_s = e^{(\Psi - V_s)/U_T}$$

$$Q_s = \ln(1 + e^{(\kappa(V_g - V_T) - V_s)/U_T})$$

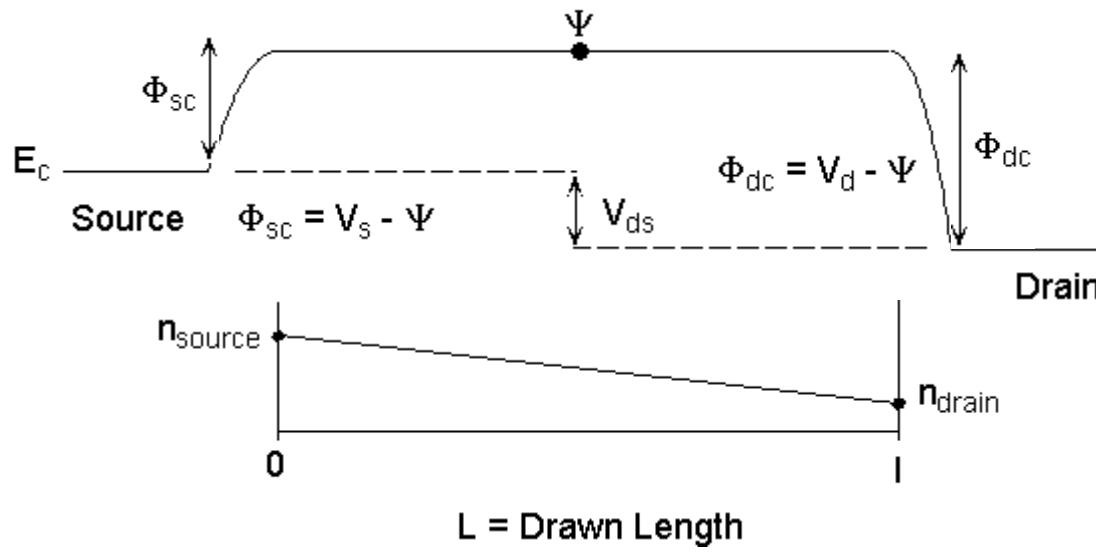
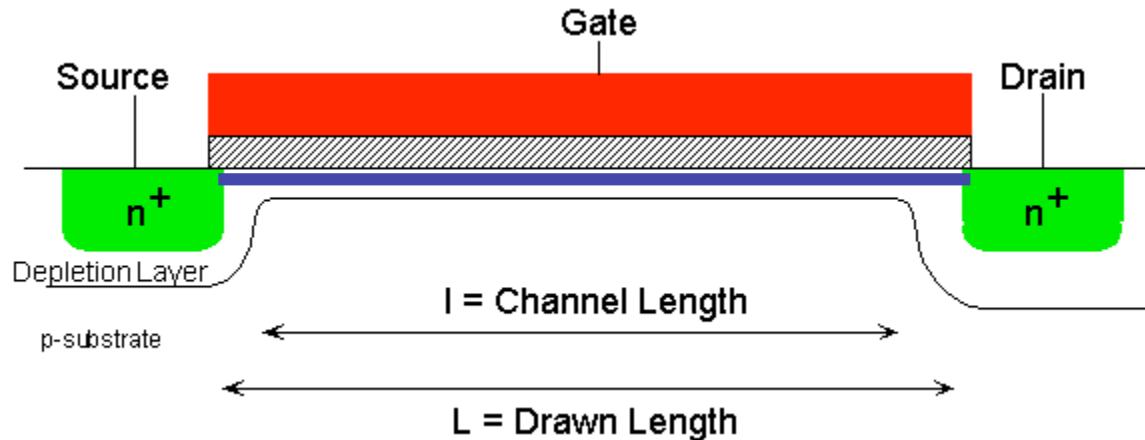
Depletion ($\kappa(V_g - V_T) - V_s \leq 0$)

$$Q_s = e^{(\kappa(V_g - V_T) - V_s)/U_T}$$

Inversion ($\kappa(V_g - V_T) - V_s \geq 0$)

$$Q_s = (\kappa(V_g - V_T) - V_s)/U_T$$

MOSFET Channel Picture

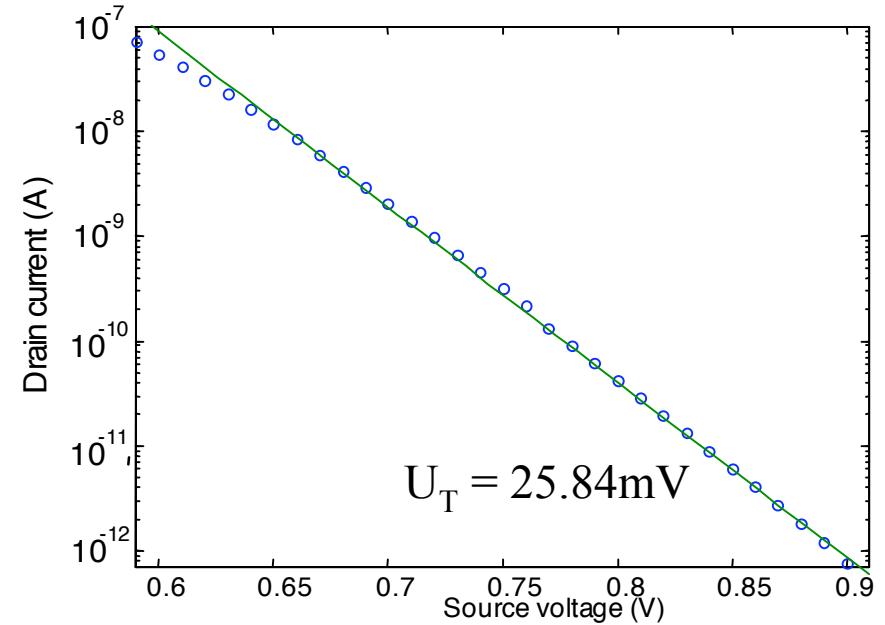
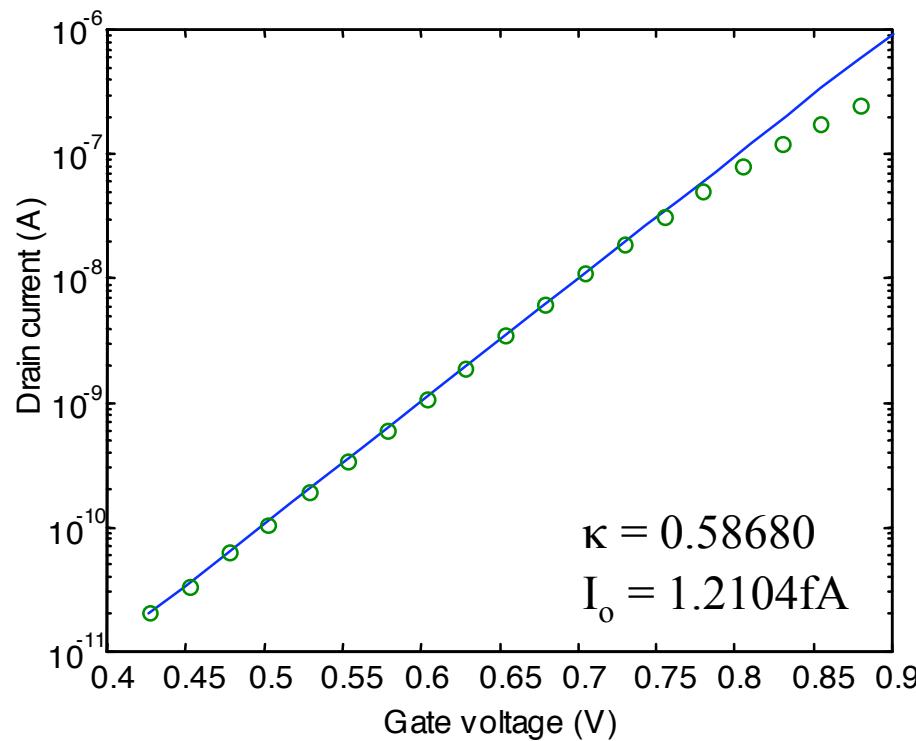


Channel Current is constant

$$\text{Diffusion: } J_n = q D_n \frac{dn}{dx} = q D_n \frac{n_{source} - n_{drain}}{l}$$

$$I = I_0 \left(e^{\kappa V_g - V_s / U_T} - e^{\kappa V_g - V_d / U_T} \right)$$

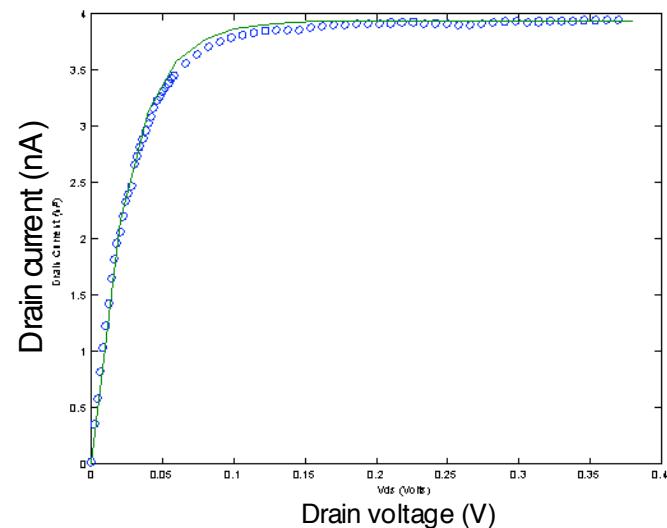
Subthreshold MOSFET Curves



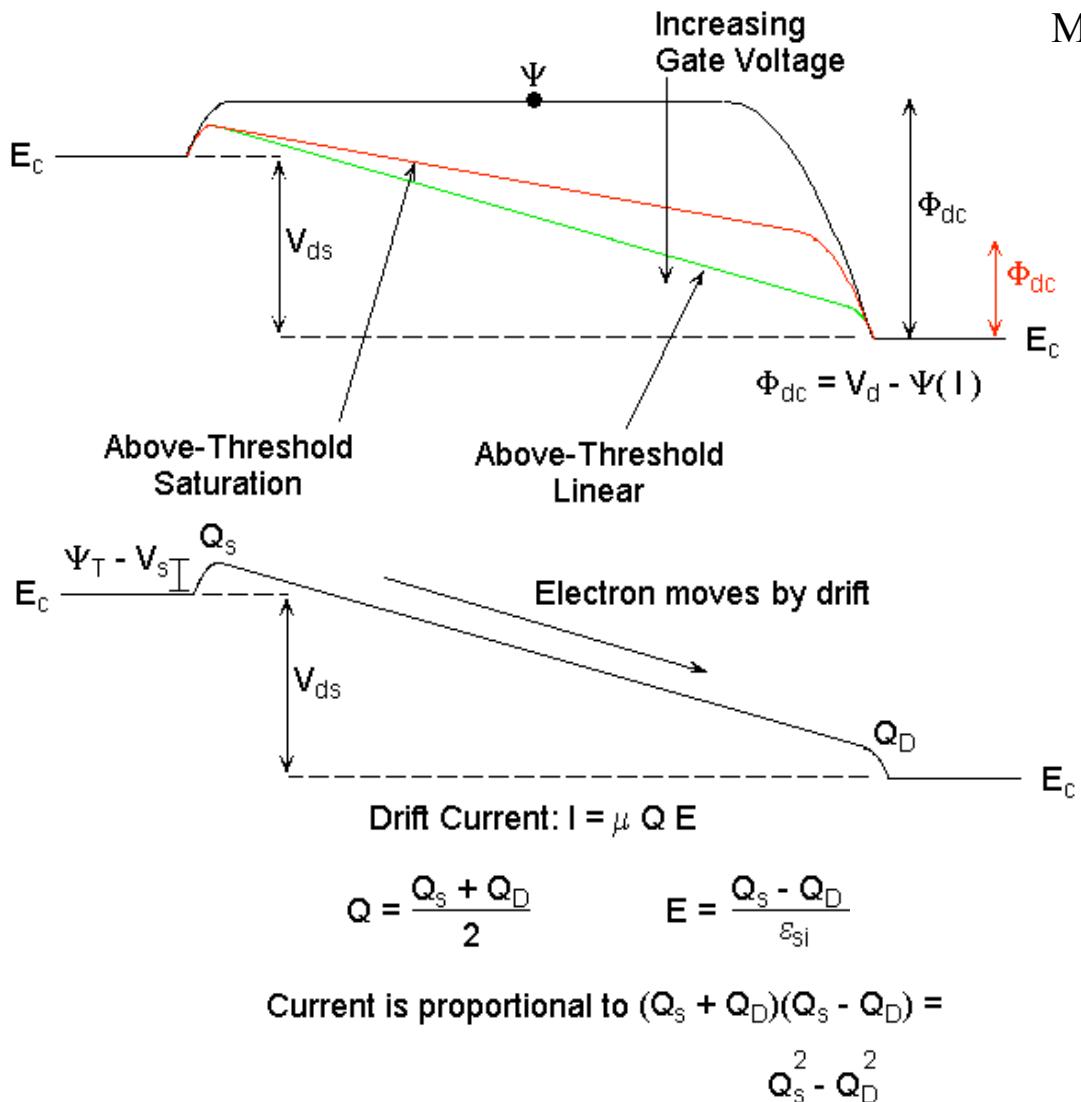
$$I_{ds} = I_0 e^{\kappa V_g / U_T} (e^{-V_s / U_T} - e^{-V_d / U_T})$$

$$= I_0 e^{(\kappa V_g - V_s) / U_T} \quad (V_{ds} > 4 U_T)$$

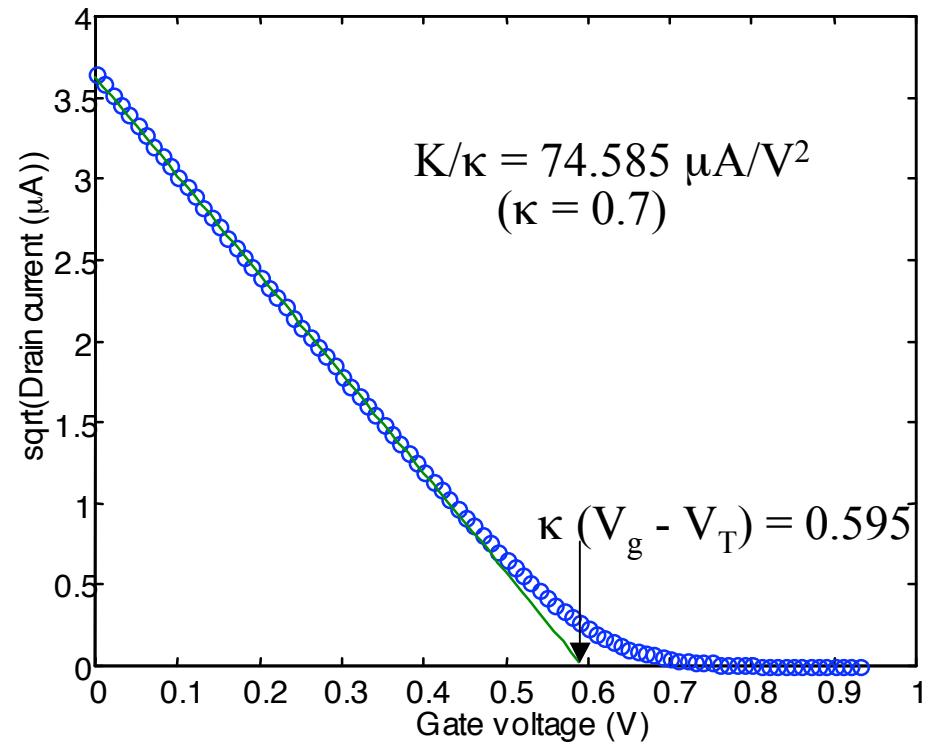
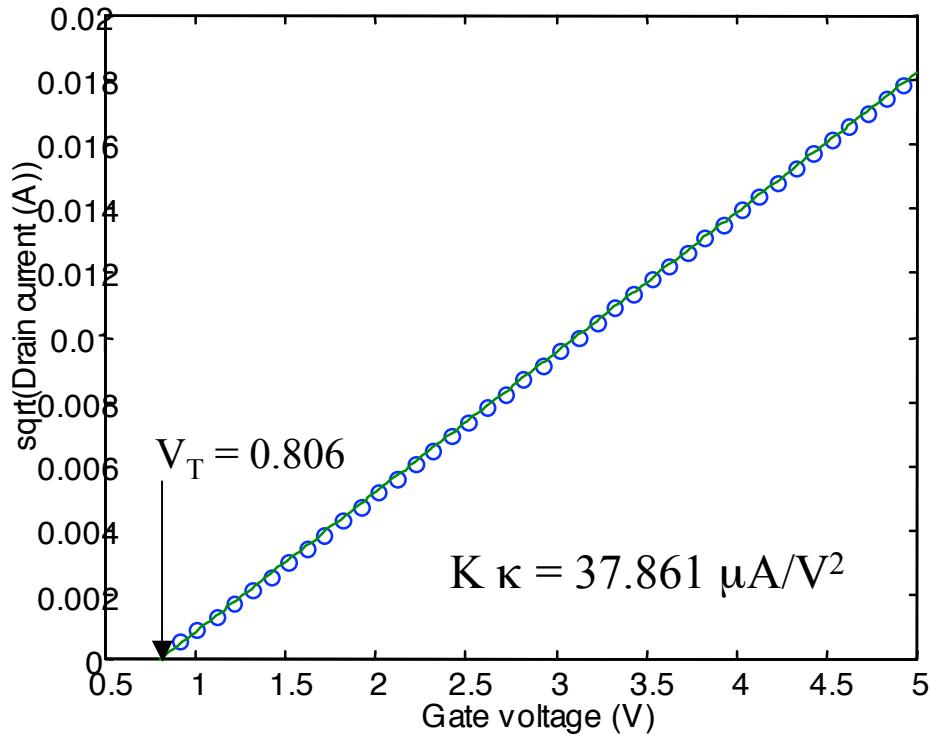
"Saturation"



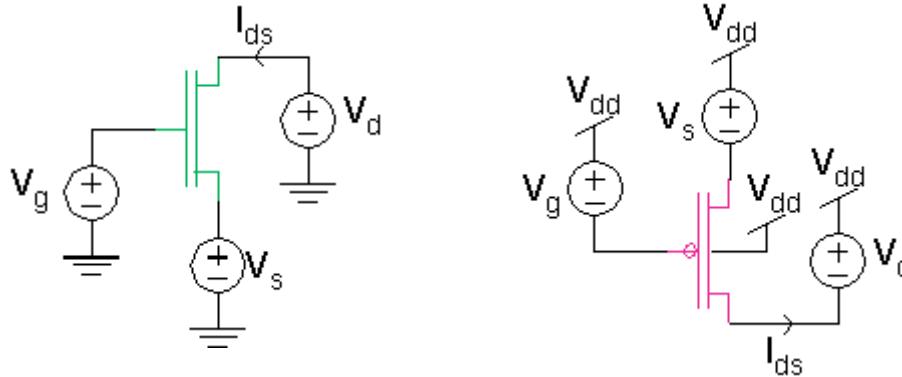
Above-Threshold MOSFET



Drain Current - Gate/Source Voltage



MOSFET Equations



$$I = \left(\frac{K}{2\kappa} \right) \left((\kappa(V_g - V_T) - V_s)^2 - (\kappa(V_g - V_T) - V_d)^2 \right)$$

Above-Threshold:

$$\text{Saturation: } (Q_d = 0) \quad I = \left(\frac{K}{2} \right) (\kappa(V_g - V_T) - V_s)^2$$

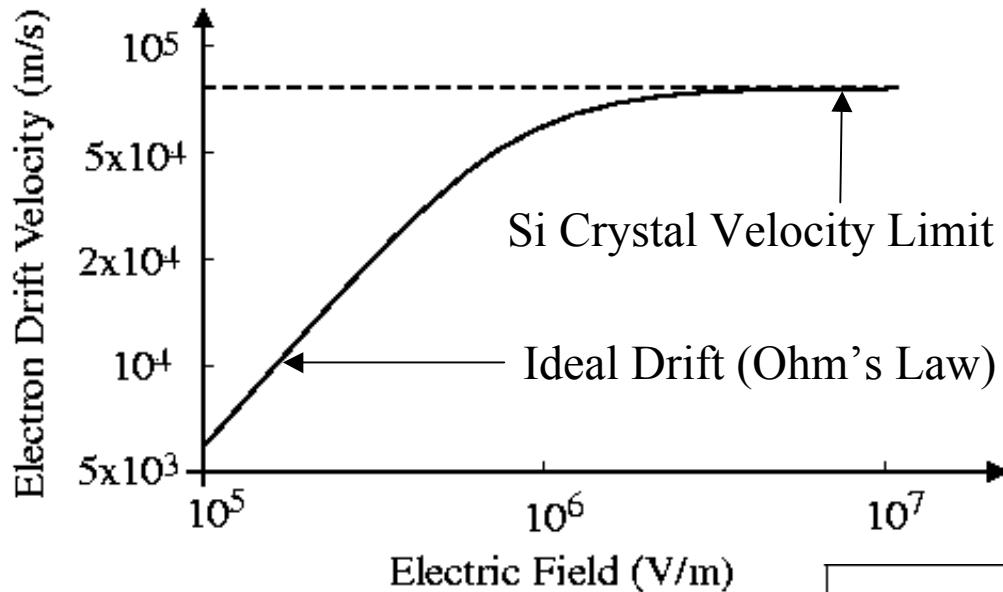
$$V_d > \kappa(V_g - V_T)$$

$$I = I_s e^{\kappa V_g - V_s / U_T} (1 - e^{-V_{ds} / U_T})$$

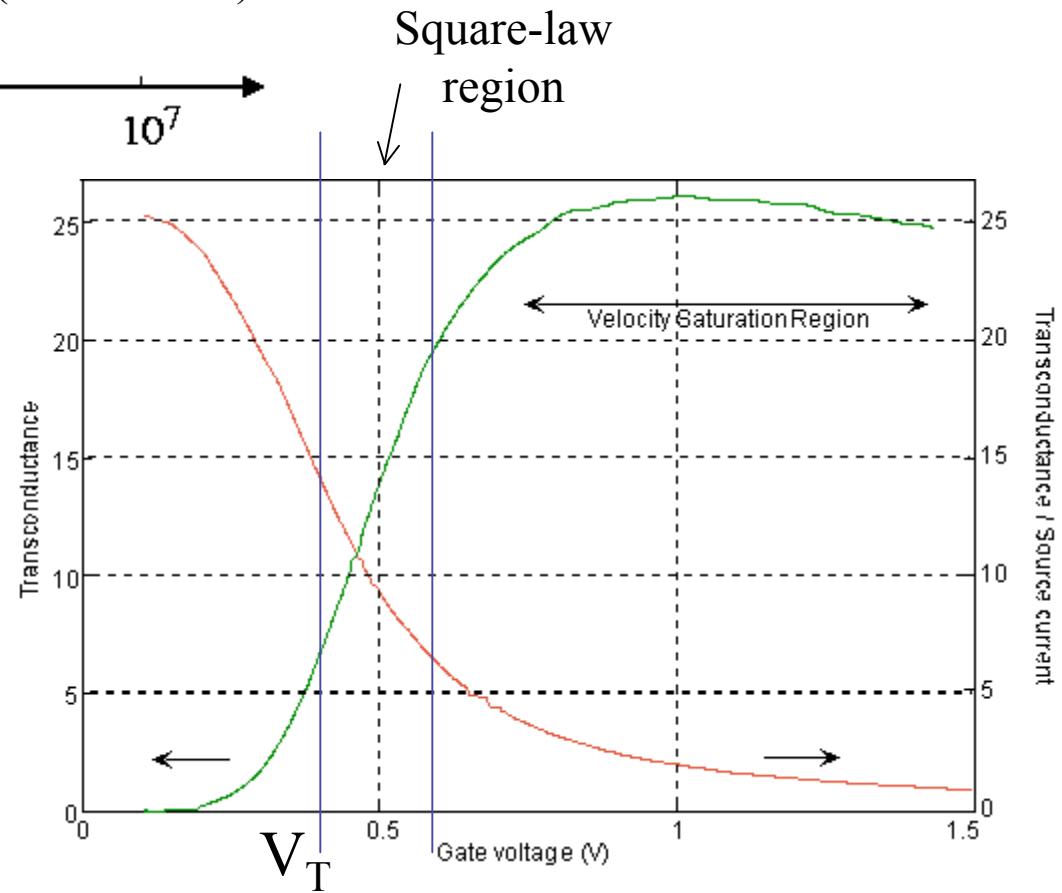
Subthreshold:

$$\text{Saturation: } (V_{ds} > 4 U_T) \quad I = I_s e^{\kappa V_g - V_s / U_T}$$

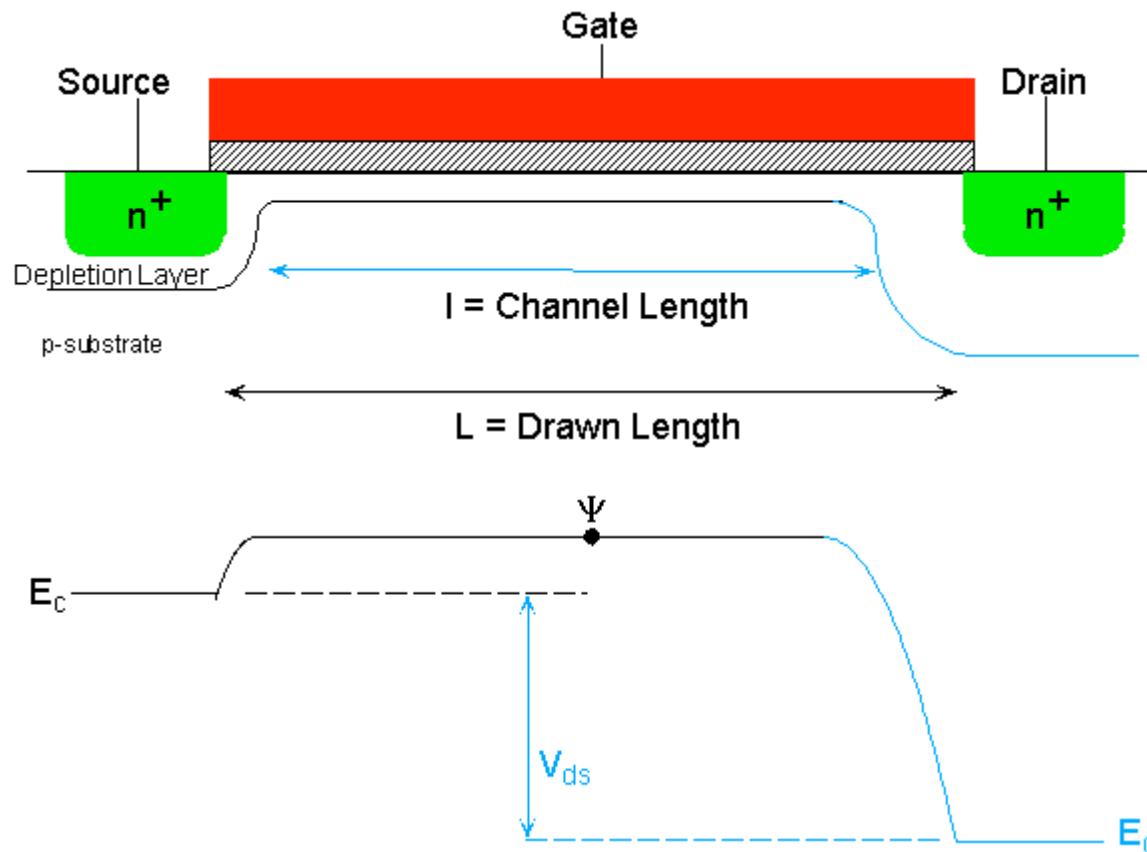
Velocity Saturation



$L = 76$ nm MOSFET



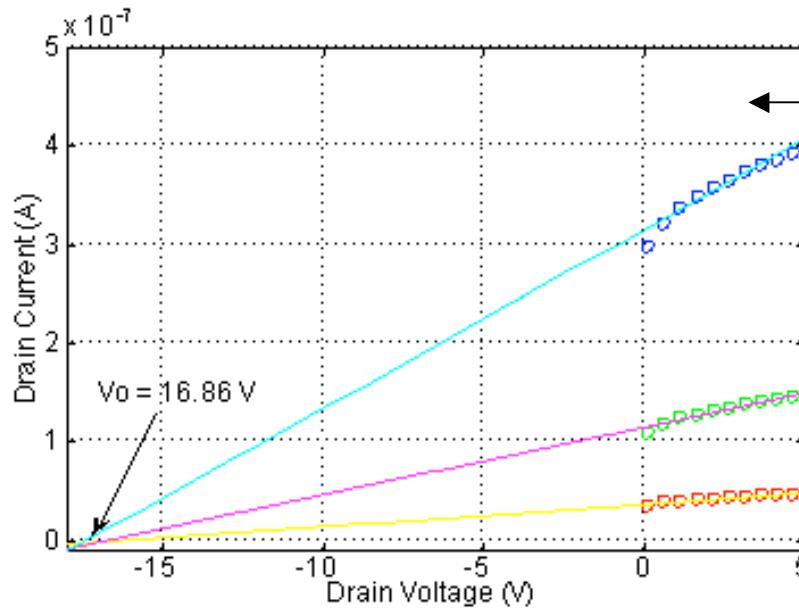
Origin of Drain Dependencies



Increasing V_d effects the drain-to-channel region:

- increases barrier height
- increases depletion width

Current versus Drain Voltage



Why is this not flat?

Effect is called the Early effect

(no, it does not come before something else)

First considered in BJT devices

Limits the gain of a Transistor

$$I_d = I_{d(\text{sat})} (1 + (V_d/V_o))$$

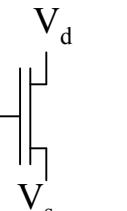
$$\begin{aligned} I_{ds} &= I_0 e^{kV_g/U_T} (e^{-V_s/U_T} - e^{-V_d/U_T}) \\ &= I_0 e^{(kV_g - V_s)/U_T} \quad (V_{ds} > 4 U_T) \\ &\quad \text{"Saturation"} \end{aligned}$$

$$I_d = I_{d(\text{sat})} e^{V_d/V_o}$$

DC-Removed Modeling

Needed for nonlinear analysis; do not want to carry biasing details through the analysis

Formulating the Approach

 Assume bias conditions, some set, some set by the circuit:
 V_{g0} , V_{d0} , V_{s0}
Resulting in a bias current = I_{bias}

We expand

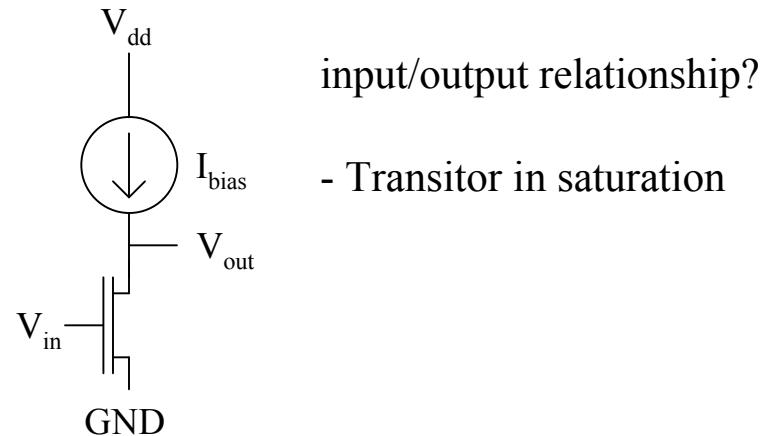
$$\begin{aligned}V_g &= V_{g0} + \Delta V_g, \quad V_d = V_{d0} + \Delta V_d, \\V_s &= V_{s0} + \Delta V_s\end{aligned}$$

For for MOSFET in saturation, we get

$$\begin{aligned}I &= I_0 \exp\left(\frac{\kappa(V_g - V_s)}{U_T}\right) \exp\left(\frac{V_d}{V_A}\right) \\&= I_{bias} \exp\left(\frac{\kappa(\Delta V_g - \Delta V_s)}{U_T}\right) \exp\left(\frac{\Delta V_d}{V_A}\right)\end{aligned}$$

$$I_{bias} = I_0 \exp\left(\frac{\kappa(V_{g0} - V_{s0})}{U_T}\right) \exp\left(\frac{V_{d0}}{V_A}\right)$$

Solving for Transistor Gain



$$I_{bias} = I_{bias} \exp\left(\frac{\kappa \Delta V_{in}}{U_T}\right) \exp\left(\frac{\Delta V_{out}}{V_A}\right)$$

$$\text{Gain} = \frac{\Delta V_{out}}{\Delta V_{in}} = -\frac{\kappa V_A}{U_T}$$

Key parameters of EKV model

$$K' \longrightarrow K_p$$

$$\kappa \longrightarrow \frac{\gamma}{2\phi_f} \quad \gamma = 1 / (2\kappa \sqrt{2\phi_f})$$

$$V_{T0} \longrightarrow V_{T0} \quad (\text{not voltage dependant})$$

$$V_A \longrightarrow \begin{matrix} DL \\ \lambda \end{matrix}$$

and some short-channel parameters