Analog Circuit Testing

- Test Problems
- Basic Components / Parameters
- Test Methods
  - DSP Based
  - Design for Test
  - Built-in Self-Test
  - Algorithmic Method

Test Problems

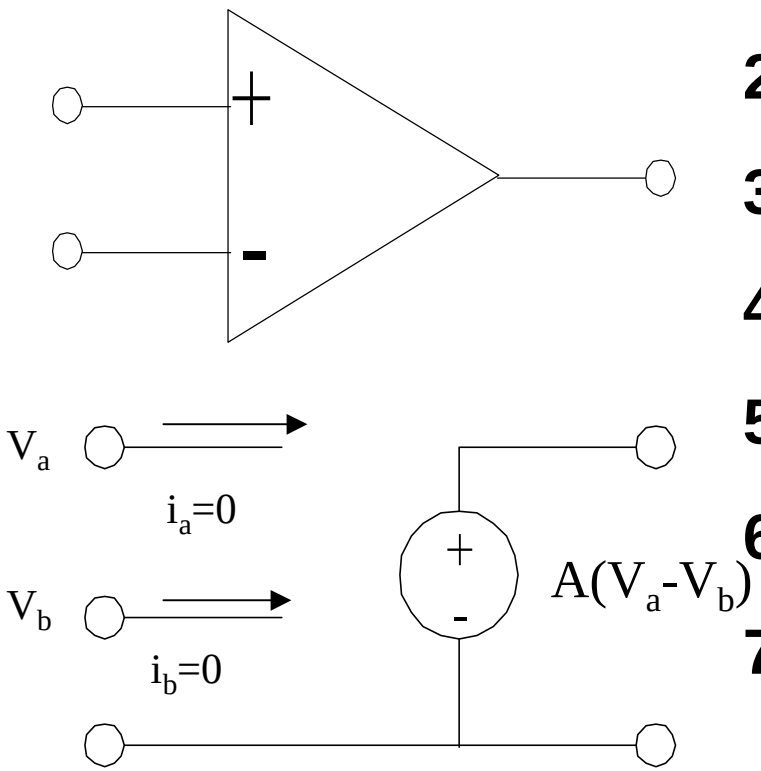
- Continuous signals in analog circuits
- Fault models
- Device parameters
- Test time
- Test effectiveness (fault coverage)
- Test cost

Typical Analog Components

- Operational amplifiers
- Integrators
- DAC & ADC
- Phase lock loops
- Filters

Operational Amplifiers

Ideal op-amp



Property

1. voltage-controlled voltage source
2. infinite voltage gain
3. infinite input impedance
4. zero output impedance
5. infinite bandwidth
6. no offset voltage
7. infinite CMRR

Property of real op-amp

1. finite gain(practical op-amps $A \cong 10^{2\sim} 10^{4}$)
2. finite linear range($V_{DD} > V_o > GND$)
3. offset voltage
   - input offset voltage V_{offset} is defined as the differential input voltage needed to restore $V_o=0$
   - for MOS op-amps, V_{offset} is about 5~15mv

   for BJT op-amps, V_{offset} is about 1~2mv

Property of real op-amp(con't)

4.Common Mode Rejection Ration(CMRR)

- The CMRR measure how much the op-amp can suppress common-mode signals at its input

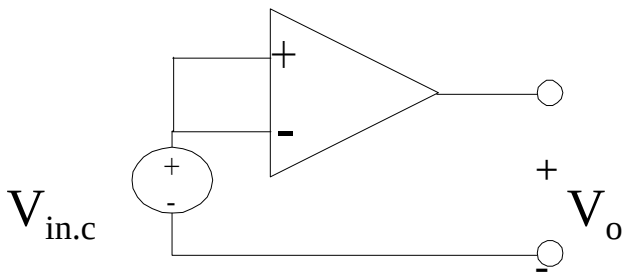
- Common-mode input voltage $V_{in.c}=\frac{(Va + Vb)}{2}$

  Differential-mode input voltage $V_{in,d}=V_a-V_b$

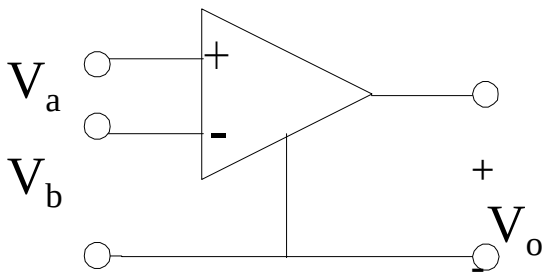
  Differential gain $A_d= V_o/ V_{in,d}$

  Common-mode gain $A_c= V_o/ V_{in,c}$

  CMRR= (A_d/A_c) or $20 \log_{10} (A_d/A_c)$ in dB (Typically 60~80dB)



Common-mode input



Differential-mode input

Property of real op-amp(con't)

5.Frequency Response

- Limited bandwidth(typically, 100MHz unity-gain bandwidth)
- Gain decreases at high frequencies , because

  a.stray capacitances

  b.finite carrier mobilities

6.Slew Rate(typically,for MOS op-amps,1~50V/μs)

- The maximum rate of output change dV_o/dt

7.Nonzero Output Resistance

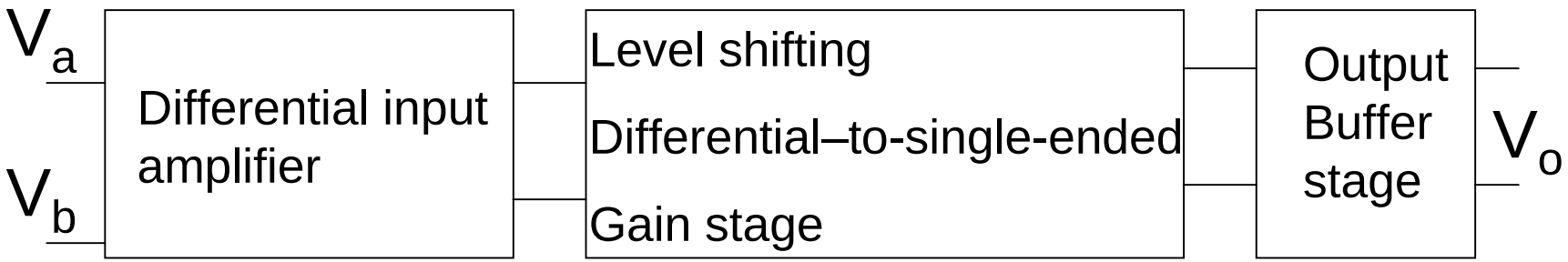
- Typically,0.1~5kΩ
- Large Ro will limit frequency response when a capacitor is connected to its output

Characteristics of Op-Amps

property	ideal	Practical(typical)
Open-loop gain	Infinite	Very high($A=10^2 \sim 10^4$)
Open-loop bandwidth	Infinite	Dominant pole (100MHz unity-gain bandwidth)
Common-mode rejection ratio	Infinite	High(60~80dB)
Input resistance	Infinite	High(>100MΩ)
Output resistance	Zero	Low(0.1~5kΩ)
Input current	Zero	Low(<0.5μA)
	Zero	Low(<10mV,<0.2nA)

Operational-amplifier architectures

The two-stage architecture



Differential amp provides:

- high input impedance
- large CMRR
- low offset voltage
- high gain

Operational-amplifier architectures(con't)

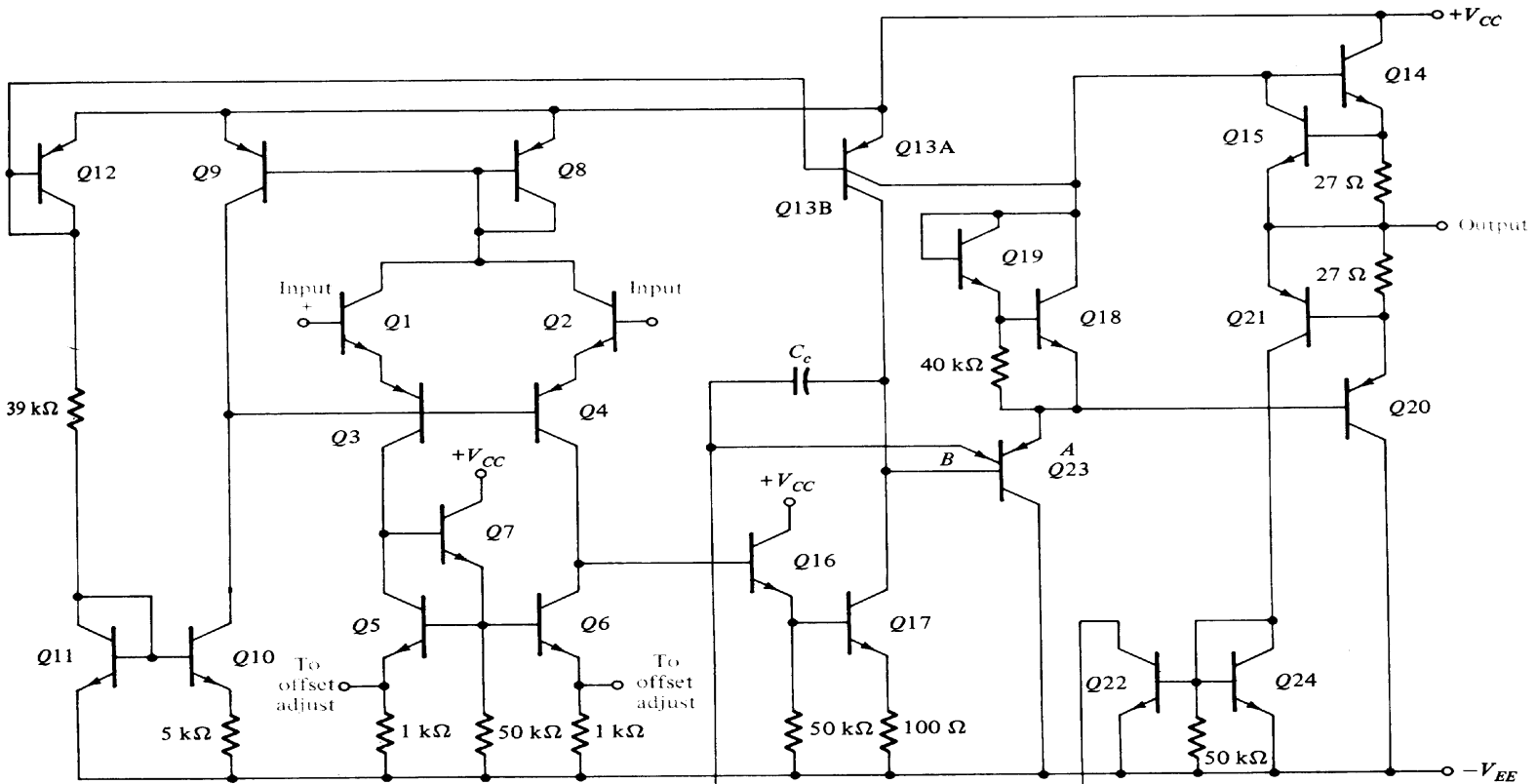
Second block provides:

- level shift
- added gain
- differential-to-single-ended conversion

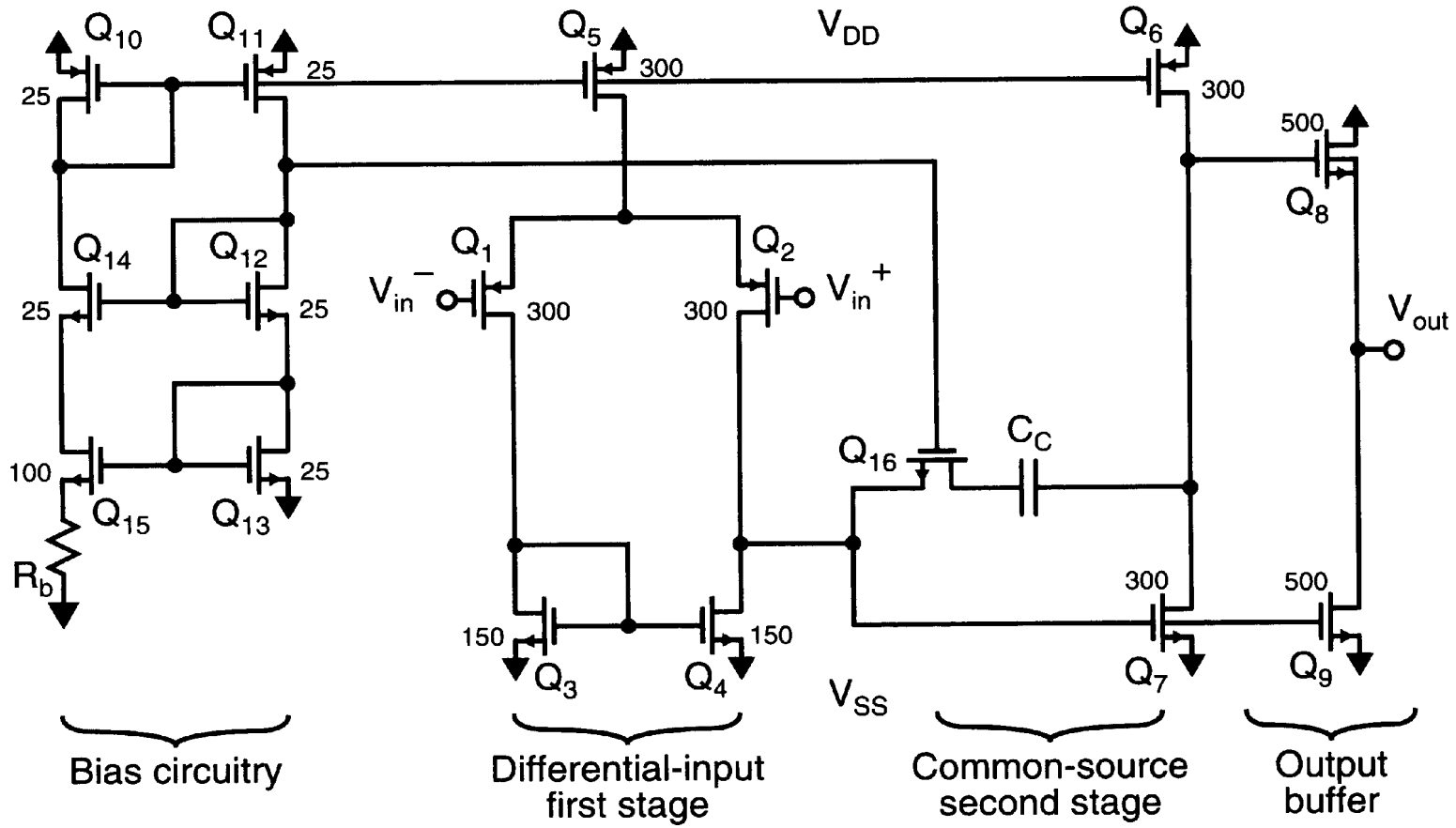
Output stage provides:

- low output impedance
- large driving capability

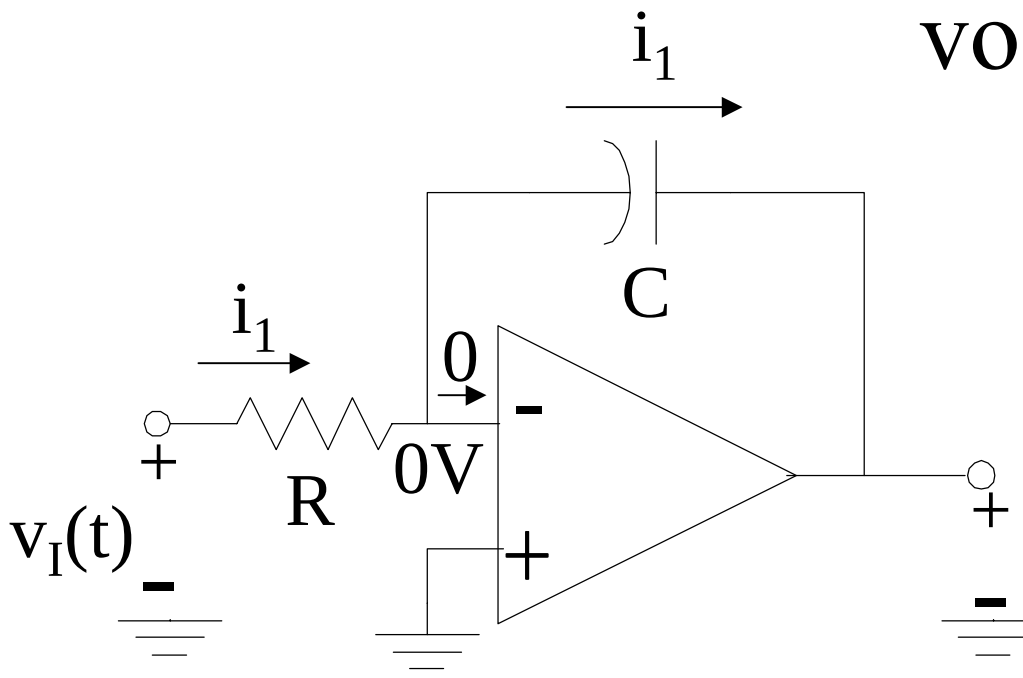
741 OPAMP (BJT)



TWO-STAGE CMOS OPAMP



Active-RC Integrator

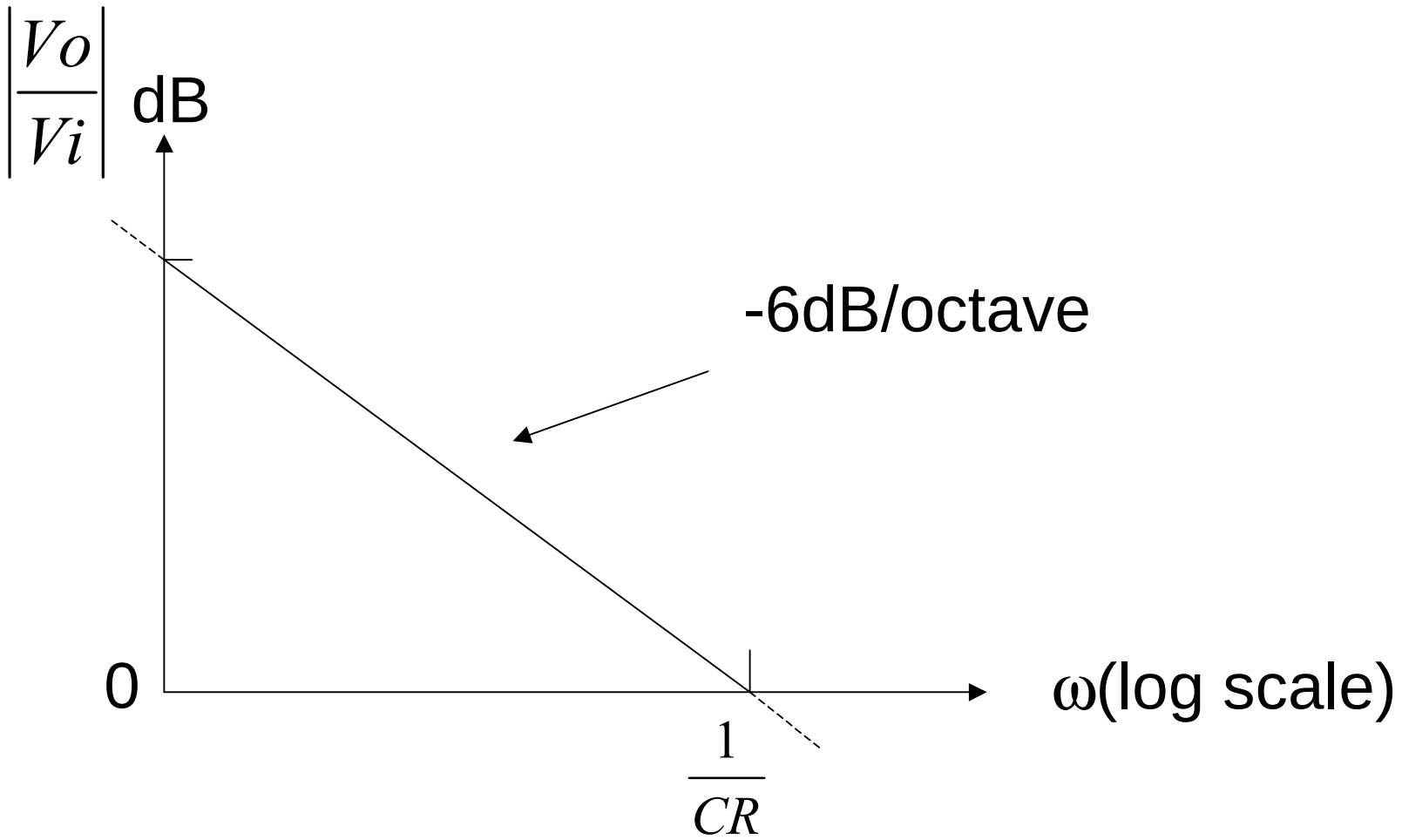


$$vo(t) = -\frac{1}{CR}\int_0^t vi(t)dt$$

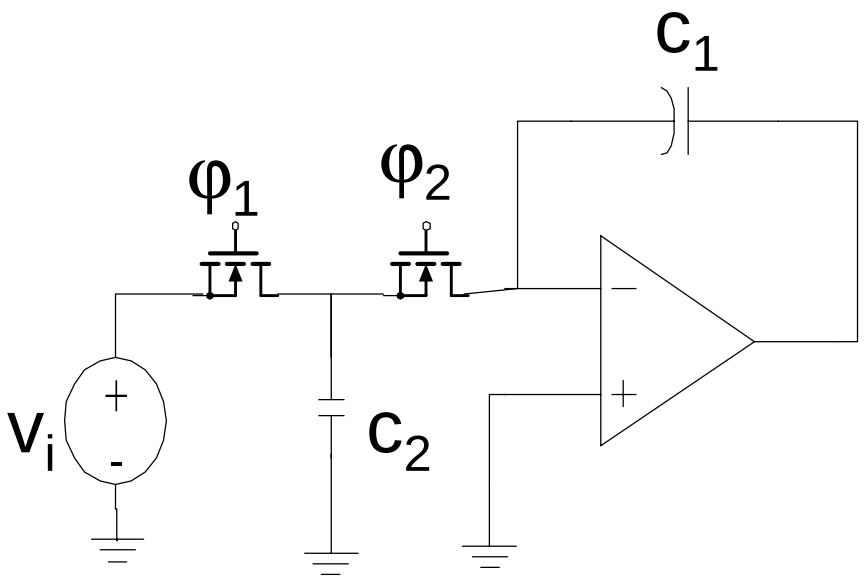
$$\frac{vo}{vi} = -\frac{1}{sCR}$$

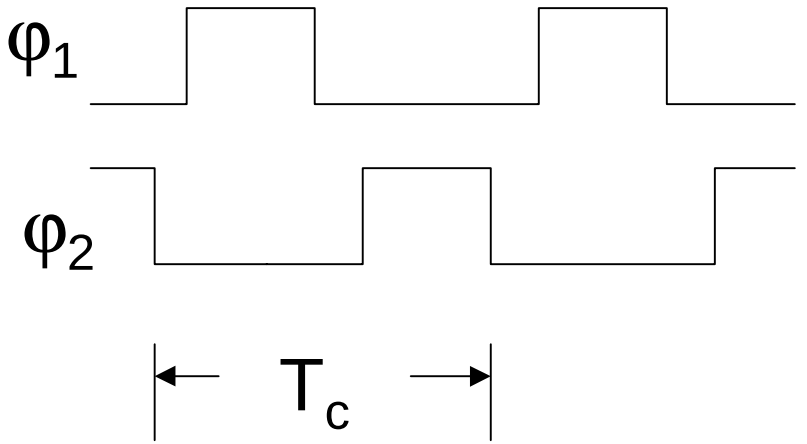
Miller or inverting integrator

Frequency response of the integrator

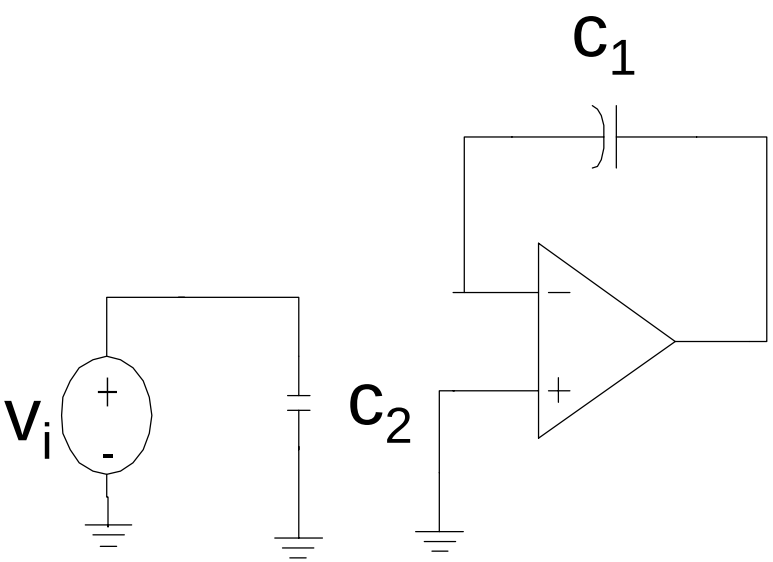


Switched-capacitor Integrator

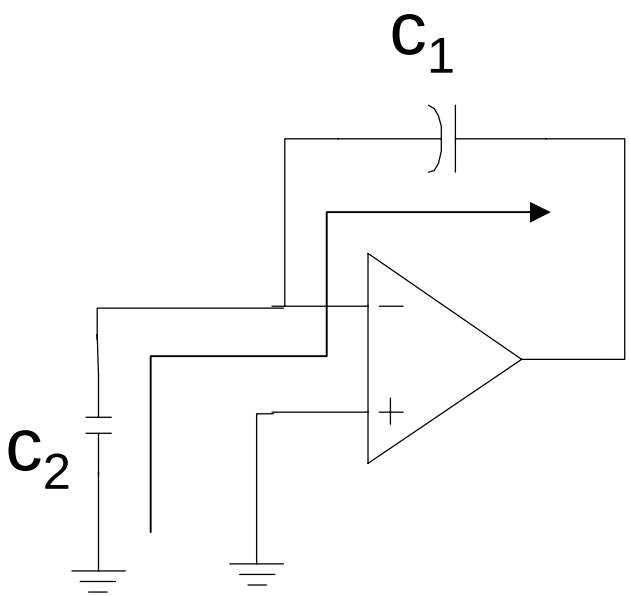




Switched-capacitor Integrator(con't)



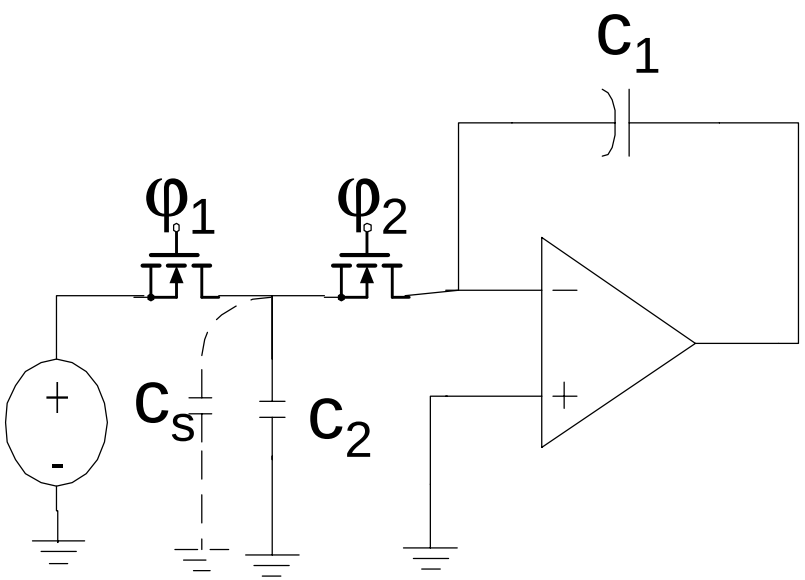
During ϕ_1



During ϕ_2

- $R_{eq} = T_c/C_2$
- Time constant $= C_1 R_{eq} = (T_c C_1)/C_2$

Switched-capacitor Integrator(con't)



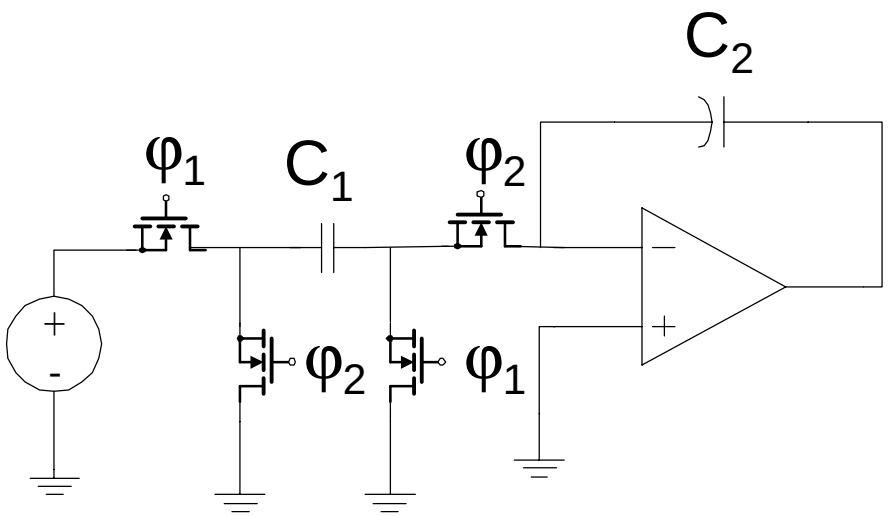
Advantage:

–Time constant=$(T_cC_1)/C_2$ can be well controlled in an IC process (The accuracy of capacitor ratios In MOS technology can be controlled to within 0.1%)

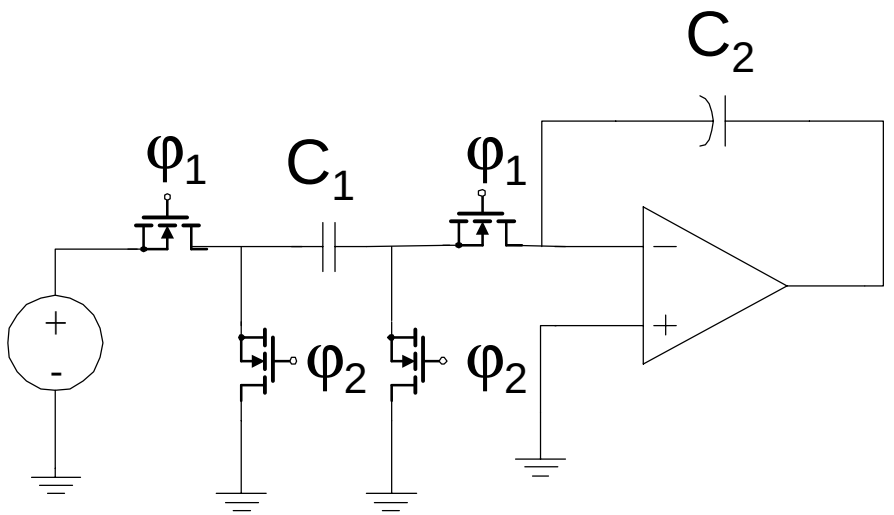
Disadvantage:

– it is sensitive to stray capacitances

Stray-insensitive switched-capacitor Integrator



Noninverting switched-capacitor integrator



inverting switched-capacitor integrator

A/D Converters

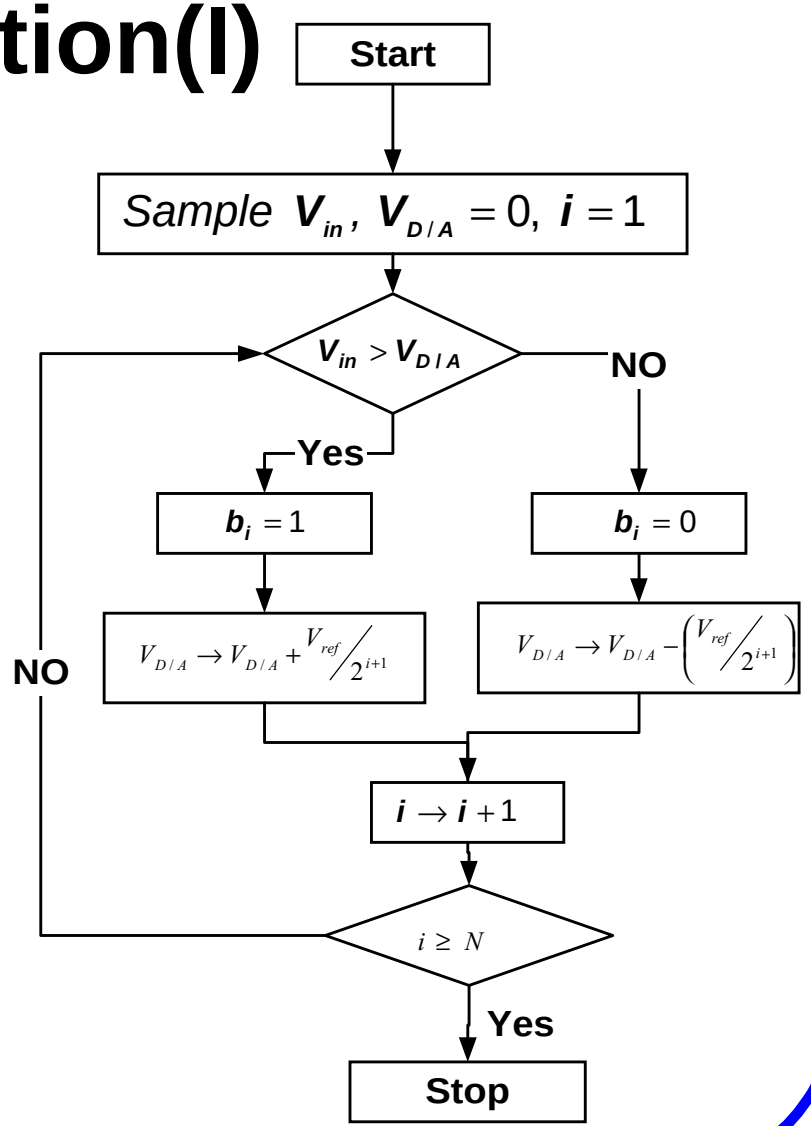
- Successive approximation
- Integrating
- Flash
- Sigma-delta

Successive Approximation(I)

- **Reasonably quick conversion time**
- **Moderate circuit complexity**
- **Basic ideal: Binary search to determine the closest digital word**
- **Signed Input: within**
- **Output: offset-binary coding**

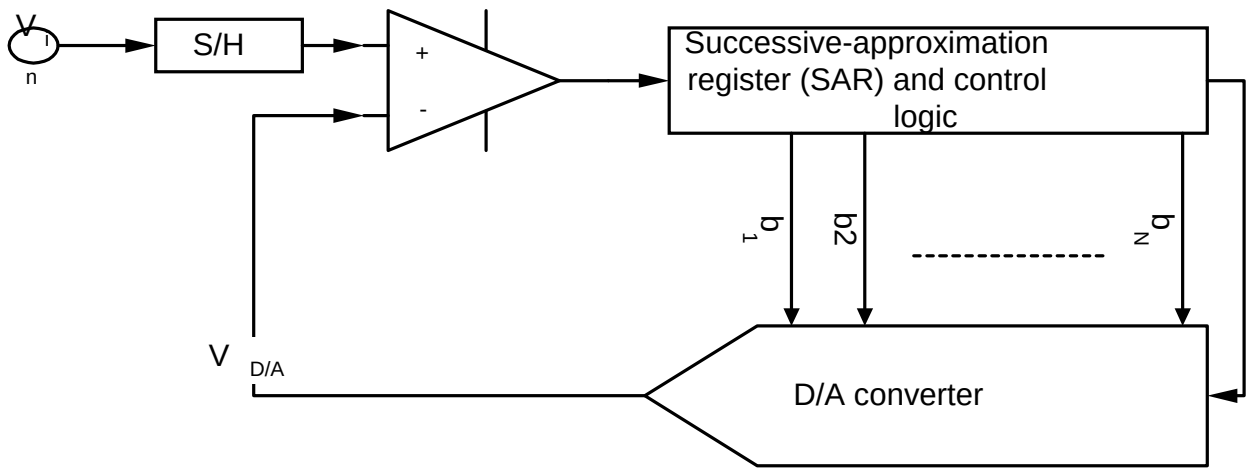
Ex : 2bit offset-binary code

Number	-2	-1	0	1
code	00	01	10	11



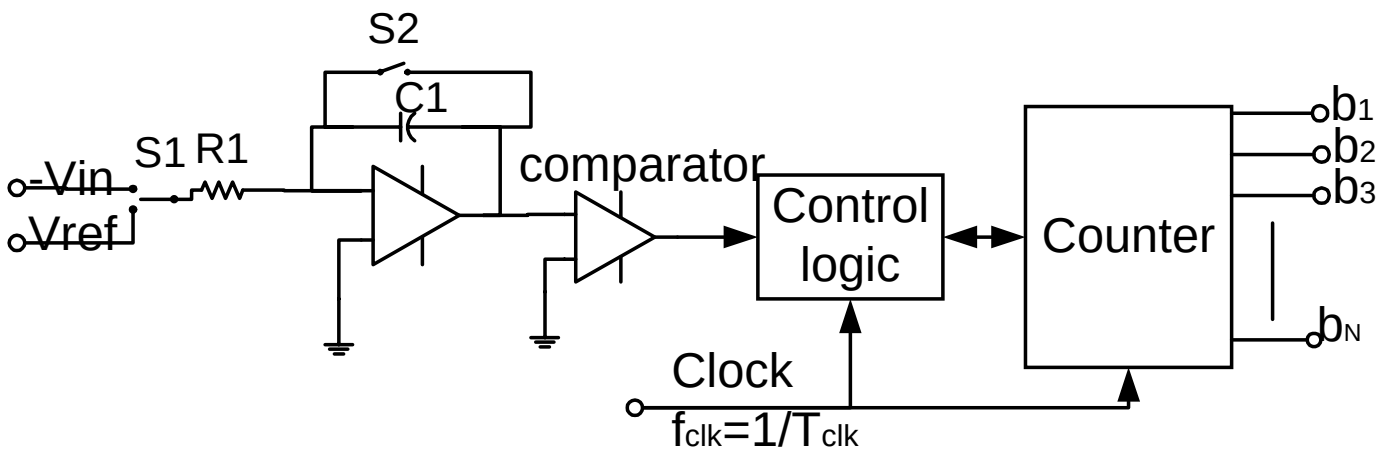
Successive Approximation(II)

- DAC-based successive approximation
  - internal DAC typically determines the accuracy and sped of the SA ADC.
  - sample/hold is required so that input does not charge during the conversion time.

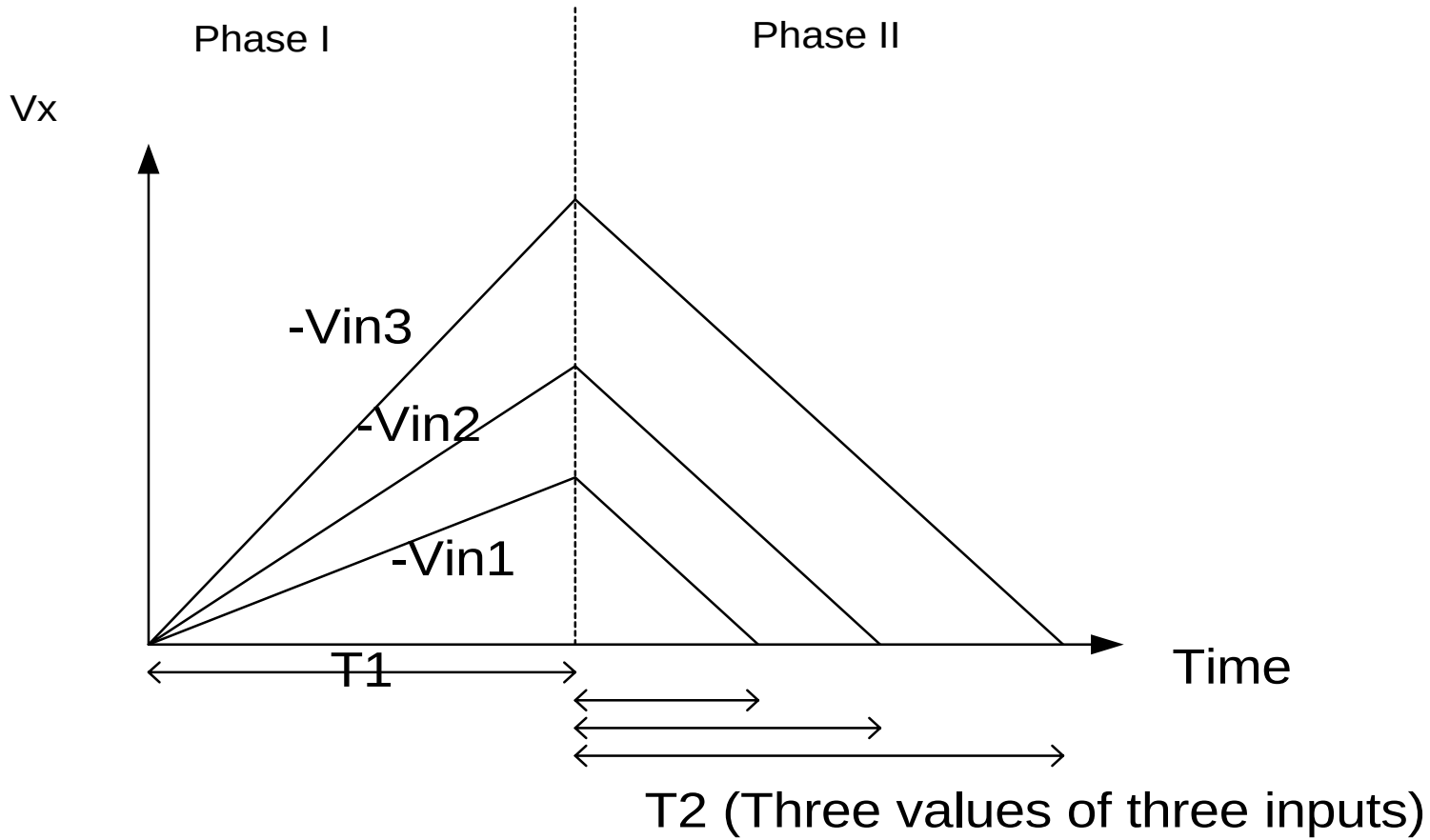


Integrating (or Dual-Slope ADC) (I)

- high-accuracy data conversion on very slow-moving signals
- Very low offset error, Very low gain error, Highly linear
- Small amount of circuitry required



Integrating (or Dual-Slope ADC) (II)



Integrating (or Dual-Slope ADC) (III)

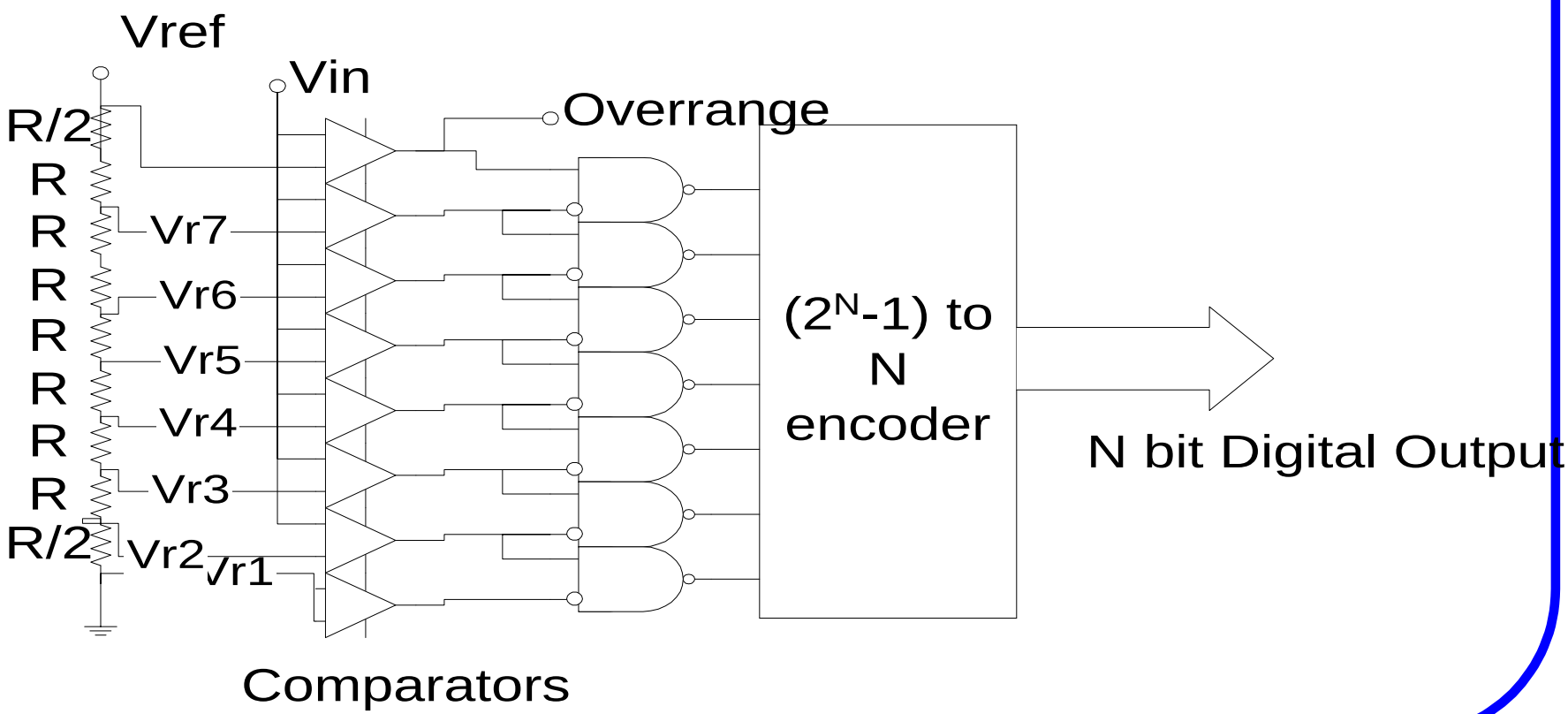
- **Basic ideal : Conversion is performed in two phases**
  - Phase I
    - fixed time interval of length T_1,$T_1=2^N T_{clk}$
      where T_{clk} is the period for one clock cycle
    - $S_1$is connected to $-V_{in}$ such that Vx ramps up proportional to the magnitude of V_{in}
    - At the end of phase I,
  - Phase II
    - At the beginning, counter is reset, S_1 is connected to V_{ref}, resulting in a constant slope for the decaying voltage at Vx
    - The counter simply counts until Vx is less than zero,and get T_2

Flash (I)

- Very-high-speed approach
- Large area and power hungry
  - 2^N comparators
  - 2^N reference voltages, V_{r1}, V_{r2}, ….,generated by a resistor string
- The invert gain must be large enough to amplify (V_{in}-V_{ri}) to V_{iH} and V_{iL} of its succeeding latches. Usually, gain＝25～100 for 8-bit resolution.

Flash (II)

Example: 8-bit A/D



Flash (III)

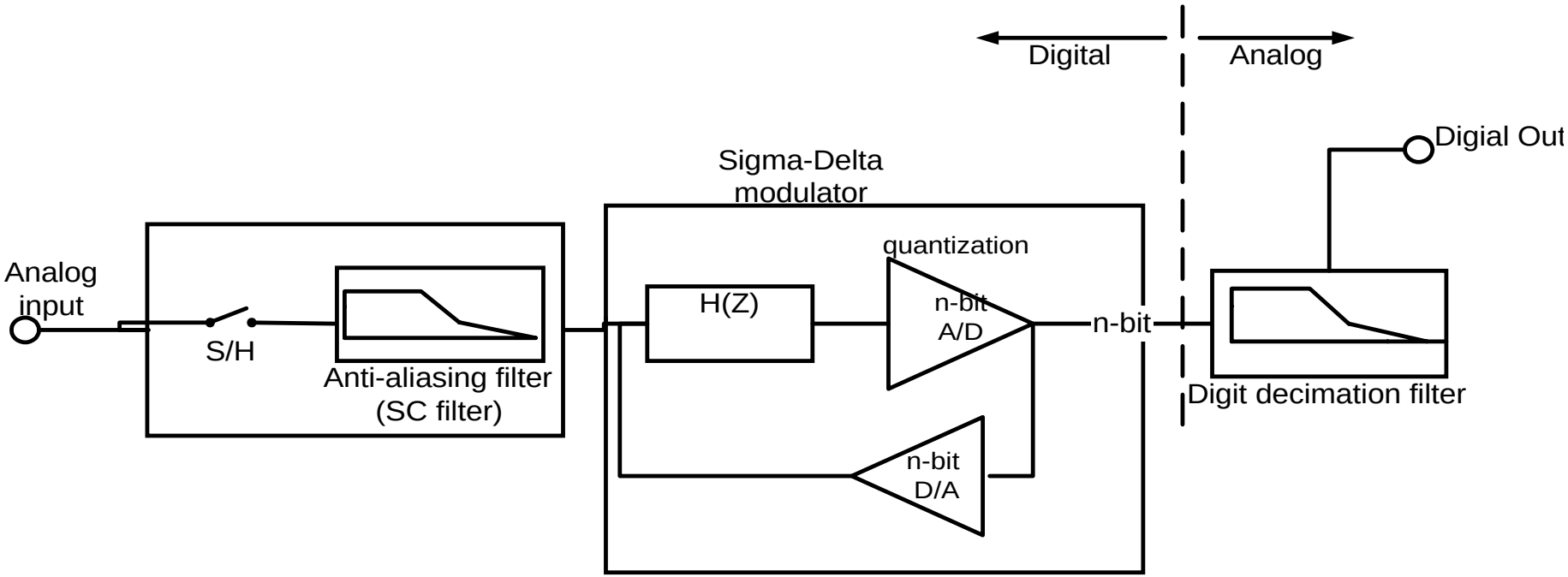
- **Issues in Designing Flash ADC**
  - Large input capacitive load
    - large number of comparators connected to Vin, and requires a strong and power hungry buffer
    - often limit the speed
  - **Resistor string bowing**
    - errors are greatest at the center node of the resistor string
    - considerable improvement obtained forcing the center tap voltage to be correct. (More voltage references)
  - **Comparator Latch-to-Track delay**
    - especially when a small input signal of the opposite polarity from the previous period is present
    - minimized by keeping the time constants of the internal nodes of the latch as small as possible.

Flash (IV)

- **Issues in Designing Flash ADC**
  - Signal and/or clock delay
    - Even very small differences in the arrival of clock or input signals at the different comparators can cause errors.
    - Ex:8bit 250MHz ADC, if clock skew between comparators greater than 5ps, the converter will have more than 1 LSB error.
  - **Substrate and power supply noise**
    - 7.8mV of noise injection would cause a 1LSB error for an 8-bit convertor with V_{ref}=2V
  - **Bubble error**
    - error due to comparator metastability, noise, cross talk, limited bandwidth, …,etc.
  - **Flashback**
    - caused by latched comparators when they are switched from track to latch mode.

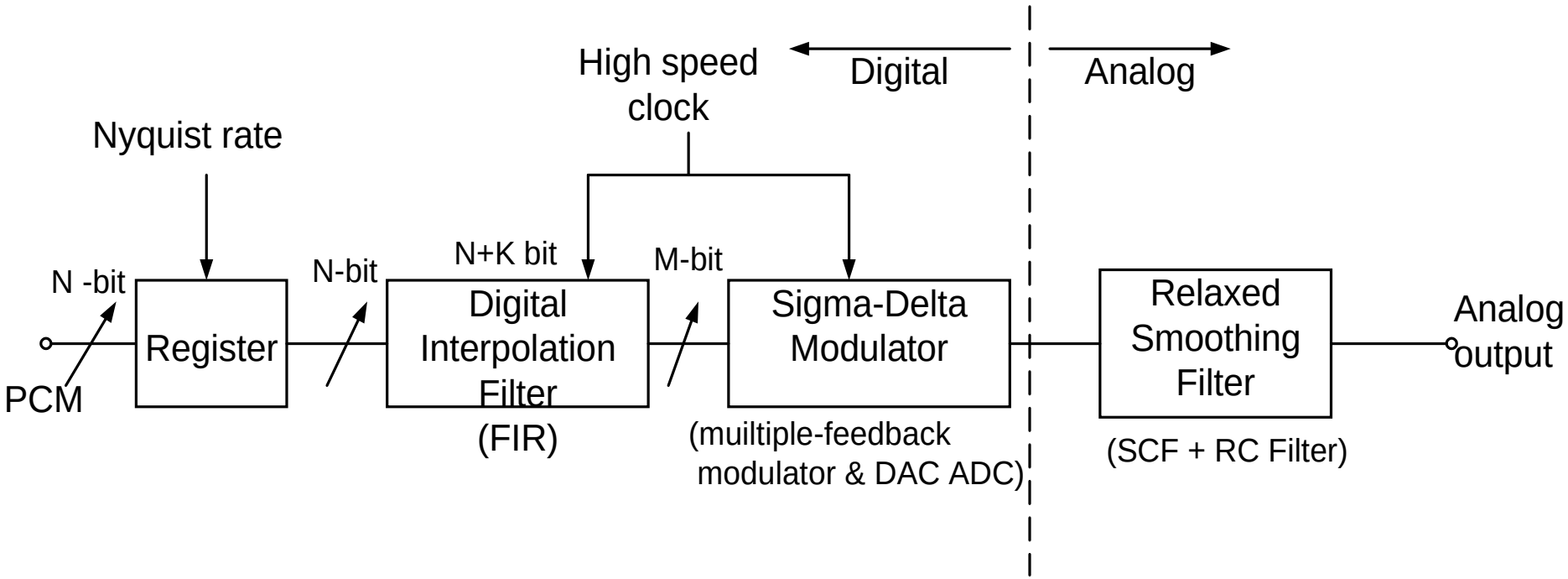
Sigma-delta(I)

- **Block diagram of a $\sum \triangle$ A/D converter**



Sigma-Delta(II)

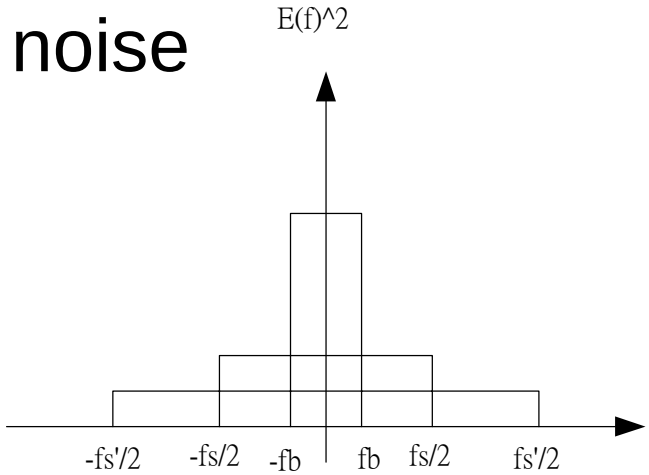
- **Block diagram of a $\Sigma\triangle$ D/A converter**



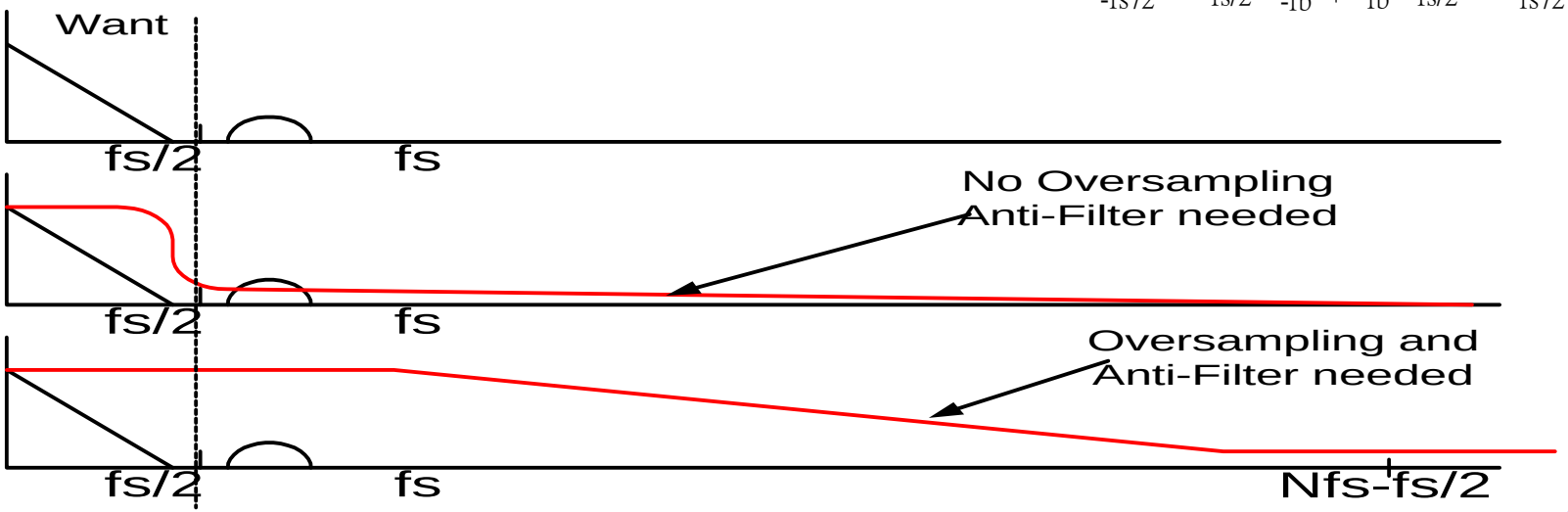
Sigma-Delta(III)

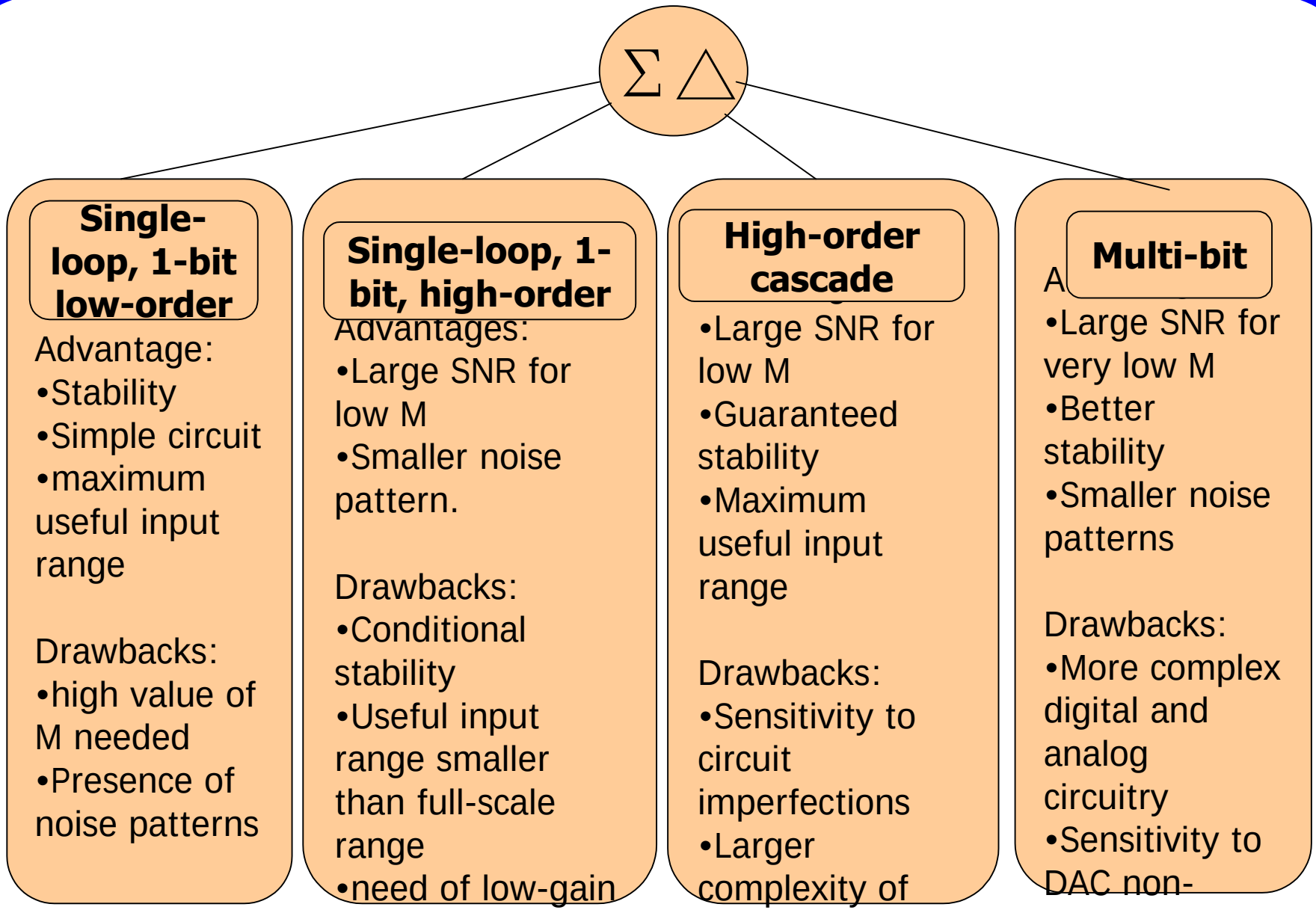
- Oversampling and quantization noise

$$\text{Quantization noise } E^2 = \frac{LSB^2}{12}\frac{1}{Fs}$$



- Oversampling and Anti-filter




ΣΔ
Single-loop, 1-bit low-order
Advantage:
•Stability
•Simple circuit
•maximum useful input range
Drawbacks:
•high value of M needed
•Presence of noise patterns
Single-loop, 1-bit, high-order
Advantages:
•Large SNR for low M
•Smaller noise pattern.
Drawbacks:
•Conditional stability
•Useful input range smaller than full-scale range
•need of low-gain integrators
High-order cascade
•Large SNR for low M
•Guaranteed stability
•Maximum useful input range
Drawbacks:
•Sensitivity to circuit imperfections
•Larger complexity of the digital part
Multi-bit
•Large SNR for very low M
•Better stability
•Smaller noise patterns
Drawbacks:
•More complex digital and analog circuitry
•Sensitivity to DAC non-linearity

Sigma-Delta(IV)

- **Structure**
  - Single-loop high-order modulators
    - Feedforward (FF) modulator
    - Multiple-feedback (MF) modulator
  - Cascade modulators(MASH: Multi-stage noise shaping)
- **Stability**
  - High order(> 3 order) : non stable and little input level
  - Make sure stable:
    - Proper selection of scaling coefficient
    - Taking advantage of the bounded nature of signals at integrator output, or including limiters
    - Global resetting of the integrator when an unstable operation is detected

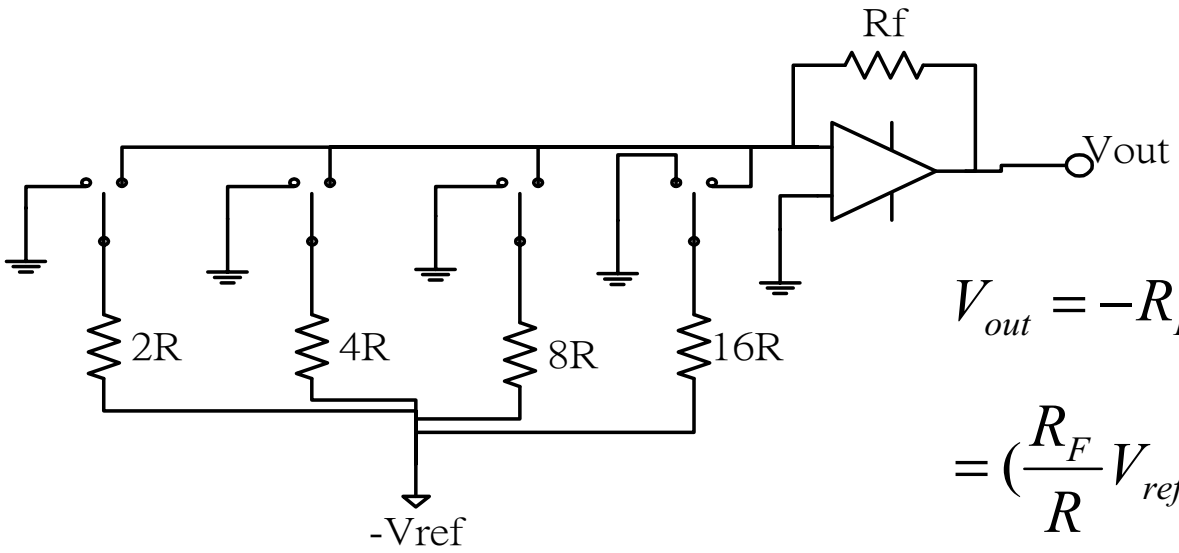
D/A Converters

- Weighted resistors
- Fixed references
- Multiple

Weighted resistors

- An appropriate set of signals that are all selected in a binary fashion
- The binary array of signals might be voltages, changes, or currents
- DAC
  - Binary-weighted resistor DAC
  - Reduced-resistance-ratio ladders
  - R-2R-based DAC
  - charge-redistribution switched-capacitor DAC
  - current-mode DAC

Binary-Weighted Resistor



$$V_{out} = -R_F V_{ref}(-\frac{b_1}{2R} - \frac{b_2}{4R} - \frac{b_3}{8R} - .....)$$

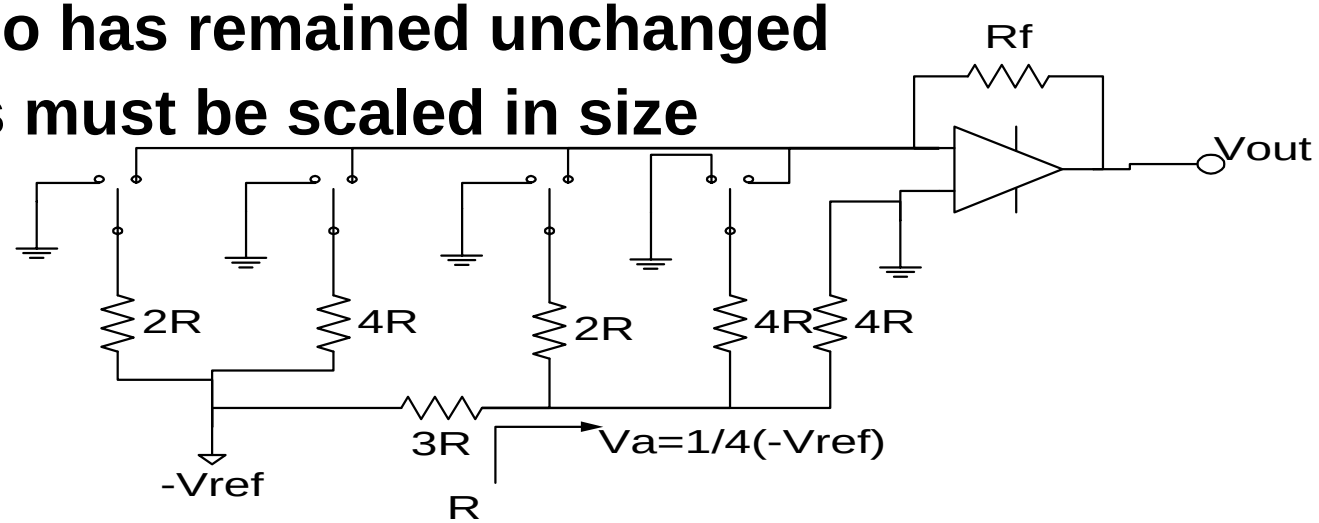
$$= (\frac{R_F}{R} V_{ref}) B_{in}$$

- **Does not require many resistor or switches**
- **Disadvantages**
  - **Resistor ratio and current ratio are on the order of**
  - **monotonicity is not guaranteed**
  - **prone to glitches**

Reduced-resistance-ratio ladders

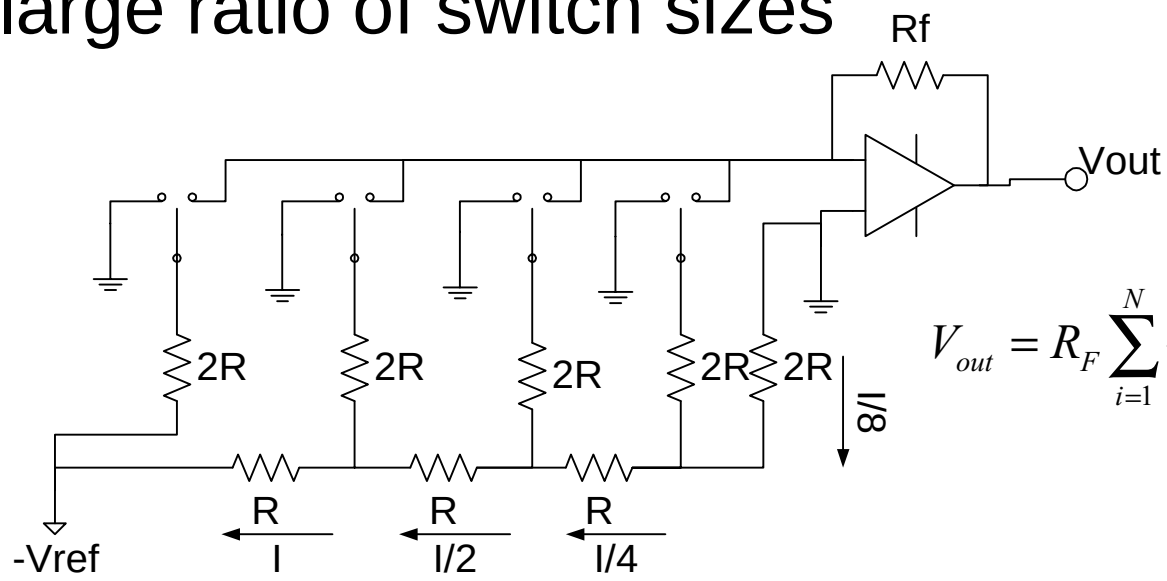
- Reduce the large resistor ratios in a binary-weighted array
- Introduce a series resistor to scale signals in portions of the array V_A=-1/4 V_{ref}
- An additional 4R was added such that resistance seen to the right of the 3R equals R.
- One-forwith the resistance ratio compared to the binary-weighted case
- Current ratio has remained unchanged

  =>Switches must be scaled in size



R-2R-based DAC

- Smaller size and better accuracy than a binary-sized approach
  - resistance ratio of only 2
- Current ratio is still large
  =>large ratio of switch sizes

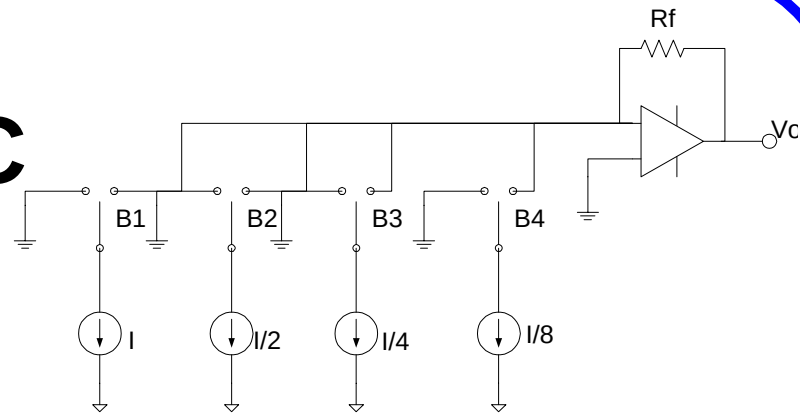


$$V_{out} = R_F \sum_{i=1}^{N} \frac{b_i I_r}{2^{i-1}} = V_{ref}\left(\frac{R_F}{R}\right)\sum_{i=1}^{N} \frac{b_i}{2^i}$$

Charge-redistribution Switched-Capacitor DAC

- Replace R into switch and capacitor in previous DAC
- Insensitive to OPAMP input-offset voltage, 1/f noise, and finite amplifier gain
- An additional sign bit can be realized by interchanging the clock phases(shown in parentheses)

Current-Mode DAC



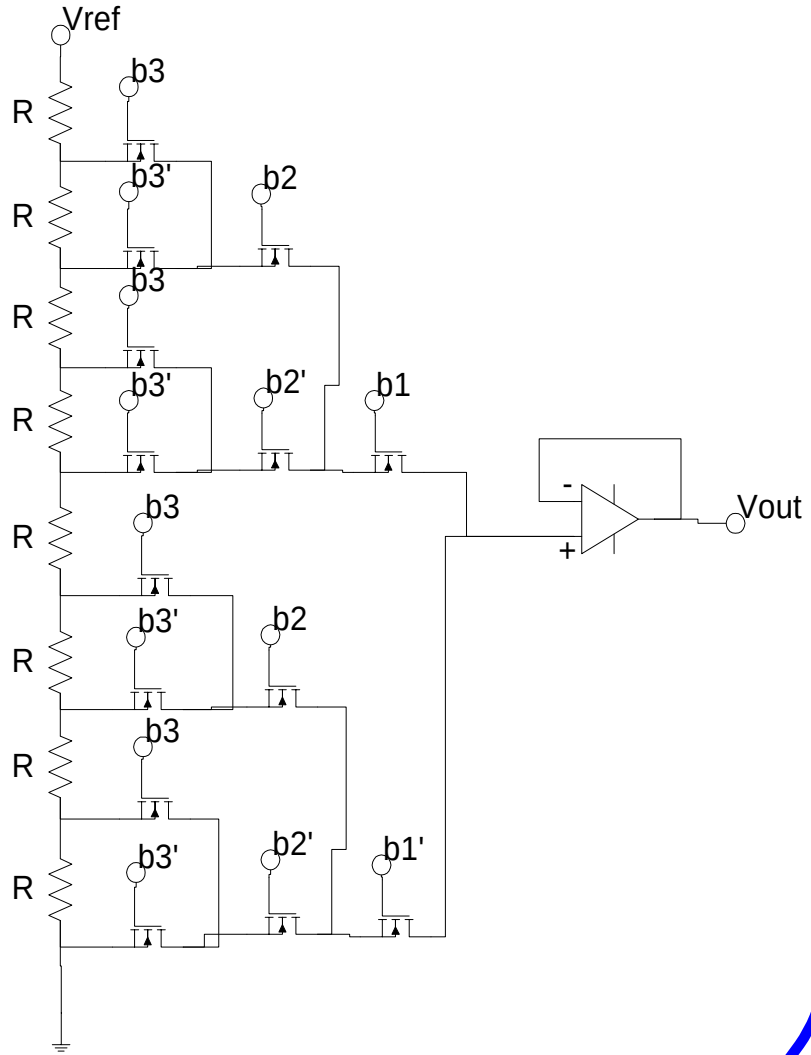
- High-speed
- Switch current to output or to ground
- The output current is converted to a voltage through R_F
- A major limitation during high-speed operation→Glitches
- Glitch disturbance can be reduced by
  - limiting the bandwidth (placing a capacitor across R_F)
    - This method slows down the circuit.
  - using a sample and hold on the output signal to a thermometer code.
  - modifying some or all of the digital word from a binary code to a thermometer code.(most popular method.)

Fixed references(Decoder-based DAC)

- Most straight forward approach
  - Create 2^N reference signals and pass the appropriate signal to the output
- Resistor string
- Folded resistor-string

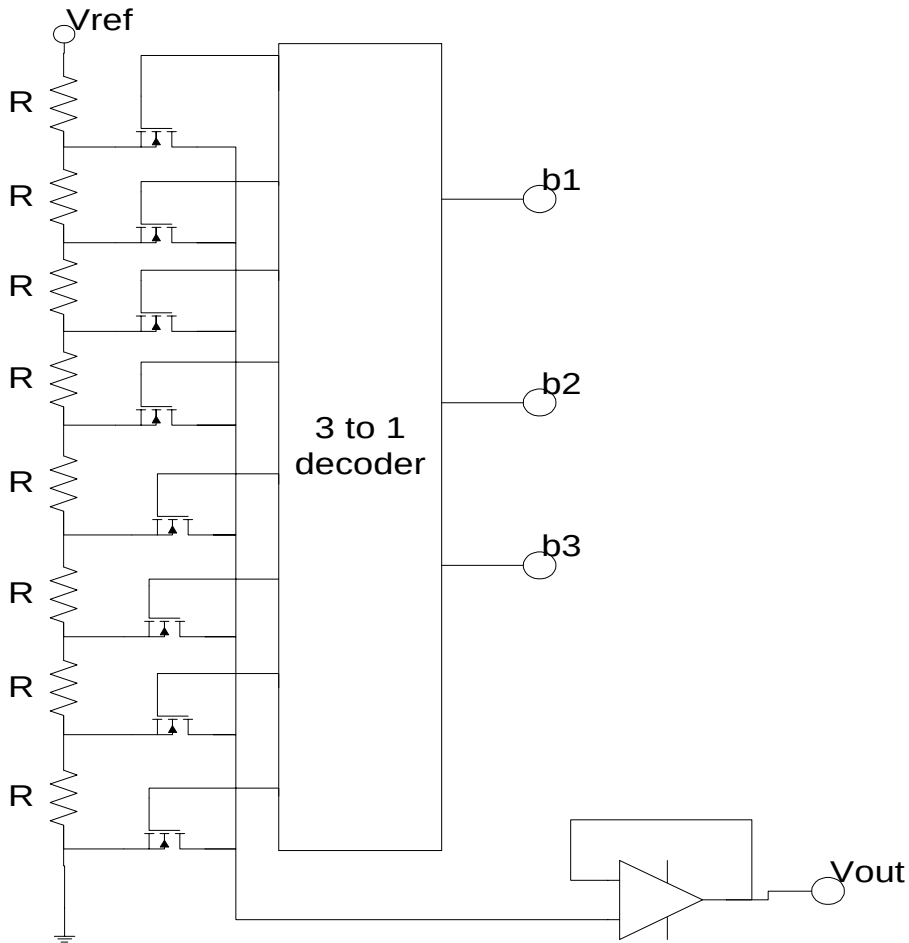
Resistor string

- Example 1: a 3-bit DAC with transmission-gate, tree-like decoder
- Time-constant $\approx 3R_{tr}C_{tr}+2\bullet 3R_{tr}C_{tr}+\ldots\ldots+N\bullet 3R_{tr}C_{tr}=N(N+1)/2 *3\ R_{tr}C_{tr}$



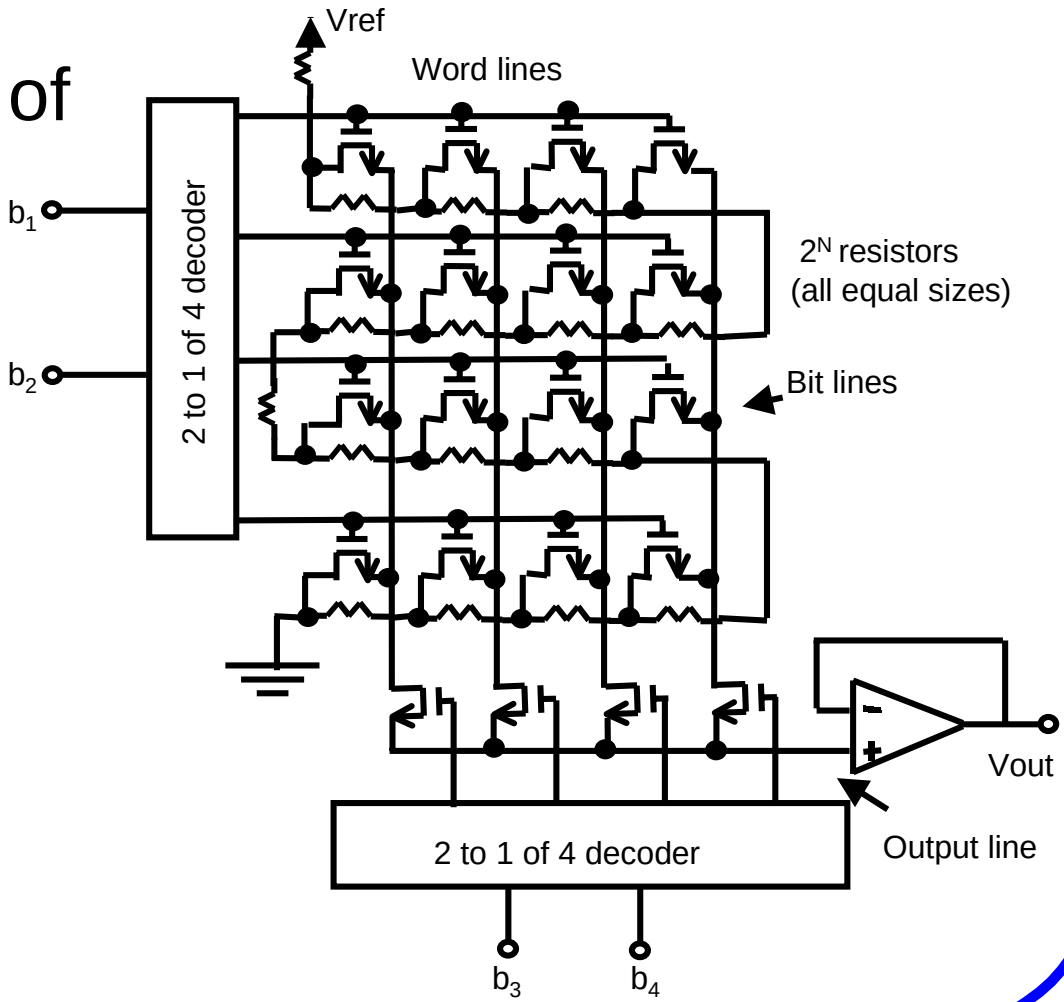
Resistor string

- Example 2: a 3-bit DAC with digital decoding
- Time-constant ≈ $R_{tr} \bullet 2^N C_{tr}$



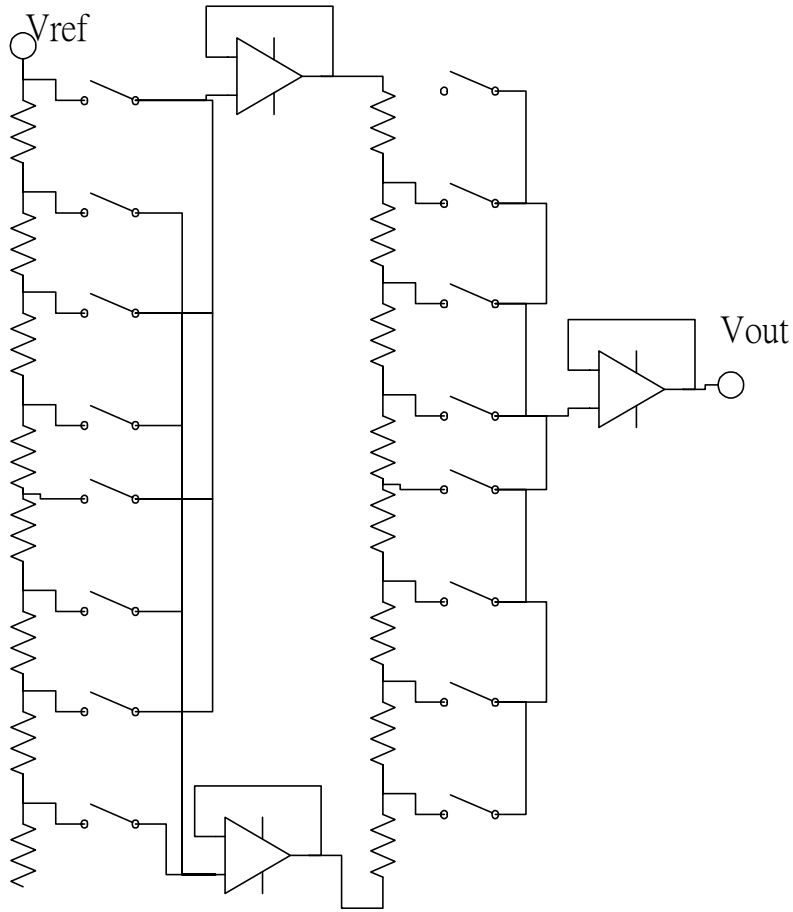
Folded resistor-string

- Reduce the amount of digital decoding
- Reduce large capacitive loading
- Decoding is very similar to that for a digital memory



Multiple

- **Requires only $2*2^{N/2}$ resistors**
- **Monotonic if OPAMPS have matched, voltage-insensitive offset voltages.**
- **For high speed, OPAMPS must be fast.**
- **For high resolution, OPAMPS must be low noise.**
- **The matching requirements of the second resistor string are not nearly as severe as those for the first string.**
  - The second resistor string is used to decode only lower-order bits



Parameters of ADC &DAC

- Resolution & accuracy
- A/D conversion time & D/A settling time
- Rise & fall time
- Signal to noise ratio
- Dynamic Range
- Harmonic distortion & Intermodulation distortion

Parameters of ADC &DAC

- Differential nonlinearity (DNL)
- Integral nonlinearity (INL)
- Gain and offset errors
- Monotoicity
- Missing codes
- Slew rate
- Overshoot

Resolution & Accuracy

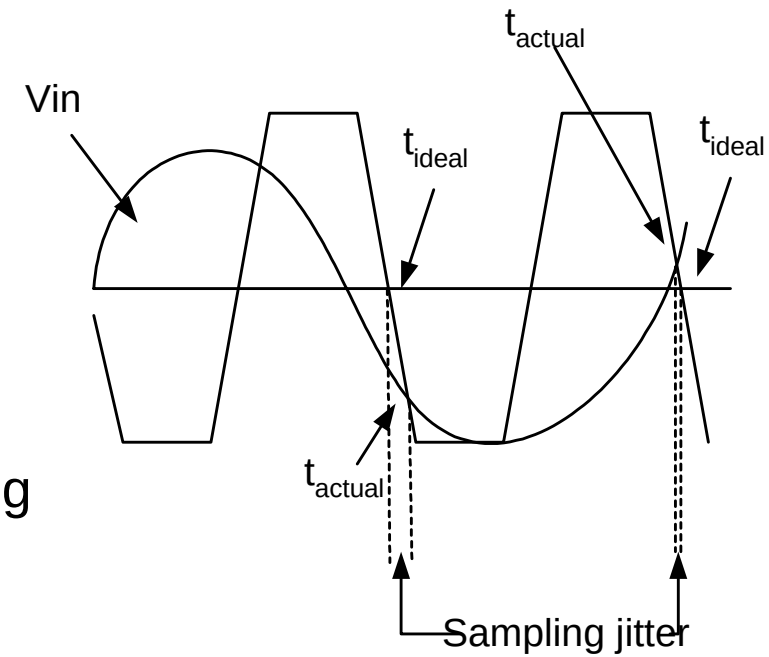
- **Resolution**
  - the number of distinct analog levels corresponding to different digital words. i.e. N-bit resolution implies distinct analog levels.
  - Resolution is not necessarily an indication of the accuracy of the converter, but instead it usually refers to the number of digital input or output bits.
- **Accuracy**
  - **Absolute accuracy**
    - the difference between the expected and actual and transfer responses
    - Includes offset, gain and linearity errors
  - **Relative accuracy**
    - the accuracy of offset and gain errors have been removed
    - a 12-bit accuracy implies that the converter's error is less than the (full-scale/2^{12})

A/D Conversion Time, D/A Settling Time

- **A/D conversion time & sampling Rate**
  - The conversion time is the time taken for the converter to complete a single measurement including acquisition time for the input signal.
  - the sampling rate is the speed at which sampling can be continuously converted and is typically the inverse of the conversion time.
- **D/A Settling Time**
  - the settling time is defined as the time it takes for the converter to within some specified amount of final value(usually 0.5LSB).
  - The sampling rate is the rate at which sample can be continuously converted and is typically the inverse of the settling time.
- **Both A/D and D/A converter have limited accuracy when their sampling instance are ill defined**.

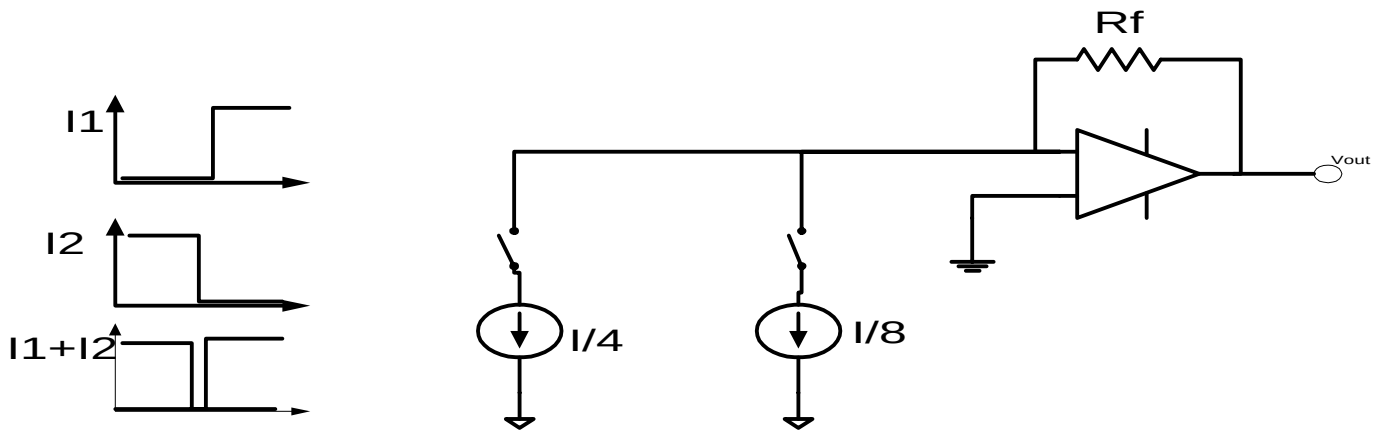
Rise & Fall Time (I)

- **Cause sampling jitter & glitch**
  - **Sampling jitter**
    - This error is result of the effective sampling time changing from one sampling instance to the next and becomes more pronounced for high-speed signals.
    - When high-speed signals are being sampled, the input signal changes rapidly, resulting in small amounts of aperture uncertainly causing the held voltage to be significantly different from the ideal held voltage



Rise & Fall Time (I)

- **Glitch**
  - Glitches are a major limitation during high-speed operation for converter that have digital logic
  - Glitches area mainly the result of different delay occurring when switching different signals.
  - The glitch disturbance can be reduced by limiting the bandwidth
  - In DAC, thermometer-based converter does have advantages over its binary counterpart, such as low DNL errors, guaranteed monotonicity, and reduced glitching noise



Signal to Noise Ratio(SNR) (I)

- The signal to noise ratio(SNR) value (in dB) of a signal node in a system is defined as

$$SNR = 10 \log[\text{signal power/noise power}]$$

$$= 10 \log[V^2_{x(rms)} / V^2_{n(rms)}]$$

$$= 20 \log[V_{x(rms)} / V_{n(rms)}]$$

where $V_{x(rms)}$ is a normalized signal of a node in a circuit, $V_{n(rms)}$ is a normalized noise power

Signal to Noise Ratio(SNR) (II)

- **If V_x is a sawtooth of heght V_{ref} (or a random signal uniformly distributed between 0 and V_{ref}),and noise only quantization noise $V_{Q(rms)}=V_{LSB}/\sqrt{12}$**

  $SNR=20\log [V_{x(rms)} / V_{Q(rms)}]$

  $=20\log [(V_{ref(rms)}/\sqrt{12}) / (V_{LSB(rms)}/\sqrt{12})]$

  $=20\log(2^N) = 6.02\ N\ dB$

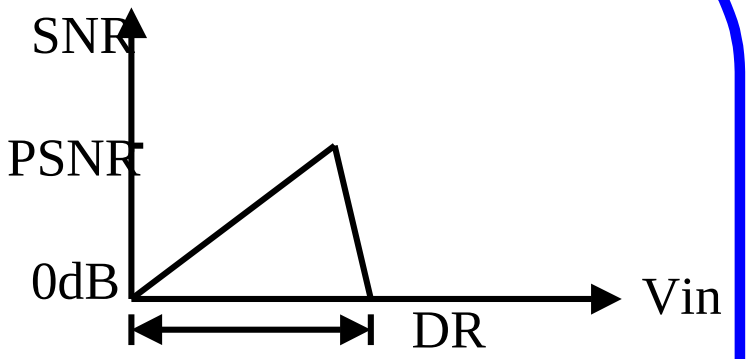
- **If V_x is a sinusoidal waveform between 0 and V_{ref}.**

  $SNR=20\log [V_{x(rms)} / V_{Q(rms)}]$

  $=20\log [(V_{ref(rms)}/2\sqrt{2})/ (V_{LSB(rms)}/\sqrt{12})]$

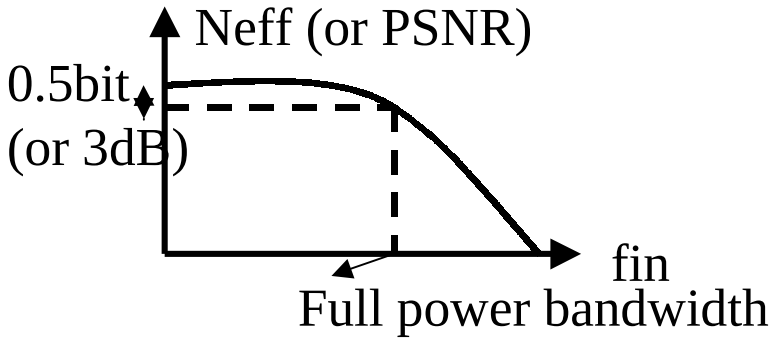
  $=20\log(\sqrt{3/2}\,2^N) = 6.02N + 1.76\ dB$

Dynamic Range(DR) (I)



- Two different definitions:
  1. The ratio of maximum amplitude input sinusoidal to minimum amplitude input sinusoidal.
     - maximum input: input with PSNR or maximum allowable input.
     - minimum input : input with SNR=0.
  2. Effective number of bit using the equation PSNR=6.02Neff+1.76dB where 1 is commonly used.

Dynamic Range(DR) (II)



- DAC

  analog output measured using spectrum analyzer
- ADC

  digital output analyzer using Fast Fourier Transform(FFT).
- Dynamic Range is function of the frequency of the sinusoidal input

Harmonic Distortion & Intermodulation Distortion

- **Nonlinear Distortion**
- **For the application of a certain device(amplifier or mixer** ……)
  - One of the series term provides the desired output
  - The remaining term produce undesired spurious signals which correspond to conversion loss & signal distortion
- **If input vi=Acosw_1t ➔Single tone test (only HD)**

  output vo: vo=k1vi+k2vi^2+k3vi_3+……

Then,

$$
\begin{aligned}
Vo &= k_1 v_i + k_2 v_i^2 + k_3 v_i^3 + \ldots \\
&= k_1 A \cos w_1 t + k_2 A^2 \cos^2 w_1 t + k_3 A^3 \cos^3 w_1 t + \ldots \\
&= k_1 A \cos w_1 t + k_2 A^2 \left(\tfrac{1}{2} + \tfrac{1}{2}\cos 2w_1 t\right) + k_3 A^3 \left(\tfrac{3}{4}\cos w_1 t + \tfrac{1}{4}\cos 3w_1 t\right) \\
&= \tfrac{1}{2} k_2 A^2 + \left(k_1 A + \tfrac{3}{4} k_3 A^3\right)\cos w_1 t + \tfrac{1}{2} k_2 A^2 \cos 2w_1 t + \tfrac{1}{4} k_3 A^3 \cos 3w_1 t
\end{aligned}
$$

Harmonic Distortion & Intermodulation Distortion

If input vi: vi=A(cosw_1t +cosw_2t) ➔Two-tone test

output vo: vo=k0+k1vi+k2vi^2+k3vi_3+……

Then,

$$Vo = k_0 + k_1 v_i + k_2 v_i^2 + k_3 v_i^3 + \ldots$$

$$= k_0 + k_1 A \quad w_1 t + \quad w_2 t \; + k_2 A^2 \quad w_1 t + \quad w_2 t^{\;2} + k_3 A^3 \quad w_1 t + \quad w_2 t^{\;3} + \ldots$$

$$= k_0 + k_2 A^2$$

$$+ k_2 A^2 \quad w_1 - w_2 \; t + k_2 A^2 \quad w_1 + w_2 \; t \qquad {}_1 \pm {}_2$$

$$+ \; k_1 A + \diagup\, k_3 A^3 \quad w_1 t + \; k_1 A + \diagup\, k_3 A^3 \quad w_2 t \qquad {}_1 \; w_2$$

$$+ \diagup\, k_2 A^2 \quad w_1 t + \diagup\, k \; A \quad w \; t \qquad {}_1$$

$$+ \diagup\, k \; A \quad w_1 t + \diagup\, k \; A \quad w \; t \qquad {}_1$$

$$+ \diagup\, k \; A \quad w_1 - w \; \; t + \diagup\, k \; A \quad w \; - w_1 \; t \qquad {}_1 \qquad {}_1$$

$$+ \diagup\, k \; A \quad w_1 + w \; \; t + \diagup\, k \; A \quad w \; + w_1 \; t \qquad {}_1 + \qquad + \; {}_1$$

$$+ \ldots\ldots$$

Integral Nonlinearity (INL)

- INL error is defined to be the deviation from a straight line, after both the offset and gain error have been removed.
  - A conservative measure of nonlinearity is to use the endpoints of the converter's transfer response to define the straight.
  - An alternate define is to find the best -fit straight line such that the maximum difference (or perhaps the mean squared error) is minimized.

Differential Nonlinearity(DNL)

- DNL is defined as the variation in analog step sizes away from 1LSB (typically, once gain and offset error have been removed).
- an ideal converter has it’s maximum DNL of 0 for all digital values, where as a converter with a maximum DNL of 0.5 LSB has its step size varying from 0.5LSB to 1.5LSB.

Gain and Offset Errors(I)

- Gain Error:
  - Gain error is the difference at the full-scale value between the ideal and actual when the offset error has been reduced to zero.
  - DAC
    - Egain(DAC)=($\left.\frac{Vout}{VLSB}\right|_{1\ldots1}$ - $\left.\frac{Vout}{VLSB}\right|_{0\ldots0}$)- (2^N -1)
  - ADC
    - Egain(ADC)=($\frac{V_{1\ldots1}}{VLSB}$ - $\frac{V_{0\ldots01}}{VLSB}$) – (2^N – 2)

Gain and Offset Errors(II)

- **Offset Error**
  - **DAC**
    - offset error is the output that occurs for the input code that should produce zero output .
    - $Eoff_{(DAC)} = V_{out} / V_{LSB|0.....0}$
  - **ADC**
    - Offset error is the deviation of $V_{0...01}$ from 1/2LSB
    - $Eoff_{(ADC)} = \frac{V_{0..01}}{V_{LSB}}$ - 1/2LSB

Monotonicity

- Monotonicity mean the output always increase as the input increases.
- A monotonic D/A , the slope of the D/A converter's transfer response is of only one sign.
- If the maximum DNL error is less than 1LSB, then a D/A converter is guaranteed to be monotonic. However, many monotonic converter may have a maximum DNL greater than 1 LSB.
- Similarly,a converter is guaranteed to be monotonic if the maximum INL is less than 0.5LSB.

Missing Codes

- Although monotonicity is appropriate for D/A converters, the equation term for A/D converter is missing codes.
- An Q/D converter is guaranteed not to have any missing codes if the maximum DNL Error is less than 1LSB or if the maximum INL error is less than 0.5LSB.

Slew rate

- The slew rate is the maximum rate at which the output changes when input signal are large
- Additional slewing time greatly increase the distortion and also increase the transient time during slew rate limiting(which occurs often for opamps used in switched-capacitor applications).
- In non-oversampled D/A converter the largest distortion mostly occurs at the high frequency end of the frequency band.This distortion results from the finite slew rate of output amplifiers.

Overshoot

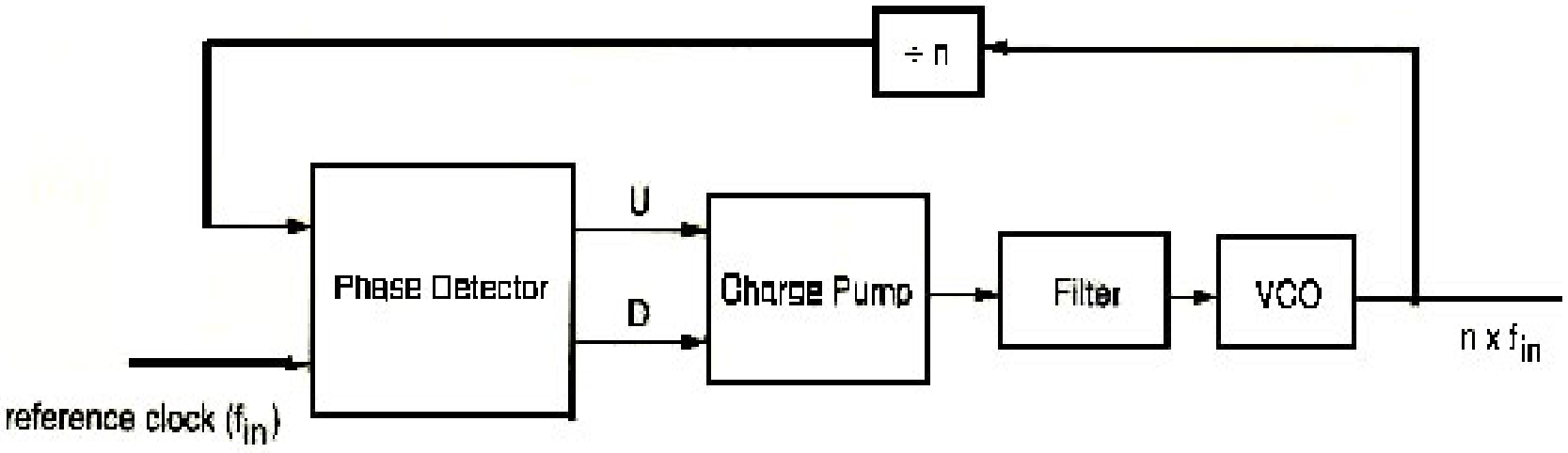
- In some designs, the output voltage of the sample-and-hold can show an overshoot at the moment the slew operation in amplifiers is finished and the signal level comes within the linear operation rate.
- This overshoot can be caused by a limited overall system stability introduced by a maximization of the bandwidth.

Phase Lock Loop

- **Used in two ways**
  - Demodulator-follow phase or frequency modulation
  - Track a carrier or synchronizing signal
- **Narrowband filters to recover signals**
- **Synchronizing digital transmissions in communications**
- **Frequency synthesizers,multipliers and dividers**

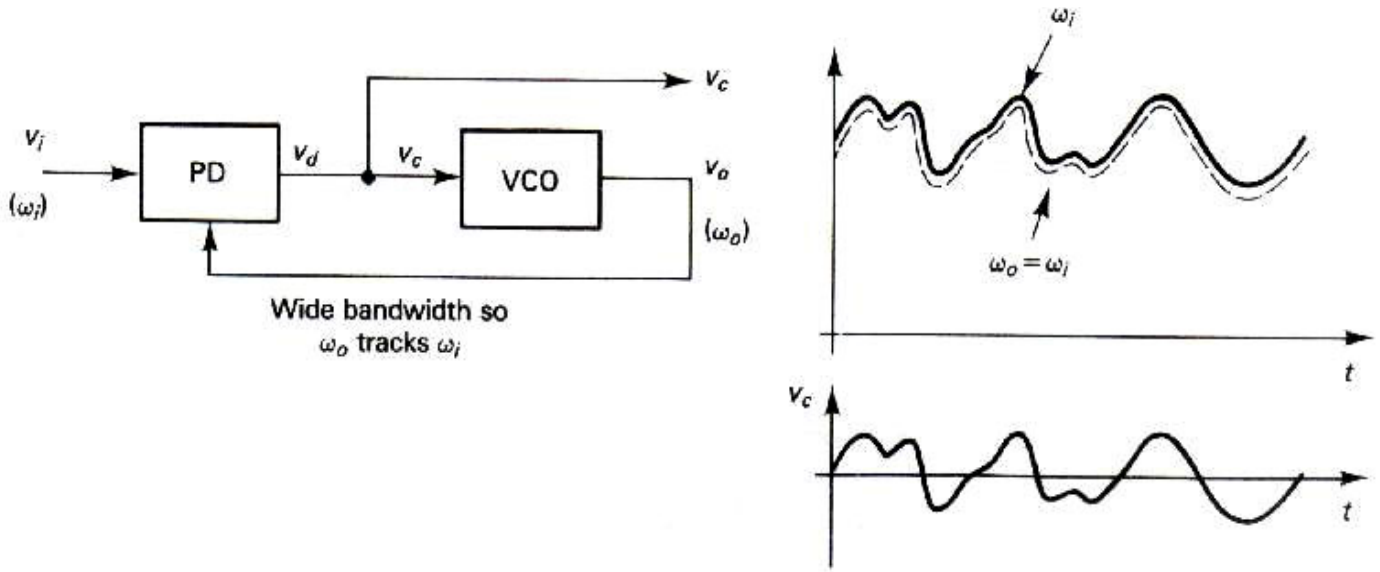
Phase lock loop

- **Structure :phase detector,charge pump, filter,VCO**



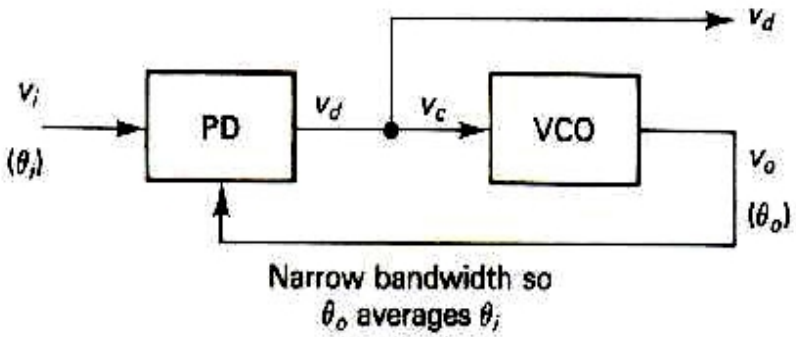
Demodulator(1)

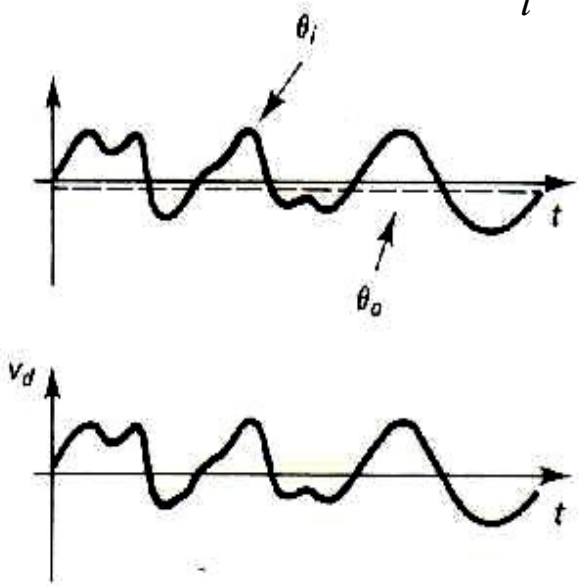
- **frequency demodulation :wo tracks the input frequency wi as it varies according to the modulation.**
- **Vc is proportional to wo,therefore,Vc is demodulated signal**



Demodulator(2)

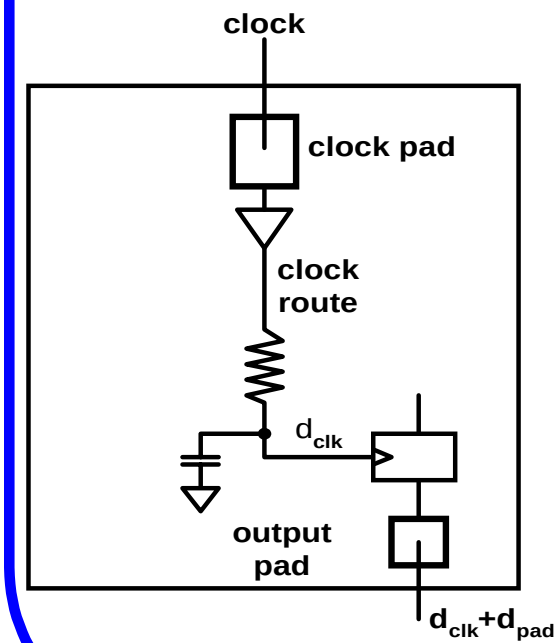
- Phase demodulation:
  - **In this application, θ_o sits at the average of θ_i**
  - **Vd is the demodulated output**

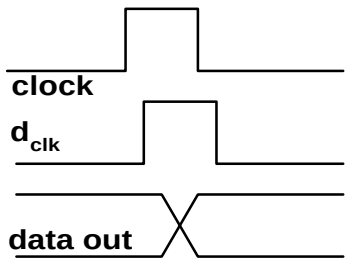


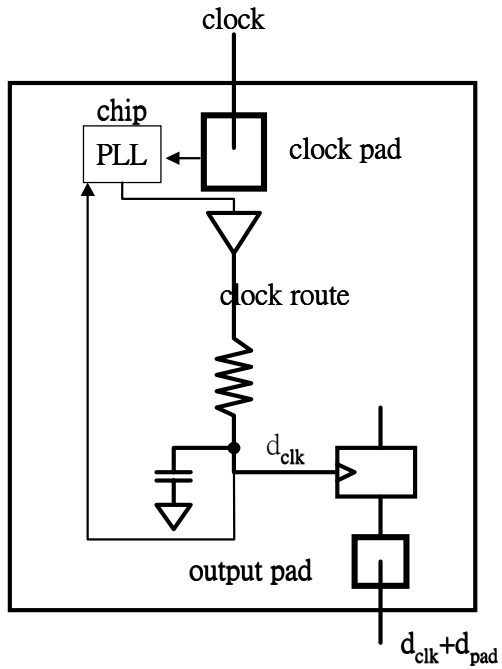


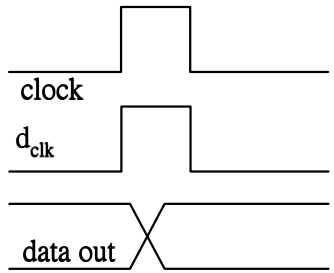
Track a carrier or synchronize signal

- Synchronize signal



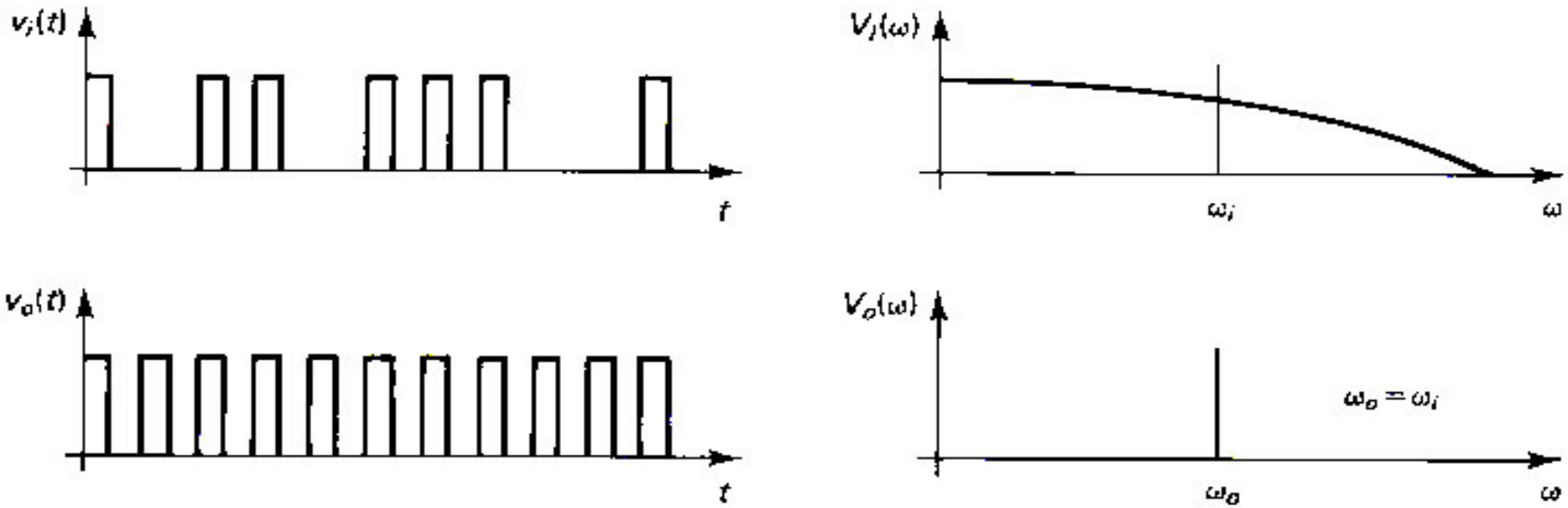






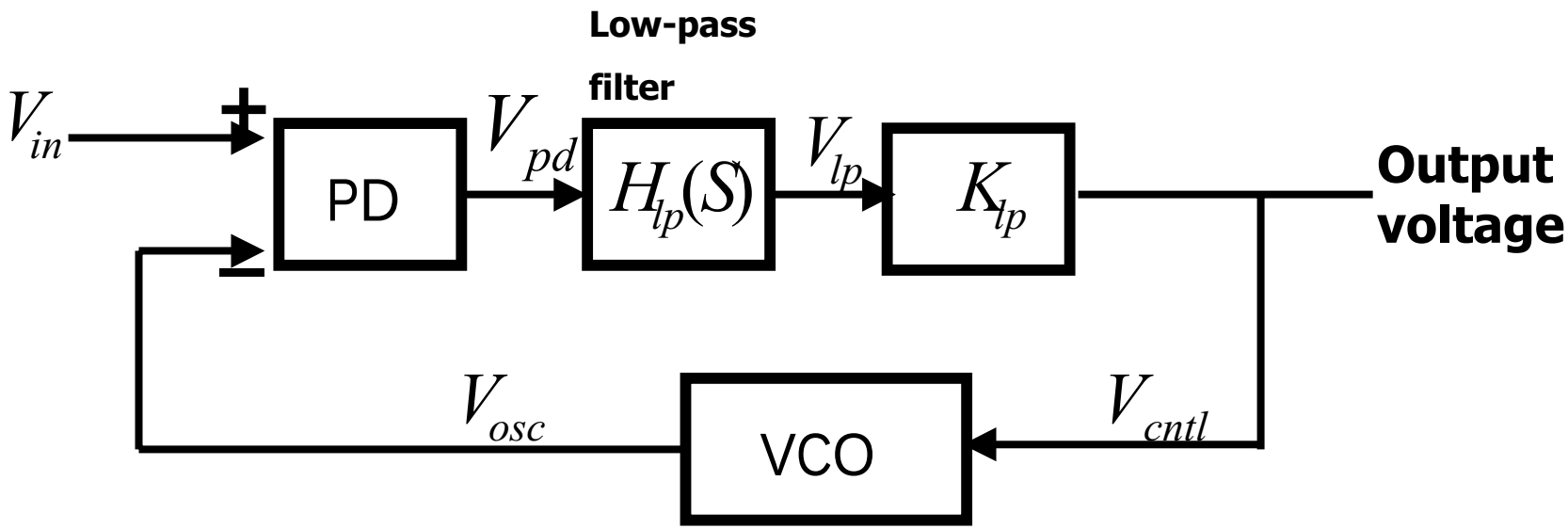
Narrowband filters to recover signals

- A clock signal vo is to be synchronized to a digital data signal vi
- The clock could have been recovered with a narrow-band filter



Narrowband filters to recover signals

- **The low-pass filter is first or second order**
- **The low-pass filter is to remove the second term at twice the frequency of the input signal**



Narrowband filters to recover signals

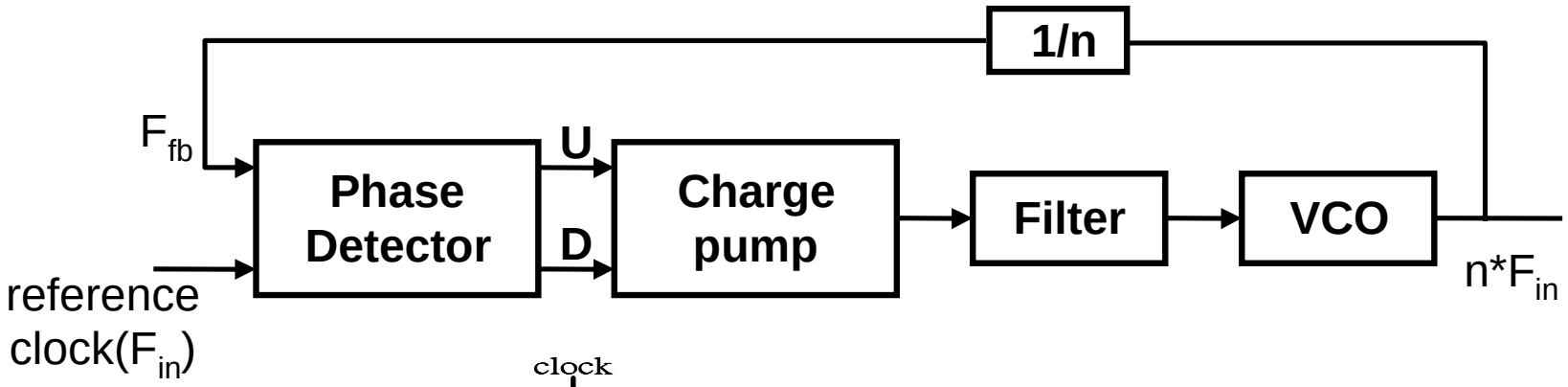
- **When the system is in lock($\Phi_d = 0$),the output of the filter is also equal to zero**
- **The increase in the low-pass filter's output will cause the VCO's frequency to increase until it is the same as that of the input signal ,which will keep the two signals in synchronism**

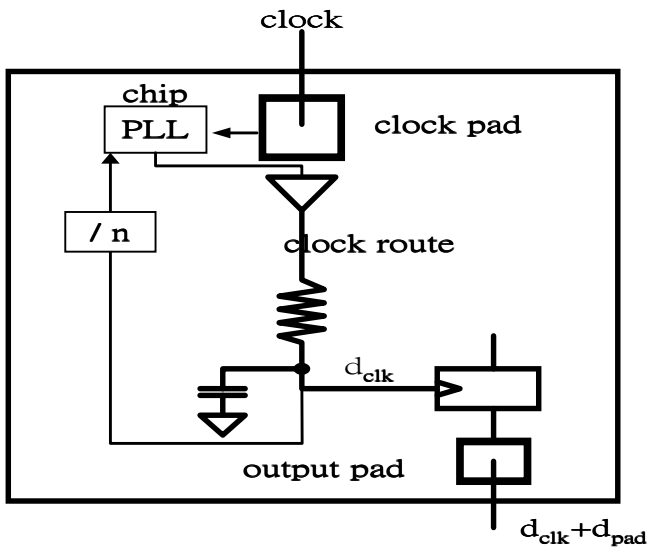
$$V_{pd} = K_M V_{in} V_{osc} = K_M E_{in} E_{osc} \sin(wt)\cos(wt - \Phi_d)$$

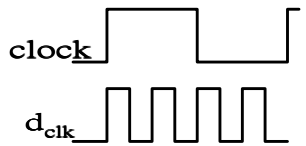
$$V_{pd} = K_M \frac{E_{in} E_{osc}}{2}[\sin(\Phi_d) + \sin(2wt - \Phi_d)]$$

$$V_{cntl} = K_{lp} K_M \frac{E_{in} E_{osc}}{2}\sin(\Phi_d)$$, V_{cntl} is the input to VCO

Frequency synthesizers, multipliers and dividers



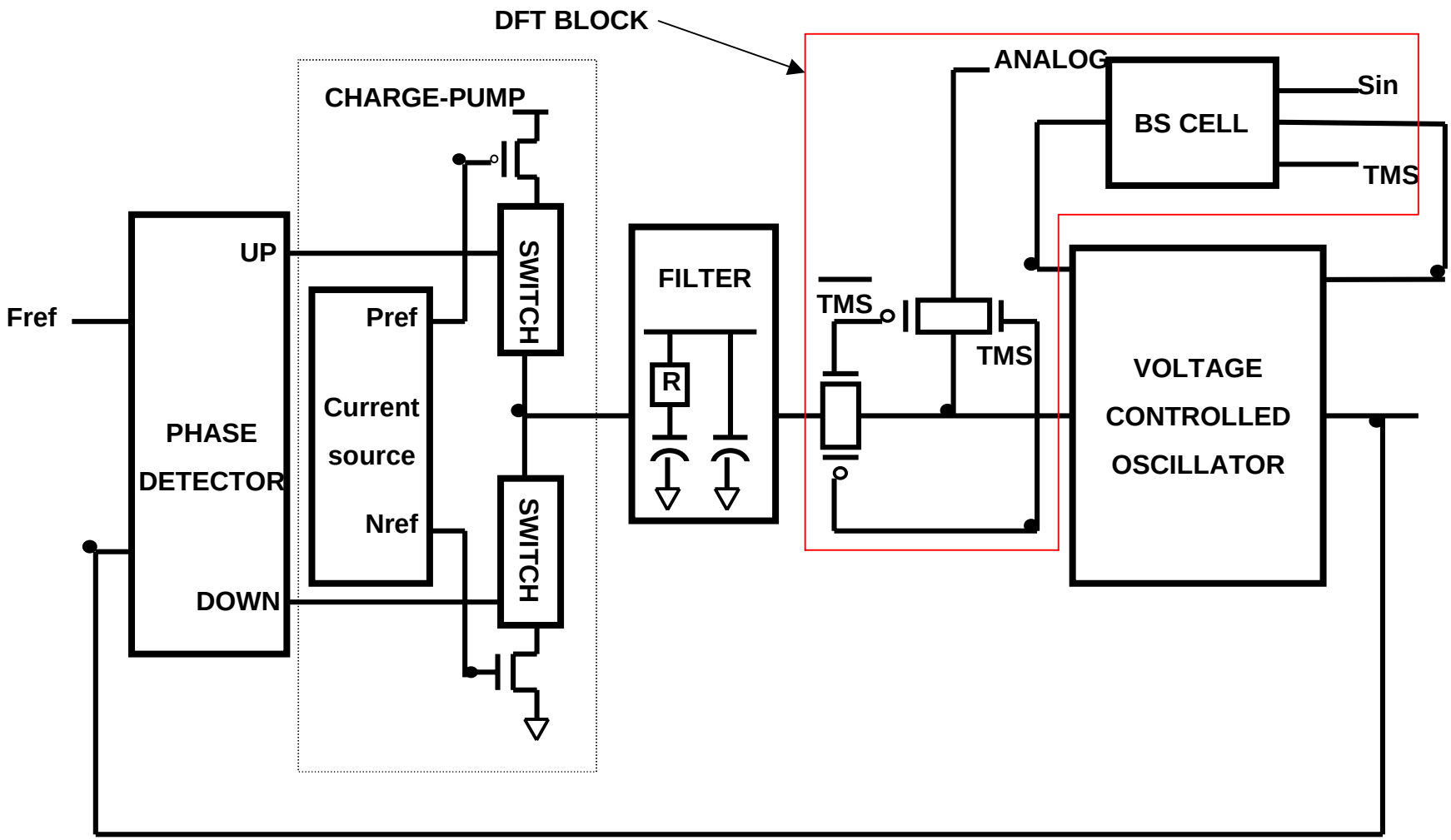




DFT for PLL using IEEE 1149.1

- A DFT strategy to test embedded Charge-Pump Phase Locked Loops in systems incorporating boundary scan
- DFT allows the verification of the operating frequency range of the CP-PLL while the system is in test mode
- This is achieved with a minimal degradation in PLL performance

Proposed DFT Circuit



Proposed Test Strategy

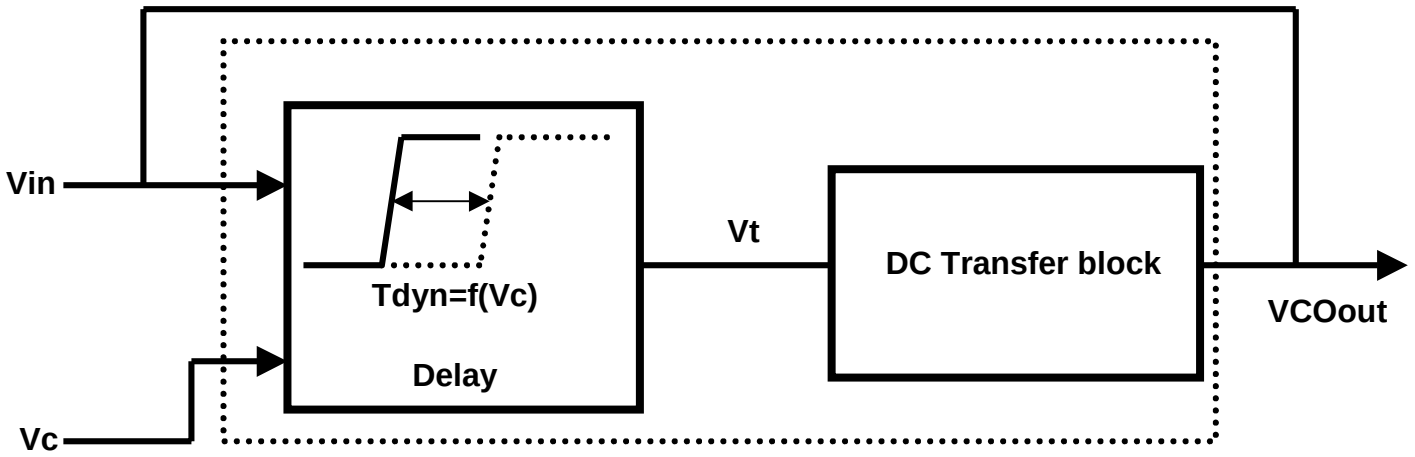
- By providing an additional test pin for an analog test signal, and by the use of an IEEE 1149.1 scan register to shift in voltage values and disable VCO feedback, we can characterize the VCO by sampling its dynamic delay
- This allows us to verify the operating frequency range of the PLL without performing any frequency measurements

Test Procedure

- 1. When system is in test mode: TMS is high
- 2. Set ANALOG to sweep Vc through in specific steps
- 3. Set Vc
- 4. Shift in voltage input to Vin through Sin line
- 5. Measure delay Tdyn at the output Fout of the PLL
- 6. Repeat steps 3, 4, 5, to sweep frequency range

VCO

- **It has a square wave frequency output VCOout which is a function of a varying input control voltage Vc**
- **The VCO can be treated as an open loop circuit with feedback provided externally**
- **The output frequency of VCO is** $f = \frac{1}{2(T_{dyn})}$



Parameters of PLL

- Capture range
- Tracking range
- Frequency settling time
- Frequency overshoot
- Frequency rise time
- Jitter

Capture range

- The maximum difference between the input signal’s frequency and the oscillator’s free-running frequency where lock can eventually be attained is defined as the capture range
- This frequency is on the order of the pole frequency of the low-pass filter

Tracking range(lock range)

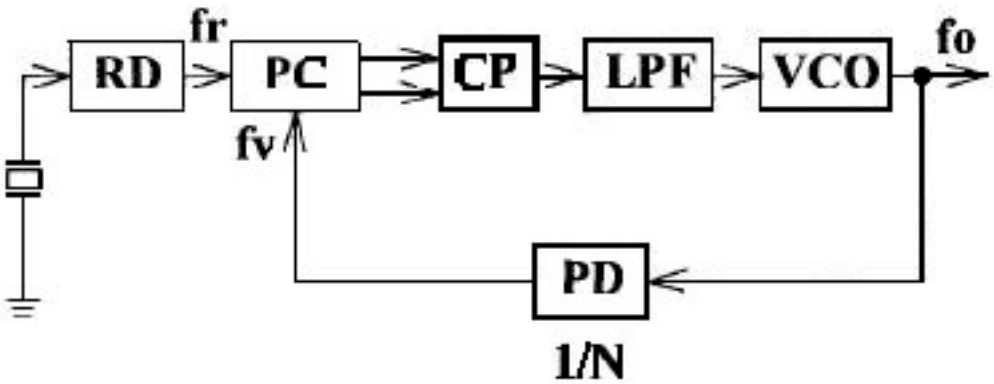
- **Once lock is attained,as long as the input signal's frequency changes only slowly it will remain in lock over a range that is much larger than the capture range**
- **This range is calculated as follows:**

$$V_{cntl-\max} = K_{lp}K_M \frac{E_{in}E_{osc}}{2} = K_{lp}K_{pd}$$

$$\omega_{lck} = \pm K_{osc}K_{lp}K_{pd}$$

- **The PLL will track the input signal as long as the frequency of the input signal does not exceed this range**

Frequency settling time(1)



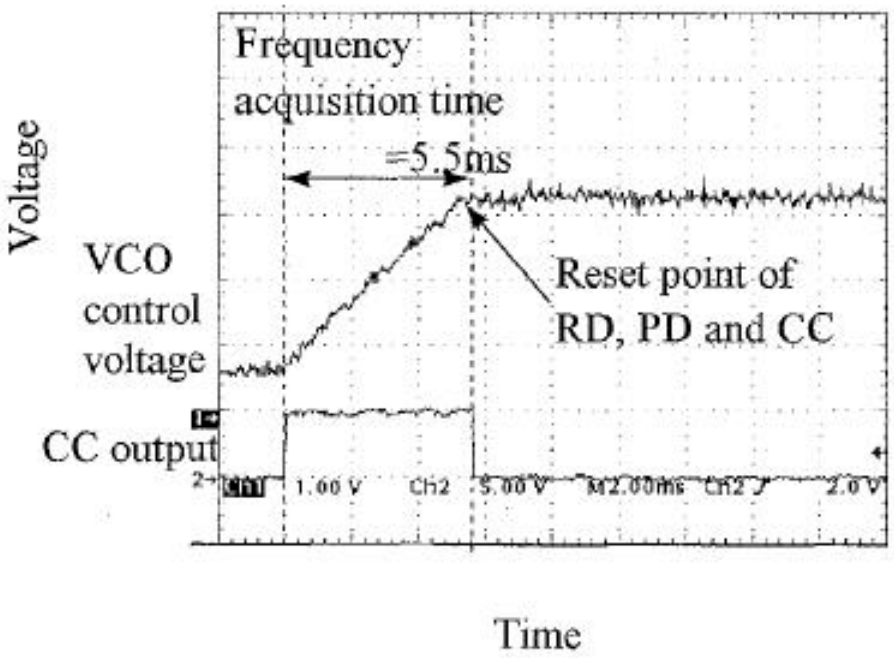
VCO:Voltage Controlled Oscillator PD : Programmable Divider

RD : Reference Divider PC : Phase Comparator

CP : Charge Pump LPF : Low Pass Filter

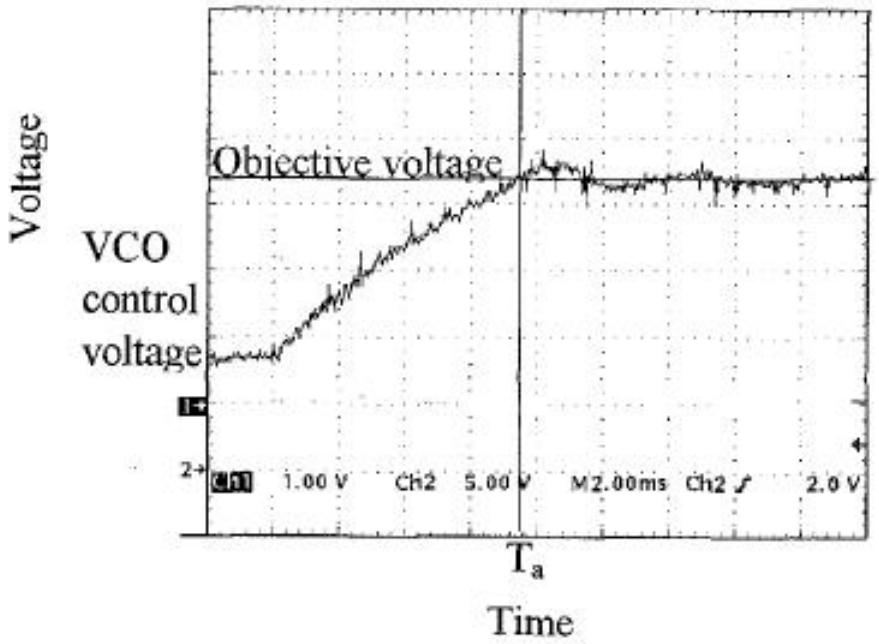
- When PD change ratio
- The output frequency will change to a target frequency
- The output voltage of VCO output frequency rises toward to objective value

Frequency settling time(2)



- **Frequency acquisition time is the Frequency settling time**

Frequency overshoot



- **Frequency overshoot is shown in the left figure**
- **Frequency rise time is the 10%~90% of settling time**

Jitter(sampling time uncertainty)

- To quantify this sampling time uncertainty as known as aperture jitter

$$V_{in} = \frac{V_{ref}}{2}\sin(2\Pi f_{in} t)$$

$$\left.\frac{\Delta V}{\Delta t}\right|_{\max} = \Pi f_{in} V_{ref}$$

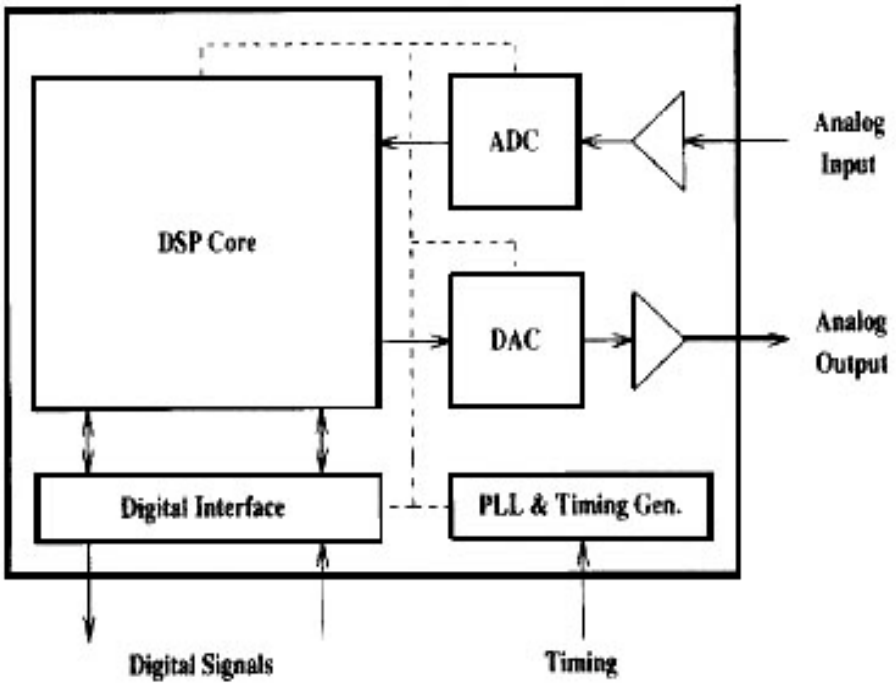
$$\Delta t < \frac{V_{LSB}}{\Pi f_{in} V_{ref}} = \frac{1}{2^N \Pi f_{in}}$$

- **An 8-bit full-scale 250MHz converter, it's sampling time uncertainty under 5ps**

Digital signal processing

- Low cost test solution
- Flexible
- Simplified instrument set
- Simplified command set
- Advanced CPU/DSP cores
- Domain transformation
- Statistic method

DSP based testing



AWG(Arbitrary Waveform Generators) is basically a DAC

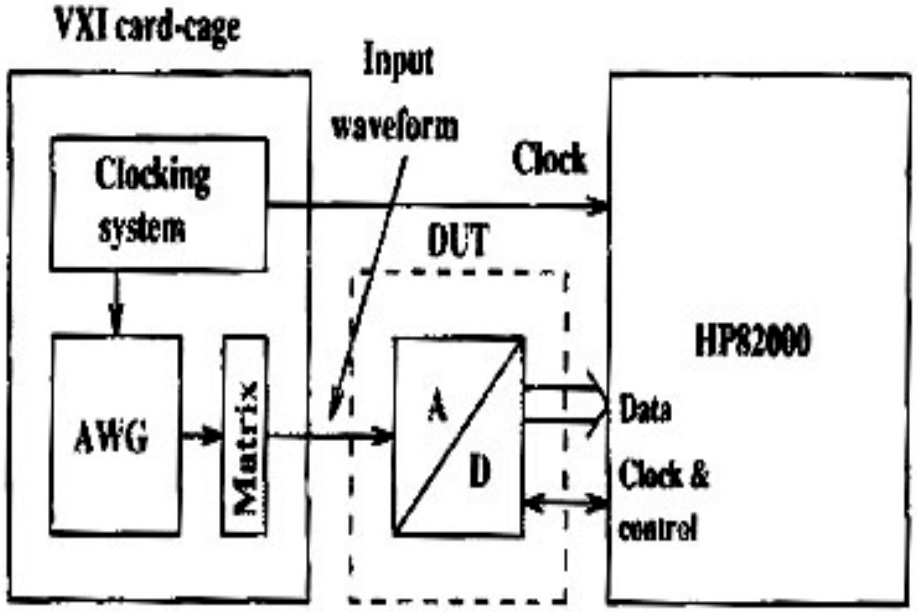
Waveform digitizer is a ADC

It can used in many purpose: spectrum analysis,scope viewing , voltage measurement etc.

It is a low cost solution compared to ATE and a more flexible design

It needs pre/post-processing circuit, so speed is reduced-undersampling the signal and signal compression is needed

DSP based testing(example)



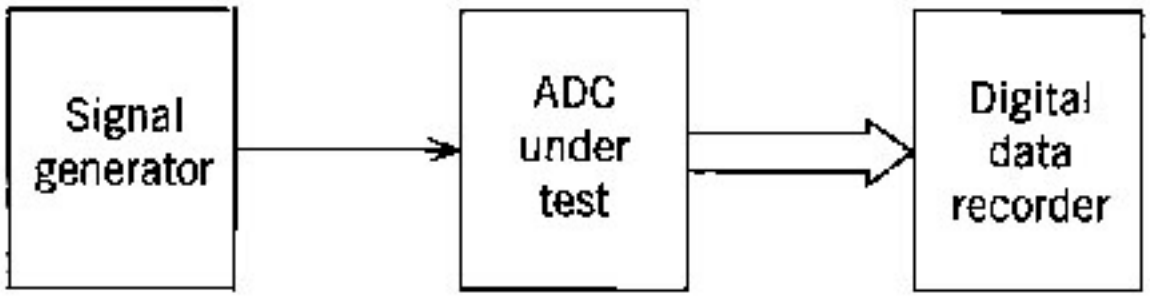
- VXI card-cage generate phase-lock clocking to AWG and HP82000 (good central clocking)
- HP82000 provides all of the timing and control signals for the ADC
- AWG provides a sine-wave for the analog input of the ADC

DSP methods

- **Histogram**
  - Gain,offset,INL,DNL
- **Fourier transform**
  - SNR,SNR+D,peak harmonic,total harmonic, coherence, non-coherence
- **Time-frequency domain(modulation)**
  - Capture &tracking range
  - Frequency rise , fall , overshoot , settling time , jitter

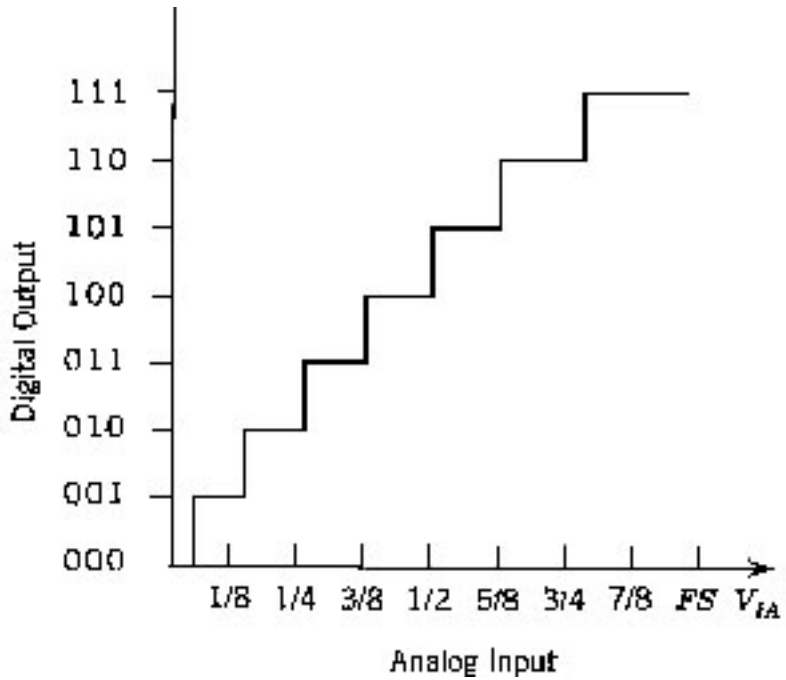
Histogram methods(1)

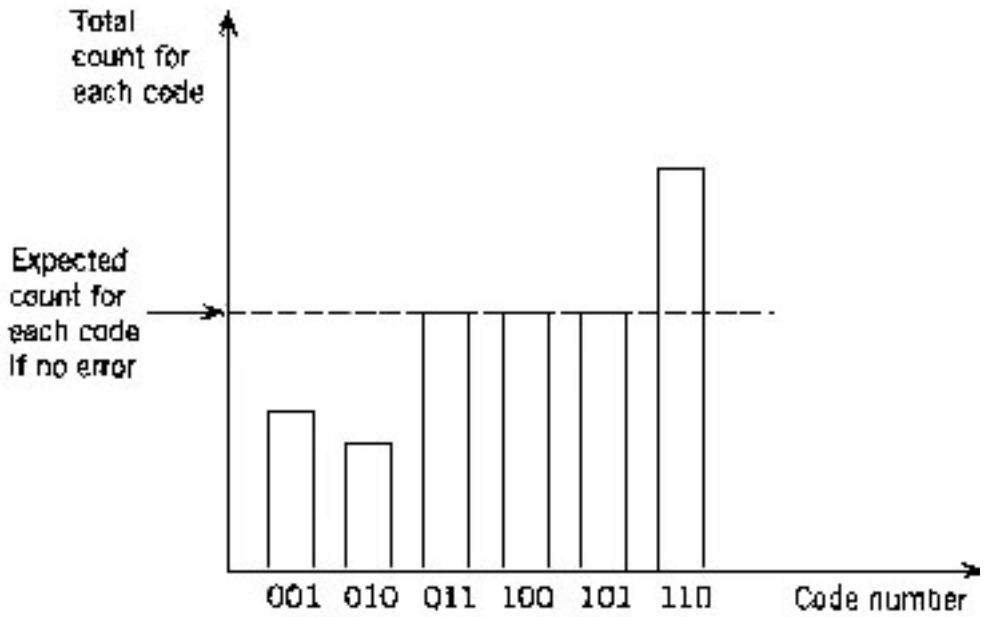
- The signal generator is not externally controlled
- Digital data recorder:analyze the data and calculate device errors



Histogram methods(2)

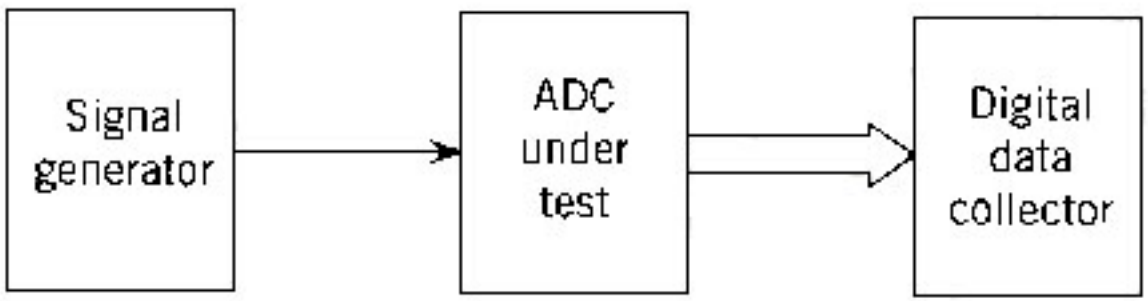
- Resulting tally count of a converter with linearity errors





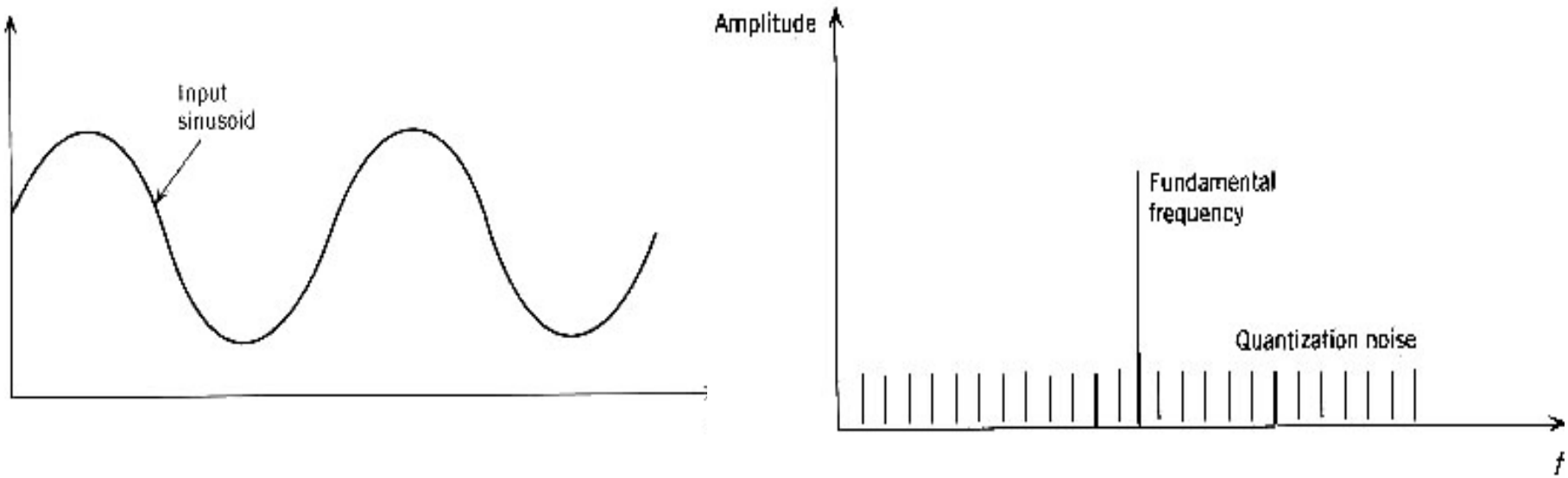
Fourier transform(FFT testing)

- Similar to histogram test method
- Many of the concerns for the histogram test are also converters for FFT testing



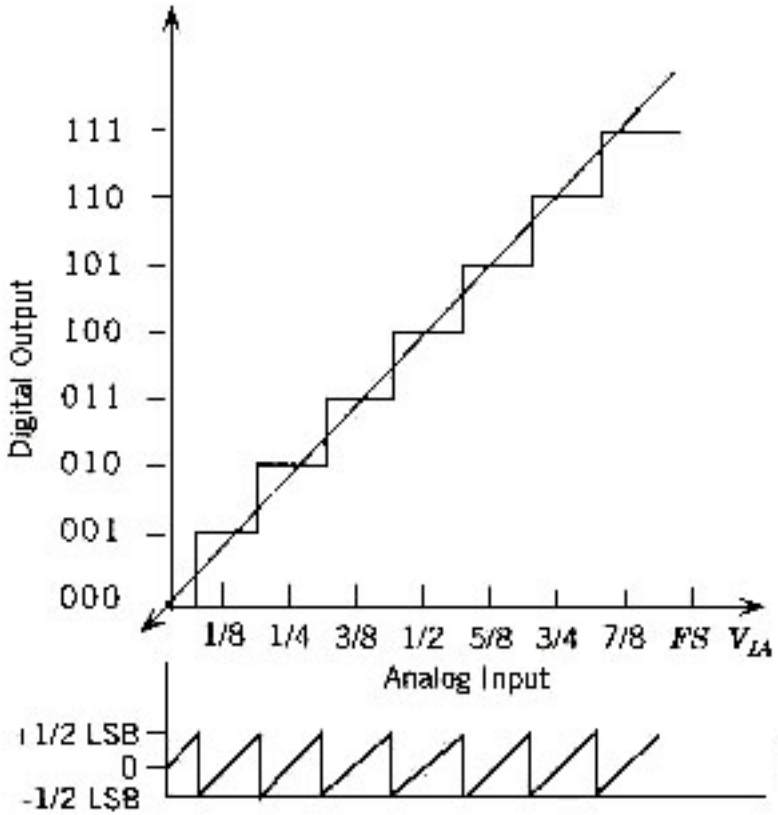
Fourier transform(2)

- Result of transforming a pure sine wave with an ideal converter

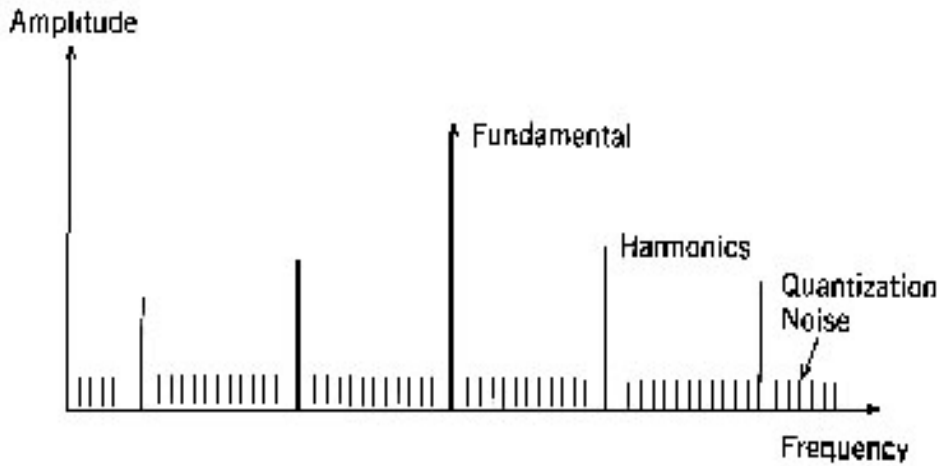


Fourier transform(3)

- **Illustration of quantization noise**



- **Results of transforming a pure sine wave with a converter with nonlinearity**



Testable design approaches

- Design for test
- BIST
- Algorithmic

Design for test

- Controllability/ Observability
- Isolation
- Sample/ hold
- COS (Control and Observation Structure)
- Analog Scan
- IEEE 1149.4

Cotrollability/Observability

- **Controllability**

  The ability to apply a specific signal value to each node in a circuit by setting values on the circuit inputs.

- **Observability**

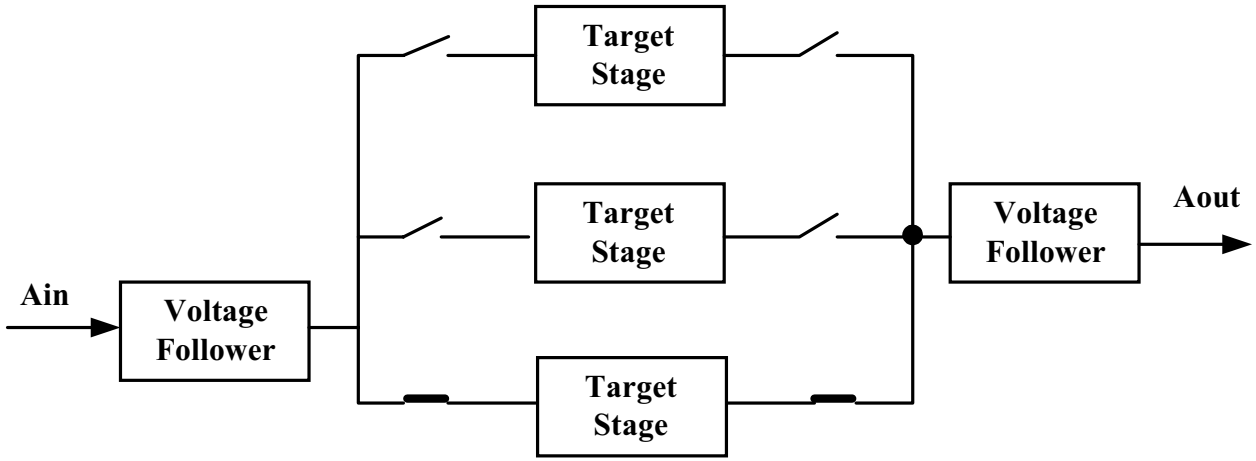
  The ability to determine the signal value at any node in a circuit by controlling the circuit's inputs and observing its outputs .

Isolation/Sampling

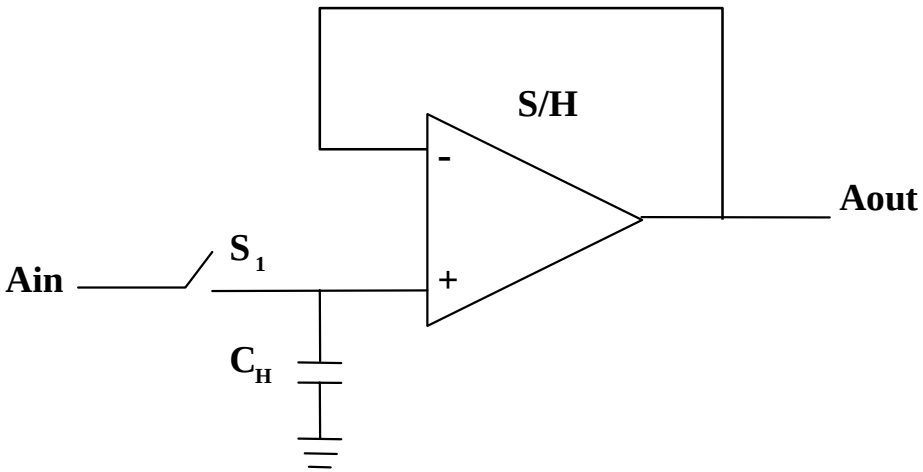
- For complex of mixed-signal devices, the functional blocks can be isolated for testability.
- In analog circuit, capacitors form the memory cell.

  The values of the signal can be sampled and held.

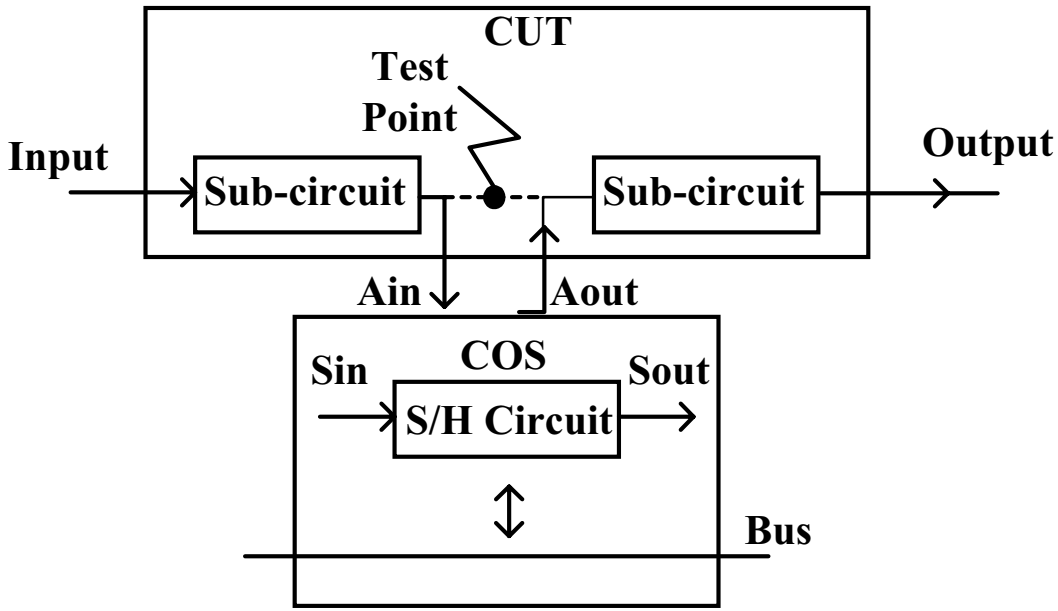
Isolation


Target
Stage
Target
Stage
Target
Stage
Ain
Voltage
Follower
Voltage
Follower
Aout

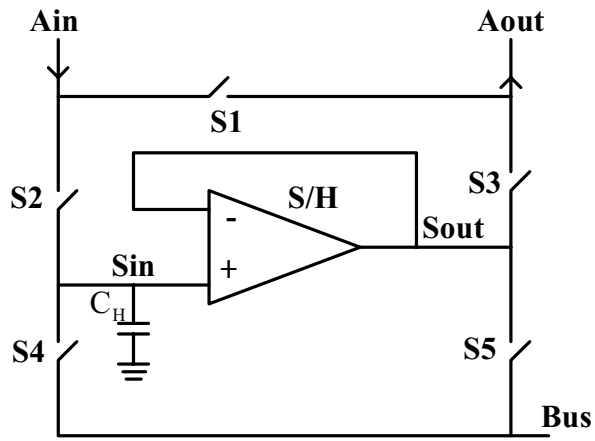
Sample/Hold



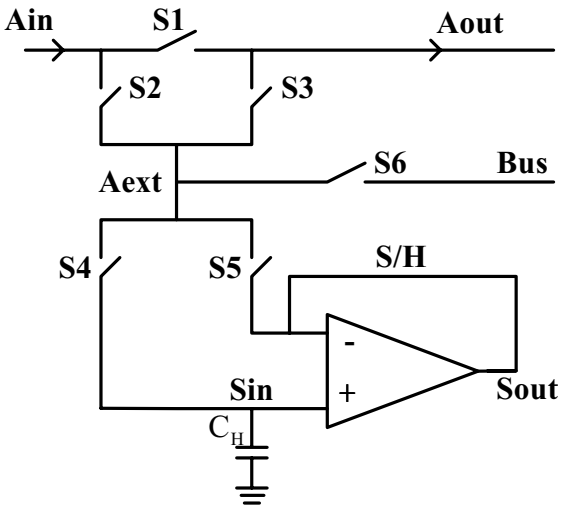
Control and Observation Structure (COS)



Examples of COSs

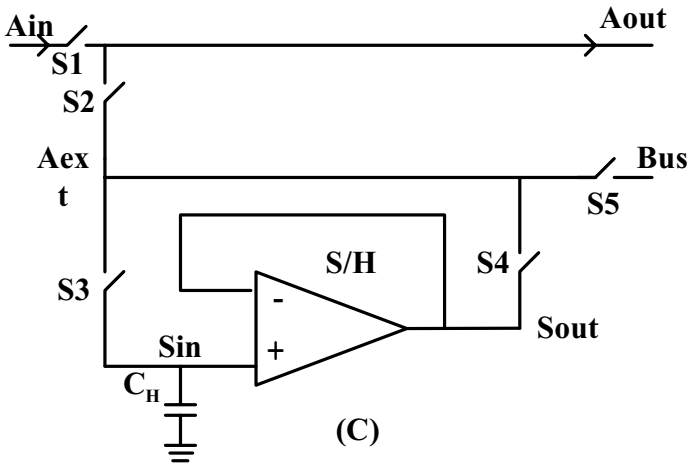


(a)

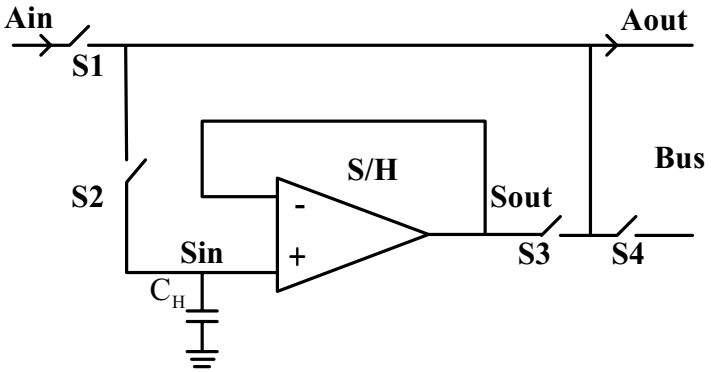


(b)

Examples of COSs



(C)



(d)

Operations of COSs

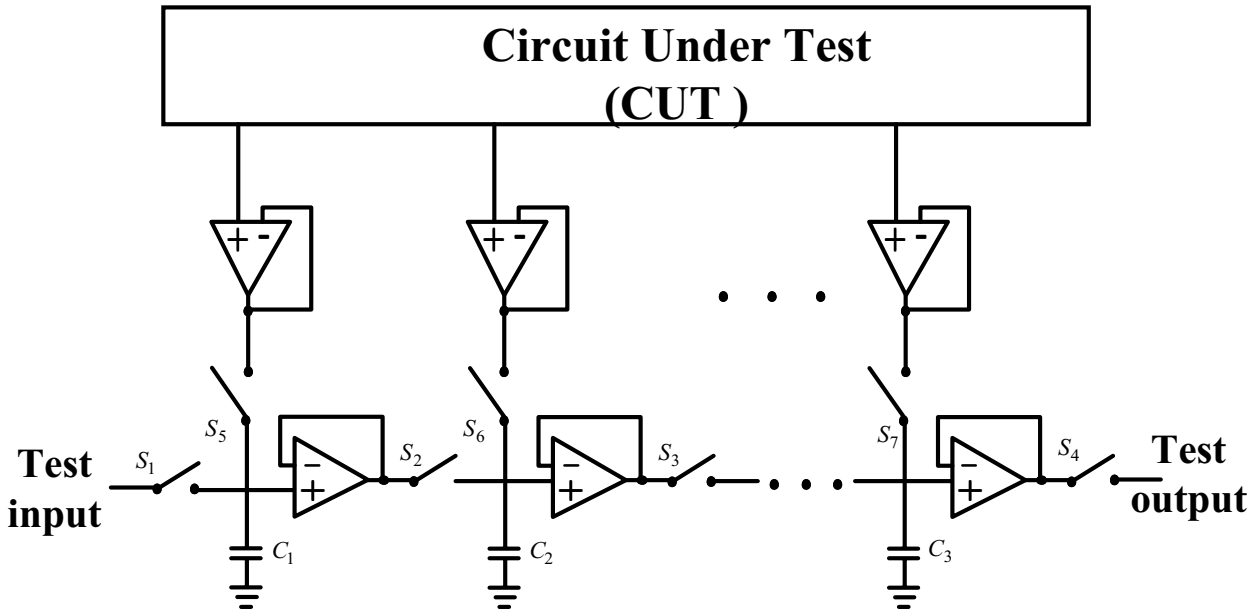
No.	Data path	Operation	Function
1	Ain→Aout	Normal	Normal operation mode
2	Ain→Bus	Monitor	AC signal observation
3	Bus→Aout	Control	AC signal application
4	Ain→Sin	Sample	DC signal observation
5	Sout→Bus	Scan-out	
6	Sout→Aout	Apply	DC signal application
7	Bus→Sin	Scan-in	

No.	Operation (Concurrent)
8	ConSample(Normal, Sample)
9	ConMonitor(Normal, Monitor)
10	ConScan-in(Normal, Scan-in)
11	ConScan-out(Normal, Scan-out)
12	ConApSout(Apply, Scan-out)
13	ConCntSin(Control, Scan-in)
14	ConSamMon(Sample, Monitor)

Scan-in/Scan-out

- A chain of capacitors and voltage-follower buffers form an analog shift register.
- The test input signal can be scanned in from input pins to the internal nodes and the test results can be scanned out from the internal nodes to output pins.

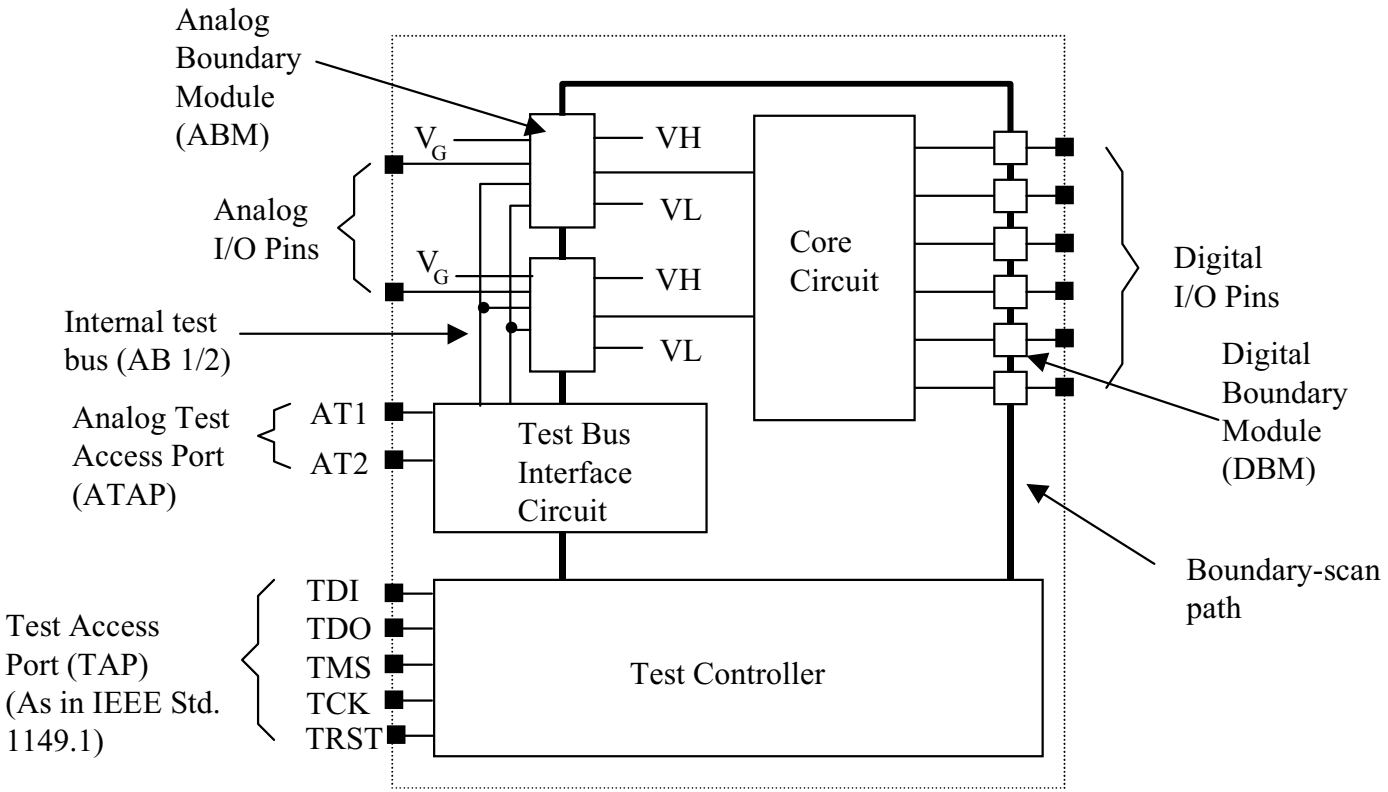
Scan-out


Circuit Under Test
(CUT)
Test
input
Test
output
S_1
S_2
S_3
S_4
S_5
S_6
S_7
C_1
C_2
C_3

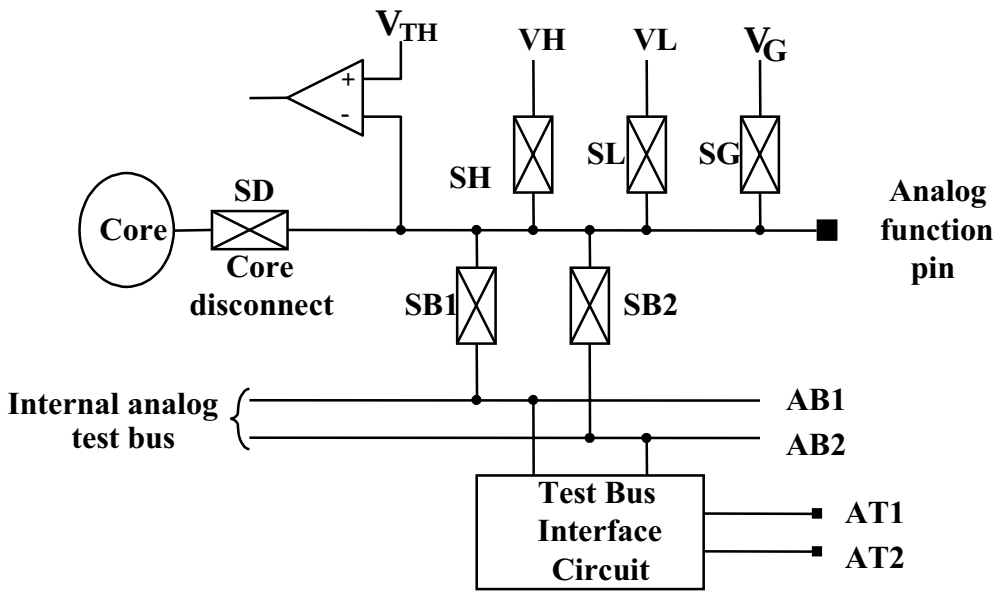
IEEE std. 1149.4

- Providing a mechanism for interconnect testing of a board with analog, digital , and mixed-signal chips.
- IC test either in isolated or in surface mounted.

Structure of an 1149.4 chip



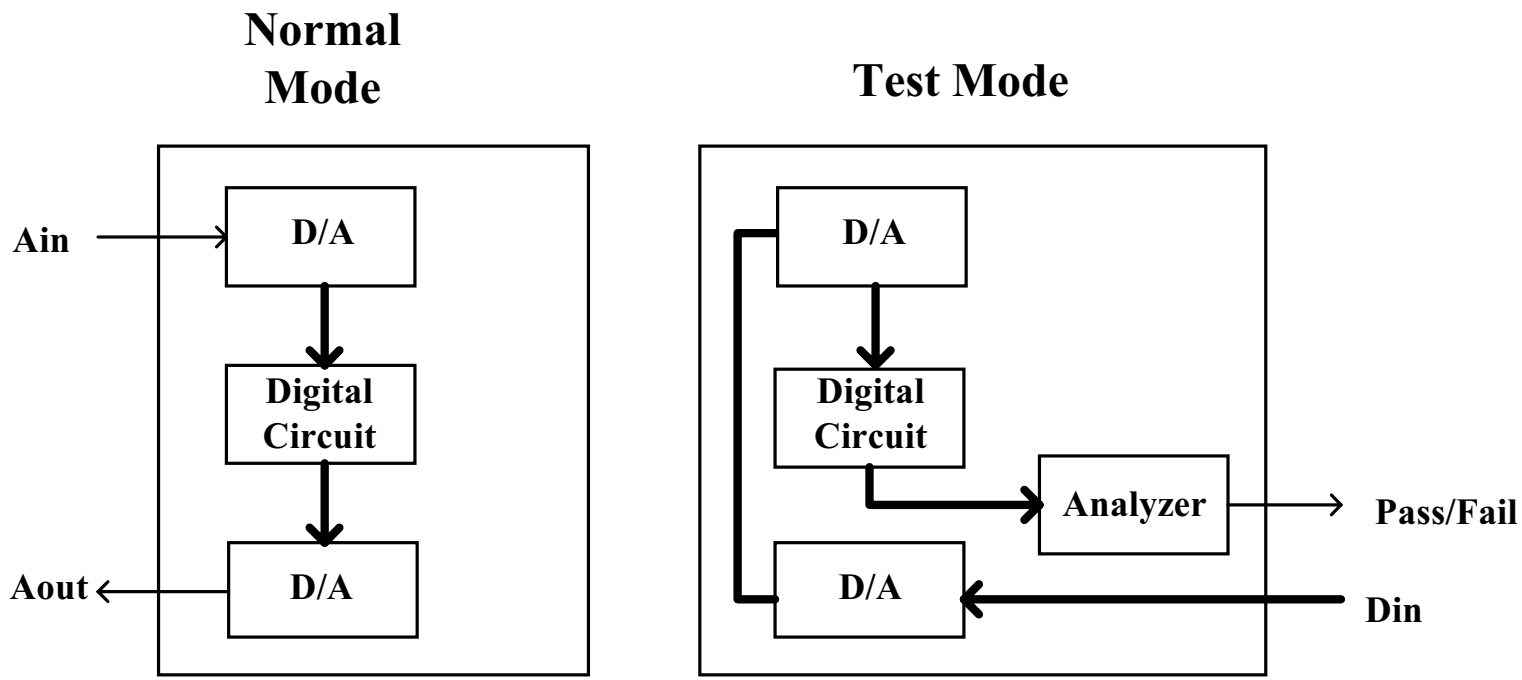
Test Bus Interface Circuit



BIST

- A/D & D/A pairs
- Oscillation-loop based
- On chip stimuli generation
- Output analysis

A/D & D/A Pairs


Normal Mode
Ain
D/A
Digital Circuit
D/A
Aout
Test Mode
D/A
Digital Circuit
Analyzer
Pass/Fail
D/A
Din

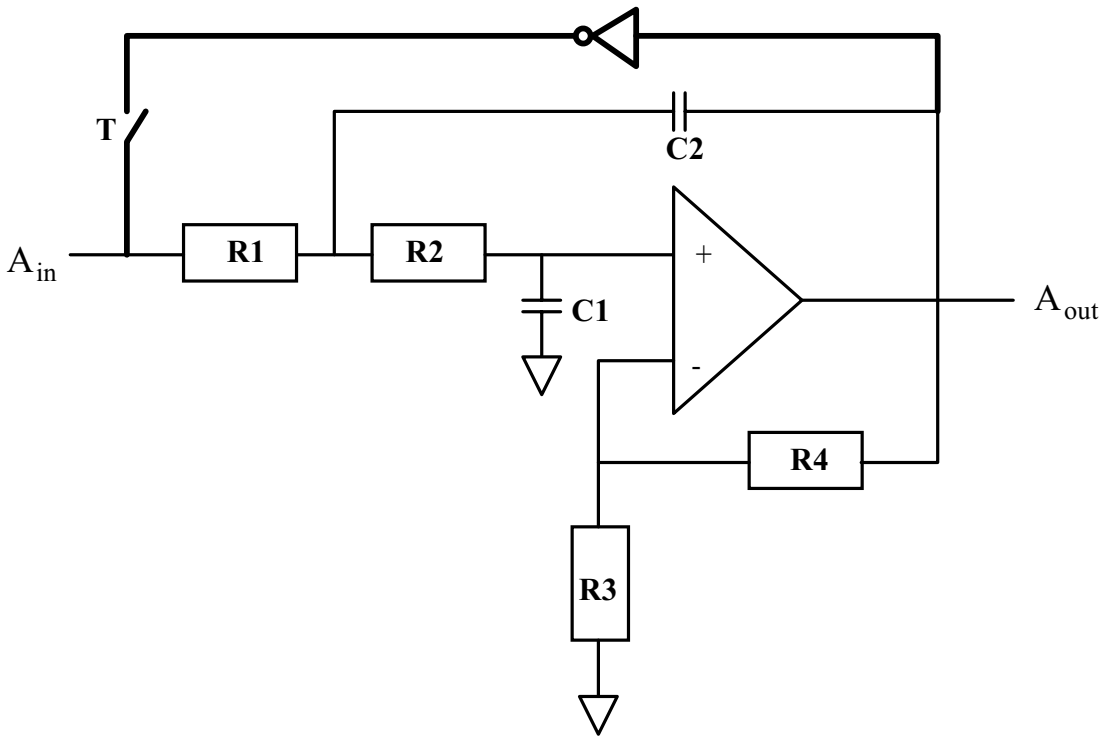
Requirements

- Only for specific circuit including A/D and D/A converters
- DAC resolution must be higher than that of ADC (usually ≥ 2 bits)

Oscillation-loop Based for OP amp.

- A fault in the circuit will either prevent the circuit from oscillating or alter the oscillation frequency.
- Feedback circuitry is added to the CUT in test mode such that the resulting circuit is an oscillator.
- The oscillation frequency is determined by circuit parameters such as the gain of the op amp and unity gain frequency.

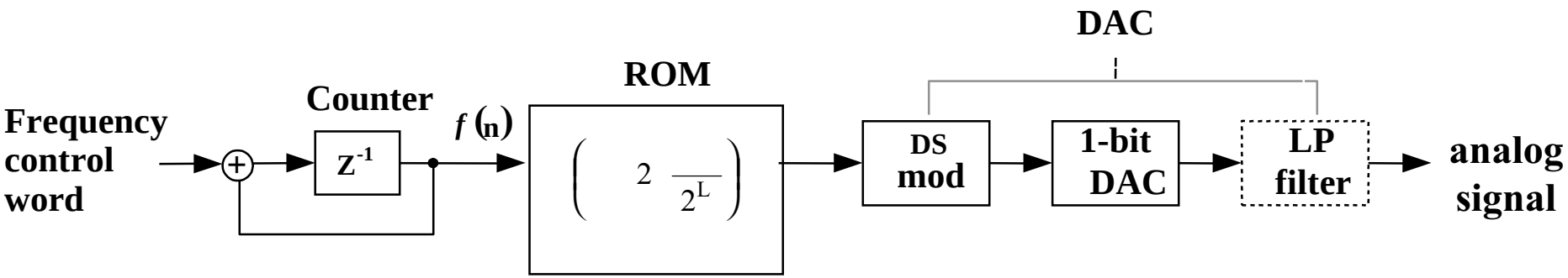
Oscillation-based Test



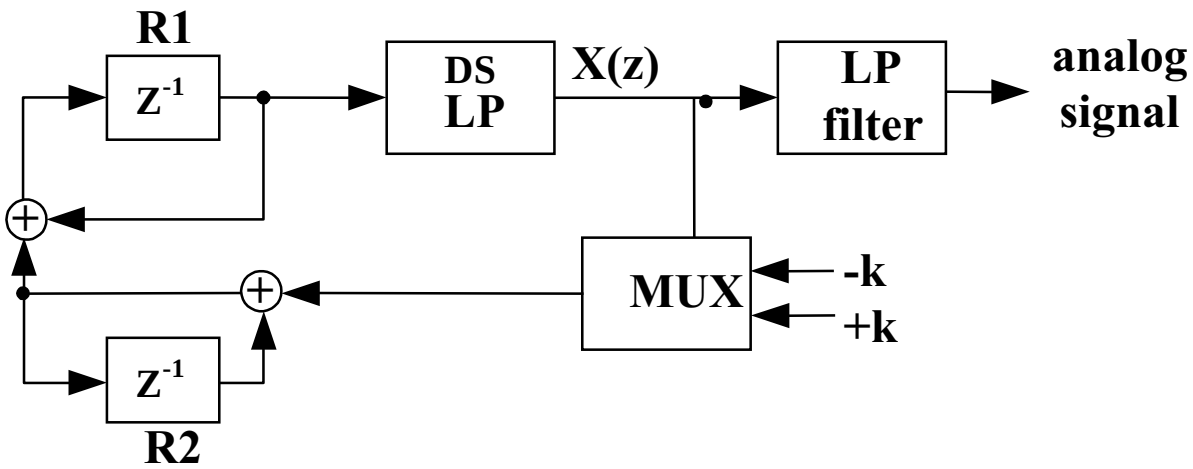
On Chip Stimuli Generation

- Digital frequency Synthesis
- Delta-Sigma Oscillators
- Fixed-length periodic bit stream

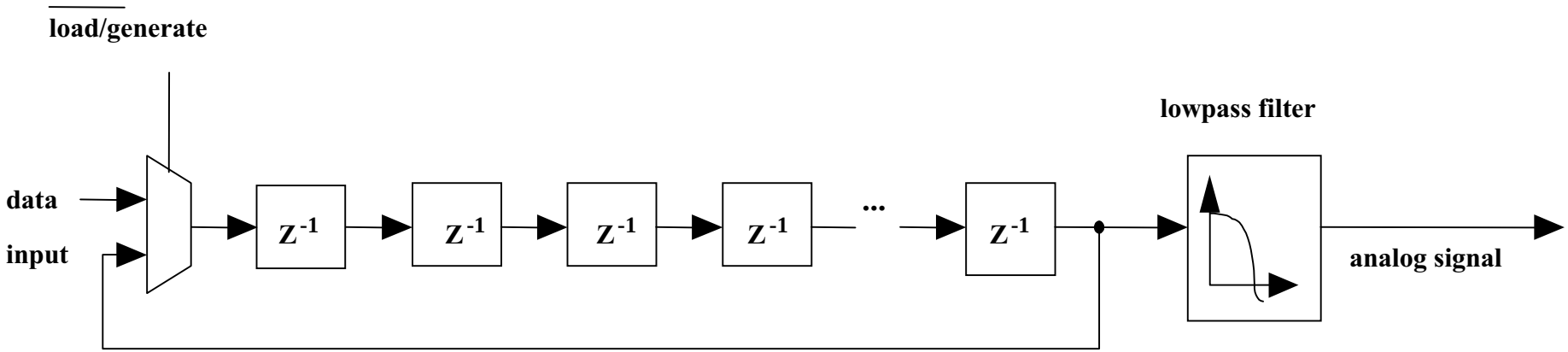
Digital frequency Synthesis



Delta-Sigma Oscillators



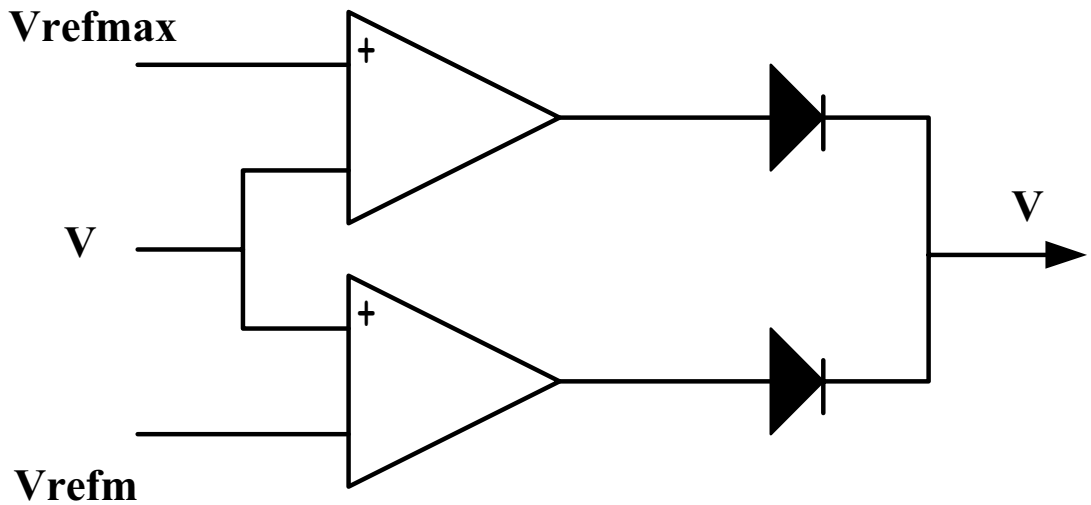
Fixed-length periodic bit stream



Output Analysis

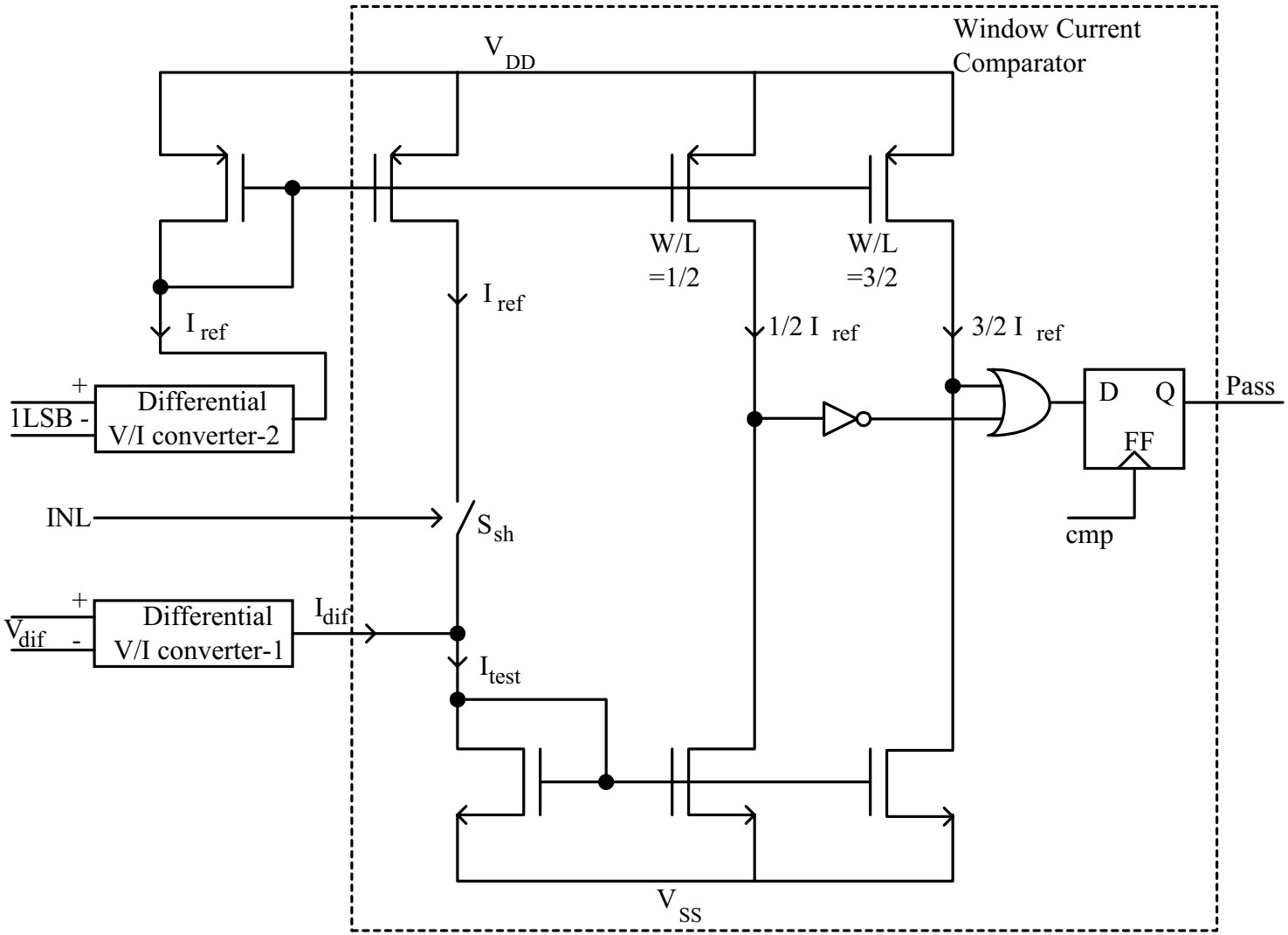
- **Voltage/Current Comparator**
- **Frequency Counter**

Voltage Comparator

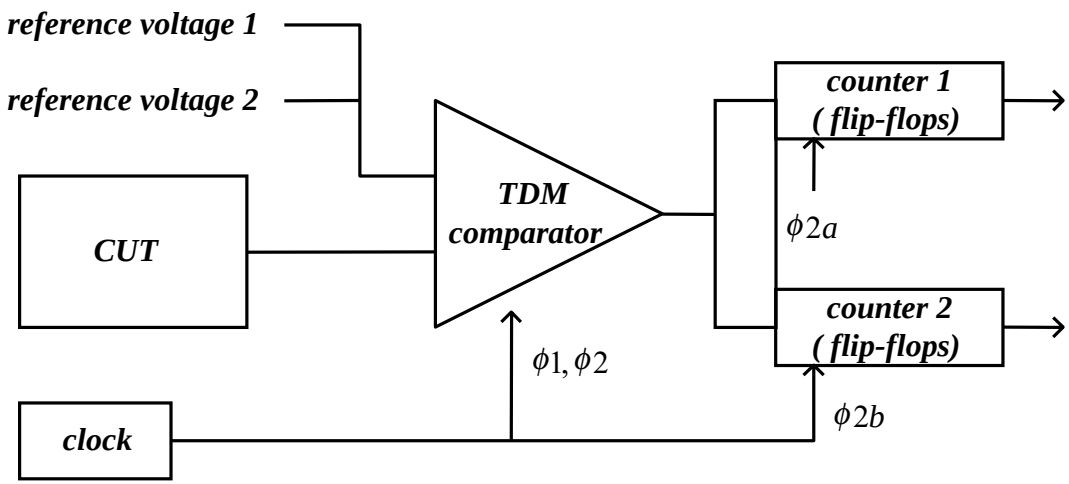


Vaemarar

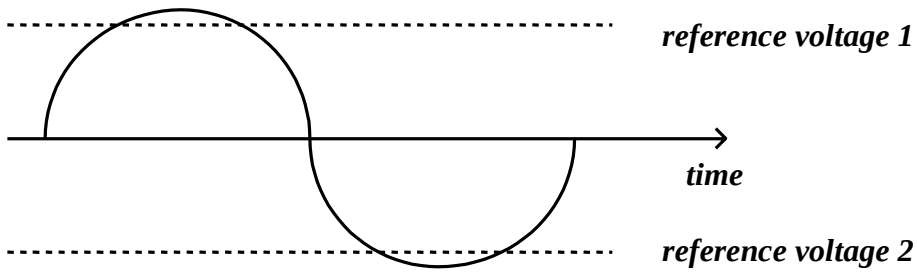
Current Comparator



Frequency Counter



Proposed BIST scheme



Example of reference voltages

Algorithmic method

- Based on the state equations of a system
- Using the check-sum method
- Capable of testing, diagnosis, and error correction
- Apply to various technologies

State Equation of a Linear System

$$\begin{bmatrix} s) \\ {}_{2}\, s) \\ \cdot \\ \cdot \\ \cdot \\ {}_{n}\, s) \end{bmatrix} = \begin{bmatrix} & {}_{2} & \cdot & \cdot & \cdot & {}_{n} \\ {}_{2} & {}_{22} & \cdot & \cdot & \cdot & {}_{2n} \\ \cdot & \cdot & \cdot & & & \cdot \\ \cdot & \cdot & & \cdot & & \cdot \\ \cdot & \cdot & & & \cdot & \cdot \\ {}_{n} & {}_{n2} & \cdot & \cdot & \cdot & {}_{nn} \end{bmatrix} \begin{bmatrix} \frac{s)}{s} \\ \frac{{}_{2}\, s)}{s} \\ \cdot \\ \cdot \\ \cdot \\ \frac{{}_{n}\, s)}{s} \end{bmatrix} + \begin{bmatrix} 2 \\ \cdot \\ \cdot \\ \cdot \\ {}_{n} \end{bmatrix} \frac{\mu\ s)}{s}$$

or $s = \cdot\ s\ /s + \cdot \mu\ s\ /s$

Check-sum Method

- Many analog circuits can be expressed as a state-variable system
- Changes in the state can be computed using matrix-vector multiplications.
- Multiple checksum vector can be used to increase the error detection capability , and/or for error correction.

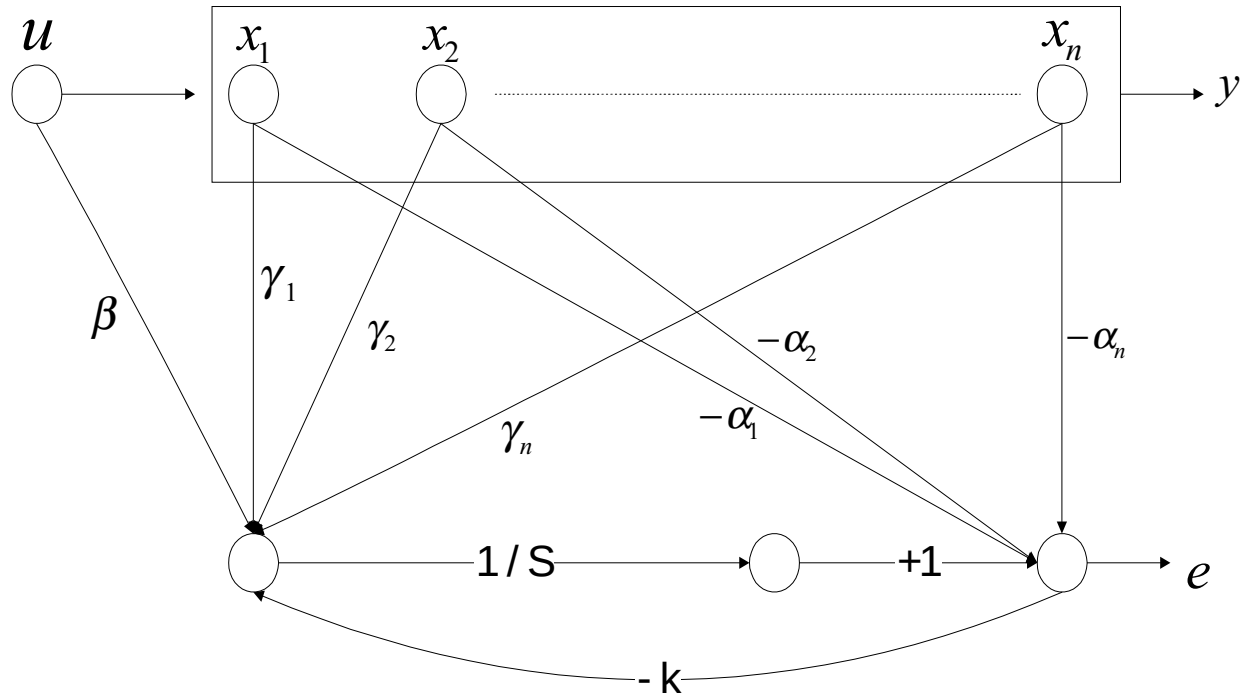
Expanded State Equation

Add one state variable

$$\begin{bmatrix} x(s) \\ x_2(s) \\ \cdot \\ \cdot \\ \cdot \\ x_n(s) \\ x_{n+}(s) \end{bmatrix} = \begin{bmatrix} a & a_2 & \cdot & \cdot & \cdot & a_n & 0 \\ a_2 & a_{22} & \cdot & \cdot & \cdot & a_{2n} & 0 \\ \cdot & \cdot & \cdot & & & \cdot & \cdot \\ \cdot & \cdot & & \cdot & & \cdot & \cdot \\ \cdot & \cdot & & & \cdot & \cdot & \cdot \\ a_n & a_{n2} & \cdot & \cdot & \cdot & a_{nn} & 0 \\ \gamma & \gamma_2 & \cdot & \cdot & \cdot & \gamma_n & 0 \end{bmatrix} \begin{bmatrix} \frac{x(s)}{s} \\ \frac{x_2(s)}{s} \\ \cdot \\ \cdot \\ \cdot \\ \frac{x_n(s)}{s} \\ \frac{x_{n+}(s)}{s} \end{bmatrix} + \begin{bmatrix} b \\ b_2 \\ \cdot \\ \cdot \\ \cdot \\ b_n \\ \beta \end{bmatrix} \frac{\mu(s)}{s}$$

where $\begin{bmatrix} \gamma & \gamma_2 & \cdot & \cdot & \cdot & \gamma_n \end{bmatrix} = \begin{bmatrix} \alpha & \alpha_2 & \cdot & \cdot & \cdot & \alpha_n \end{bmatrix} \bullet A$

Signal Flow Graph of a Current Detection Scheme



$e = \sum_{i=1}^{n} \alpha_i x_i \;\; s \;\; - \sum_{i=1}^{n} r_i \frac{x_i \;\; s}{s} + \beta \frac{u \;\; s}{s} = 0$ must hold if no faults exist.

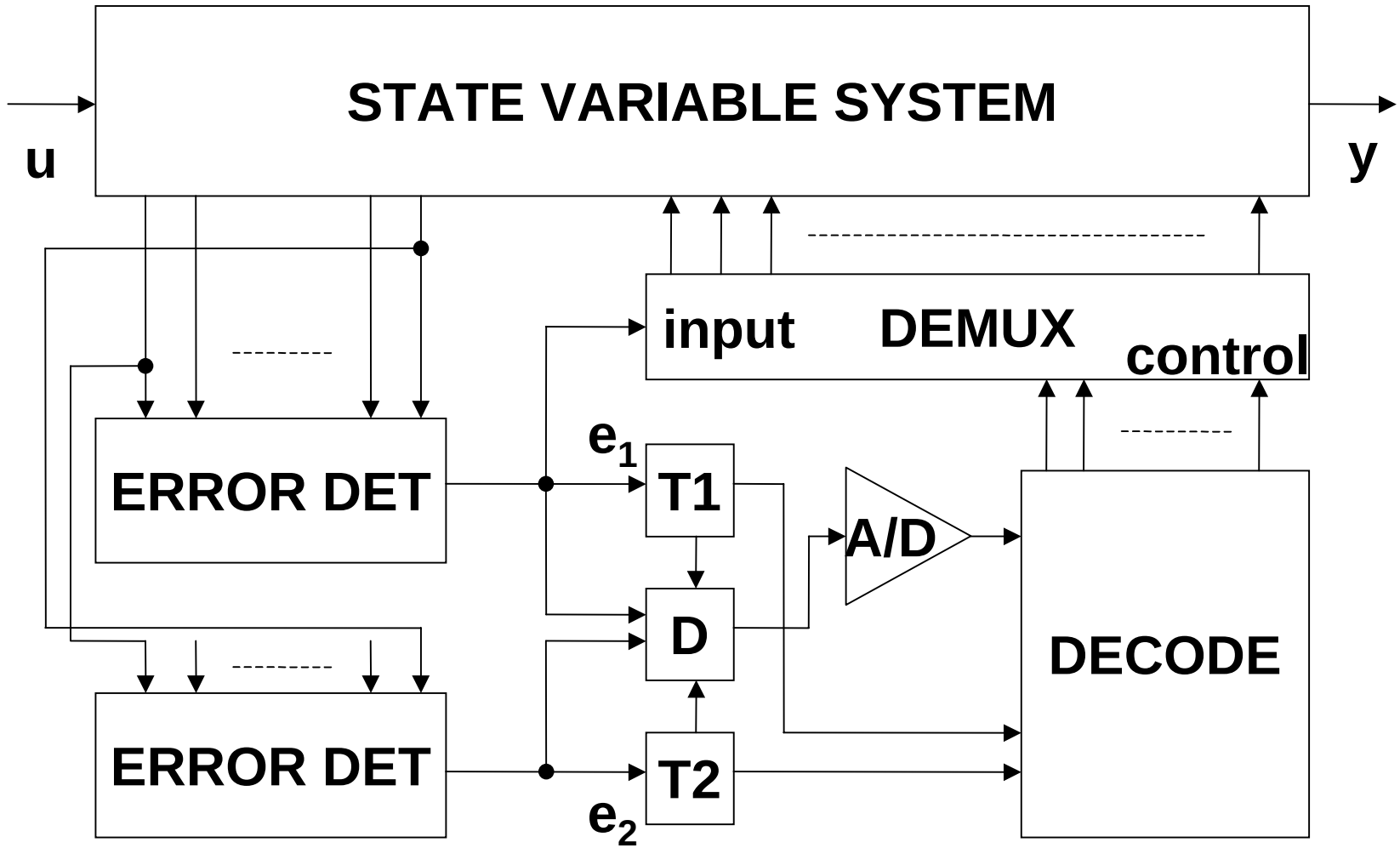
Expanded State Equation

Add two state variables

$$\begin{bmatrix} x_1(s) \\ x_2(s) \\ \cdot \\ \cdot \\ \cdot \\ x_n(s) \\ x_{n+1}(s) \\ x_{n+2}(s) \end{bmatrix} = \begin{bmatrix} a_{11} & a_{12} & \cdot & \cdot & \cdot & a_{1n} & 0 & 0 \\ a_{21} & a_{22} & \cdot & \cdot & \cdot & a_{2n} & 0 & 0 \\ \cdot & \cdot & \cdot & & & \cdot & \cdot & \cdot \\ \cdot & \cdot & & \cdot & & \cdot & \cdot & \cdot \\ \cdot & \cdot & & & \cdot & \cdot & \cdot & \cdot \\ a_{n1} & a_{n2} & \cdot & \cdot & \cdot & a_{nn} & 0 & 0 \\ \gamma_{11} & \gamma_{12} & \cdot & \cdot & \cdot & \gamma_n & 0 & 0 \\ \gamma_{21} & \gamma_{22} & \cdot & \cdot & \cdot & \gamma_{2n} & 0 & 0 \end{bmatrix} \begin{bmatrix} \frac{x_1(s)}{s} \\ \frac{x_2(s)}{s} \\ \cdot \\ \cdot \\ \cdot \\ \frac{x_n(s)}{s} \\ \frac{x_{n+1}(s)}{s} \\ \frac{x_{n+2}(s)}{s} \end{bmatrix} + \begin{bmatrix} b_1 \\ b_2 \\ \cdot \\ \cdot \\ \cdot \\ b_n \\ \beta_1 \\ \beta_2 \end{bmatrix} \frac{\mu(s)}{s}$$

It can be show that $\frac{e_2(s)}{e_1(s)} = \frac{\alpha_{2i}}{\alpha_{1i}}$ if faults directly affect $x_i(s)$

Fault Diagnosis and Error Correction Architecture



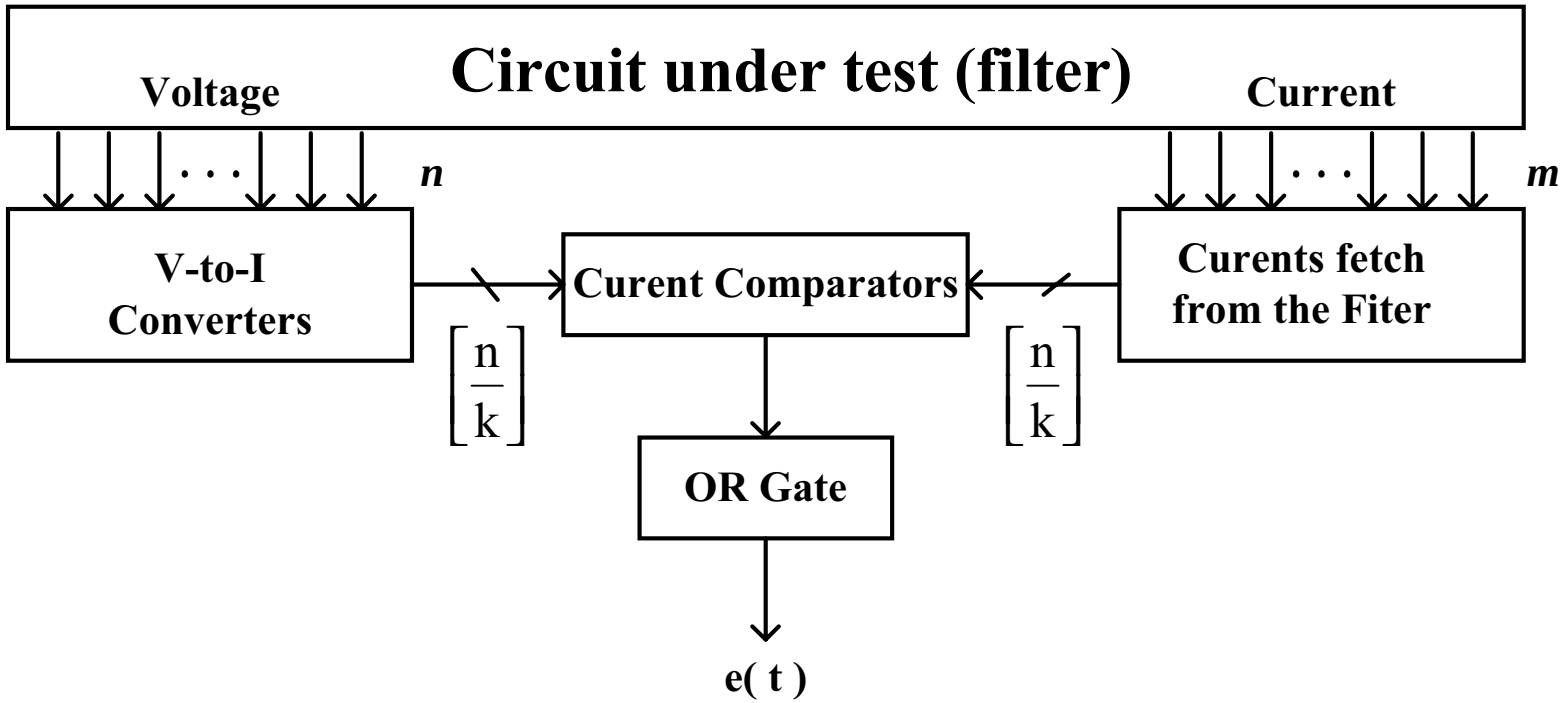
State Equations of an OTA System

A fifth-order low-pass Chebyshev filter using OTA

$$\mathbf{I(t) = AV\,(t) + B}\,\boldsymbol{u}(\,\mathrm{t}\,)$$

$$\begin{bmatrix} i_1(t) \\ i_2(t) \\ i_3(t) \\ i_4(t) \\ i_5(t) \end{bmatrix} = \begin{bmatrix} -g_m & g_m & 0 & 0 & 0 \\ -g_m & 0 & g_m & 0 & 0 \\ 0 & g_m & 0 & g_m & 0 \\ 0 & 0 & g_m & 0 & g_m \\ 0 & 0 & 0 & g_m & -g_m \end{bmatrix} \begin{bmatrix} i_1(t) \\ i_2(t) \\ i_3(t) \\ i_4(t) \\ i_5(t) \end{bmatrix} + \begin{bmatrix} g_m \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} u(t)$$

Test Structure of the filter



The architecture for testable low-pass OTA-C filter.