Modern RFIC Design

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Outline – (I)

- **RF basic fundamental**
- **Transceiver architecture**
- **RF building block**
- **Case Study**

Outline – (II)

- **Case study I:**

(H-S Kao, M-J Yang and T-C Lee,” A *A Delay-Line-Based GFSK Demodulator for Low-IF Receivers*”, ISSCC, 2007.) → *Low IF*

RF Fundamentals

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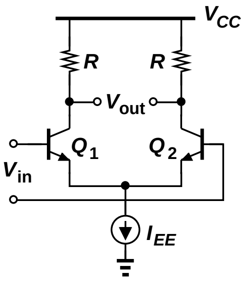
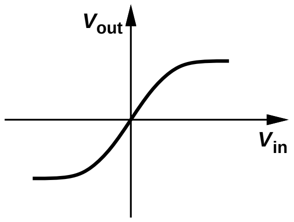
Symmetry

If x(t) and –x(t) give the same y(t), we say the system has odd symmetry. Analog designers call it “differential” and RF designers, “balanced”

Example:



(a)



(b)

With odd symmetry, all even-order terms are absent:

$$y(t) = \alpha_1 x(t) + \alpha_3 x^3(t) + \cdots$$

Effect of Nonlinearity

- **Harmonic distortion:**

$$x(t) = A\cos\omega t,\ \ y(t) = \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) + \cdots$$

$$\Rightarrow y(t) = \alpha_1 A\cos\omega t + \alpha_2 A^2 \cos^2 \omega t + \alpha_3 A^3 \cos^3 \omega t + \cdots$$

$$= (\alpha_1 A + \frac{3}{4}\alpha_3 A^3)\cos\omega t + (\quad)\cos 2\omega t + (\quad)\cos 3\omega t + \cdots$$

Note that:

❑ **with odd-order symmetry, even harmonics are absent.**

❑ **Amplitude of n-th order harmonic** $\propto A^n$

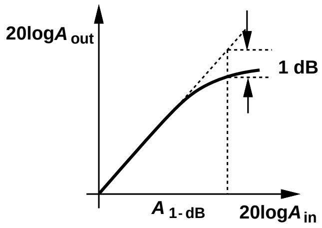
Gain compression:

Nonlinearity can also be viewed as variation of small-signal gain. In most systems, as the input level increases, the gain decreases, I.e., the nonlinearity is “compressed”.

For compressive nonlinearity, α_3 has to be negative (if we neglect higher order terms).

1-dB Compression Point

- **The input level that causes the small-signal gain to drop by 1 dB. To calculate this point, we write:**



$$20\log(\alpha_1 + \frac{3}{4}\alpha_3 A^3) = 20\log\alpha_1 - 1$$

$$\Rightarrow A_{1-dB} = \sqrt{0.145\left|\frac{\alpha_1}{\alpha_3}\right|}$$

In typical RF systems, the front-end 1-dB compression of the receive path is ~ -20 to –25 dBm.

<u>Desensitization and Blocking</u>:

If a weak signal and a strong interference experience a compressive nonlinearity, the "average" gain for the weak signal decreases. $x(t) = A_1\cos\omega_1 t + A_2\cos\omega_2 t$

$$\Rightarrow y(t) = \left(\alpha_1 A_1 + \frac{3}{4}\alpha_3 A_1^3 + \frac{3}{2}\alpha_3 A_1 A_2^2\right)\cos\omega_1 t + \cdots$$

Desensitization and Blocking

For $A_1 << A_2 : y(t) = \left(\alpha_1 A_1 + \frac{3}{2}\alpha_3 A_1 A_2^2\right)\cos\omega_1 t + \cdots$

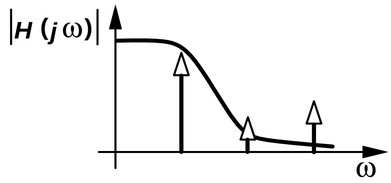
We say the large interference "desensitizes" the circuits.

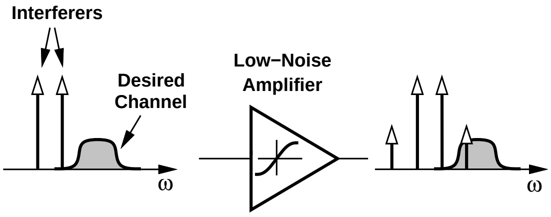
<u>Example:</u>

If $\left(\alpha_1 A_1 + \frac{3}{2}\alpha_3 A_1 A_2^2\right) = 0$ **, we say the desired signal is "blocked".**

Intermodulation (I)

In many cases, harmonic distortion is not adequate to characterize the nonlinearity:





So, we need to ensure that the result of nonlinearity falls in the band of interest. → Perform "two-tone" test.

$$x(t) = A_1 \cos\omega_1 t + A_2 \cos\omega_2 t \qquad y(t) = \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) + \cdots$$

The output has the following components:

$$\omega = \omega_1 \pm \omega_2 : \alpha_1 A_1 A_2 \cos(\omega_1 + \omega_2)t + \alpha_2 A_1 A_2 \cos(\omega_1 - \omega_2)t$$

$$\omega = 2\omega_1 \pm \omega_2 : \frac{3}{4}\alpha_3 A_1^2 A_2 \cos(2\omega_1 + \omega_2)t + \frac{3}{4}\alpha_3 A_1^2 A_2 \cos(2\omega_1 - \omega_2)t$$

$$\omega = 2\omega_2 \pm \omega_1 : \frac{3}{4}\alpha_3 A_2^2 A_1 \cos(2\omega_2 + \omega_1)t + \frac{3}{4}\alpha_3 A_2^2 A_1 \cos(2\omega_2 - \omega_1)t$$

Intermodulation (II)

And main components:

$$\omega = \omega_1, \omega_2 : \left(\alpha_1 A_1 + \frac{3}{2}\alpha_3 A_1 A_2^2 + \frac{3}{4}\alpha_3 A_1^{\ 3}\right)\cos\omega_1 t + \left(\alpha_1 A_2 + \frac{3}{2}\alpha_3 A_2 A_1^2 + \frac{3}{4}\alpha_3 A_2^{\ 3}\right)\cos\omega_2 t$$

We call the components at $\omega = 2\omega_1 \pm \omega_2$ **and** $\omega = 2\omega_2 \pm \omega_1$ **the third-order intermodulation products (IM$_3$ product)**

$$\frac{3}{4}\alpha_3 A_1^{\ 2} A_2 \cos(2\omega_1 - \omega_2)t \qquad \frac{3}{4}\alpha_3 A_2^{\ 2} A_1 \cos(2\omega_2 - \omega_1)t$$

Two-tone test is indeed a realistic representation in RF systems:

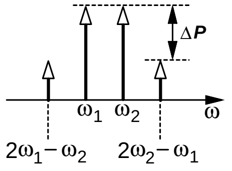
Third Intercept Point (IP_3) – (I)

Using two tones with the same amplitude, we increase the input level. The fundamentals at the output increases in proportion to *A* whereas the IM products increase in proportion to *A*^{3}.

$$y(t)=\left(\alpha_1+\frac{3}{2}\alpha_3A^2\right)A\cos\omega_1t+\left(\alpha_1+\frac{3}{2}\alpha_3A^2\right)A\cos\omega_2t+$$

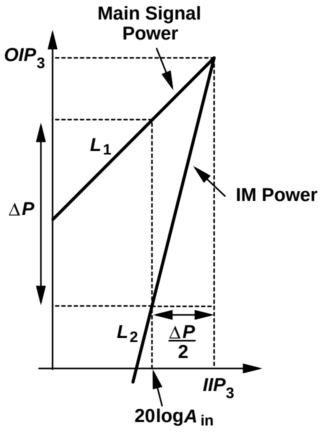
$$\frac{3}{4}\alpha_3A^3\cos(2\omega_1-\omega_2)t+\frac{3}{4}\alpha_3A^3\cos(2\omega_2-\omega_1)t+\cdots$$

Plot both:



$$IIP_3\big|_{dBm}=\frac{\Delta P\big|_{dB}}{2}+P_{in}\big|_{dBm}$$

(a)



(b)

Third Intercept Point (IP_3) – (II)

To calculate IP$_3$:

$$\alpha_1A_{IP3}=\frac{3}{4}\alpha_3A_{IP3}{}^3\Rightarrow A_{IP3}=\sqrt{\frac{4|\alpha_1|}{3|\alpha_3|}}$$

$$\Rightarrow OIP_3=IIP_3+Gain$$

Relationship between 1-dB compression point & IP$_3$:

$$\frac{A_{1-dB}}{A_{IP3}}=\sqrt{\frac{0.145}{4/3}}\cong-9.6dB$$

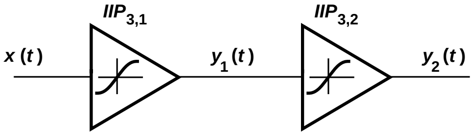
Quick method for IIP3:

$$20\log A_{IP3}=\frac{\Delta P}{2}+P_{in}\big|_{dBm}$$

The input IP$_3$ of typical LNAs is ~ – 10 to –15 dBm (70mV$_{rms}$ to 40 mV$_{rms}$) :

Cascade Nonlinear Stages

$$y_1(t)=\alpha_1 x(t)+\alpha_2 x^2(t)+\alpha_3 x^3(t) \qquad y_2(t)=\beta_1 x(t)+\beta_2 x^2(t)+\beta_3 x^3(t)$$



$$\Rightarrow A_{IP3}=\sqrt{\frac{4}{3}\left|\frac{\alpha_1\beta_1}{\alpha_3\beta_1+2\alpha_1\alpha_2\beta_2+\alpha_1{}^3\beta_3}\right|}$$

$$\Rightarrow \alpha_1\uparrow,$$

Prove that:

$$\frac{1}{IP_{3,tot}^2}\approx\frac{1}{IP_{3,1}^2}+\frac{\alpha_1^2}{IP_{3,2}^2}+\frac{3\alpha_2\beta_2}{2\beta_1}$$

Noise Figure (I)

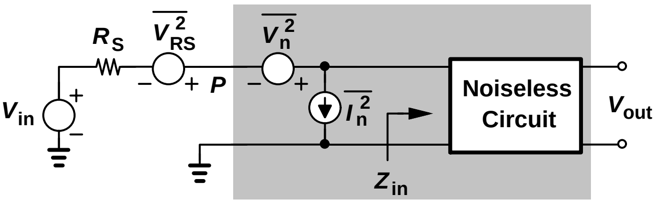
$$NF\overset{\Delta}{=}\frac{SNR_{in}}{SNR_{out}}$$

- **NF is a measure of how much the SNR degrades as the signal passes through system.**

- **If input has no noise, NF=∞!**

- **In RF systems, the received signal is corrupted by background noise and antenna radiation resistance noise.**

NF calculation:



$$\overline{v_{RS}^2}=4kTR_S$$

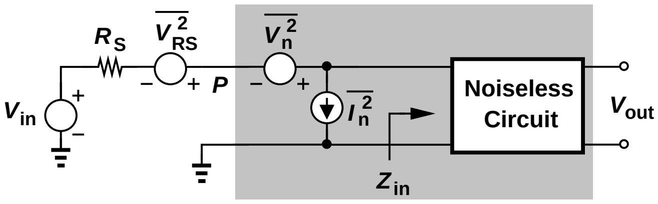
$$SNR_{in}=\frac{\alpha^2 V_{in}^2}{\alpha^2\overline{V_{RS}^2}}$$

$$=\frac{V_{in}^2}{\overline{V_{RS}^2}}$$

$$\alpha=\left|\frac{Z_{in}}{Z_{in}+R_S}\right|$$

Noise Figure (II)

For total noise that goes into the circuit:



Thus, the total noise power at the output:

$$\overline{v_{n,out}^2} = \alpha^2 A_V^2\left[\overline{V_{RS}^2} + \overline{(V_n + i_n R_S)^2}\right], \alpha = \frac{Z_{in}}{Z_{in} + R_s}$$

And the total signal power at the output:

$$v_{S,out}^2 = \alpha^2 A_V^2 V_{in}^2$$

$$\Rightarrow SNR_{out} = \frac{V_{in}^2}{\overline{V_{RS}^2} + \overline{(V_n + i_n R_S)^2}} \Rightarrow NF = 1 + \frac{\overline{(v_n + i_n R_s)^2}}{4kTR_s}$$

$$\Rightarrow NF_{\min} = 1 @ \text{no noise}$$

Noise Figure (III)

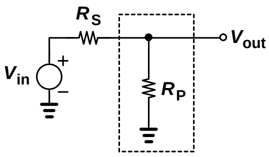
For simulation purpose:

$$\Rightarrow NF = \frac{V_{in}^2/\overline{V_{RS}^2}}{\alpha^2 A_V^2 V_{in}^2/\overline{V_{n,out}^2}} = \frac{\overline{V_{n,out}^2}}{\alpha^2 A_V^2}\frac{1}{4kTR_S}$$

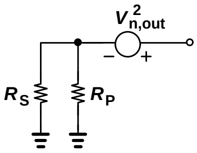
Typical LNAs achieve NF ~ 2dB.

Note: For a given source impedance, we can represent $\overline{(V_n + i_n R_S)^2}$ **as one series noise voltage:**

<u>Example</u>: What is NF of the following circuit?



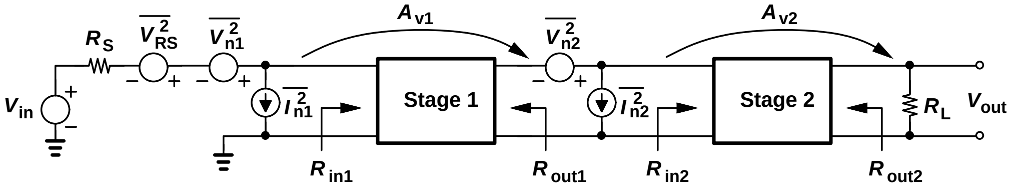
(a)



(b)

Noise Figure of Cascaded Stages

Cascaded noisy stages



Friis Equation:

$$NF_{Total} = 1 + (NF_1 - 1) + \frac{(NF_2 - 1)}{A_{V1}^2}$$

$$= 1 + (NF_1 - 1) + \frac{(NF_2 - 1)}{A_{P1}^2}$$

Try to prove it: calculate $\overline{V_{n,in1}^2}$, $\overline{V_{n,in2}^2}$

Noise contributed by a stage decreases as the gain preceding the stage increases.

If a stage exhibits attenuation (loss), NF of the following circuit is "amplified".

Sensitivity

Sensitivity is defined as the minimum signal level that the system can detect with acceptable signal-to-noise ratio:

$$NF \overset{\Delta}{=} \frac{SNR_{in}}{SNR_{out}} = \frac{P_{sig} / P_{RS}}{SNR_{out}} \quad \Rightarrow P_{sig} = P_{RS} \cdot NF \cdot SNR_{out}$$

Since the overall signal power is distributed across the channel, both sides must be integrated on the bandwidth.

$$P_{sig,tot} = P_{RS} \cdot NF \cdot SNR_{out} \cdot B$$

How much is *P_{rs}* in a 50-Ω system?

$$\Rightarrow P_{sig,tot}\Big|_{dBm} = -174dBm + NF\Big|_{dB} + 10\log B + SNR_{\min}$$

For example, in the European standard (GSM), *SNR_{min}*~ 12 dB, and B=200 kHz. Thus, if the receiver NF is 9 dB.

We have: Sensitivity=-174+9+53+12=-100 dBm

Dynamic Range (I)

The upper end of DR (actually "spurious-free" dynamic range, (SFDR) is defined as the max. input two-tone level for which intermod products do not exceed the noise floor:

If everything is expressed in dB or dBm:

$$IIP_3 = P_{in} + \frac{P_{out} - P_{IMD}}{2},$$

, where *P_{out}* and *P_{IMD}* are measured at the output. To refer to the input, we have $P_{out} = P_{in} + G$ **and** $P_{IMD} = P_{IMD,in} + G$

Where G is the gain.

$$\Rightarrow P_{in,MAX} = \frac{Noise\_Floor + 2IIP_3}{3}$$

SFDR is defined as the difference (in dB) between *P_{in}* and the sensitivity:

Dynamic Range (II)

$$\Rightarrow SFDR = \frac{Noise\_Floor + 2IIP_3}{3} - (Noise\_Floor + SNR_{\min})$$

$$= \frac{2}{3}(IIP_3 - Noise\_Floor) - SNR_{\min}$$

, where *Noise floor=-174 dBm+NF+10log B*

<u>Example</u>: In the previous example, suppose *IIP_3* =-15 dBm.
Then, SFDR=2/3(-15-(-112))-12=52.7 dB

SFDR is indication of how much interference the system can tolerate while providing an acceptable signal quality.

Transceiver Architectures

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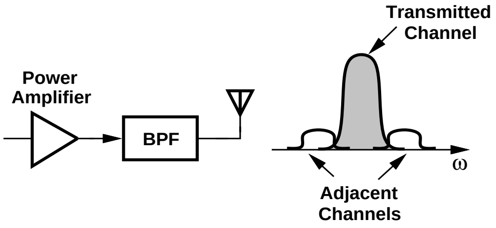
General Issues (I)

General Issues:

Transmitter:

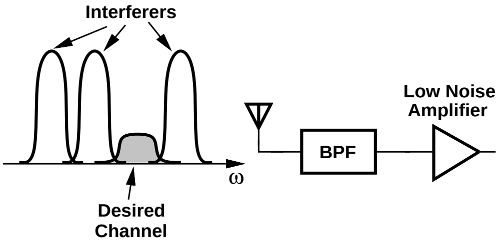
- **Output power**
- **Efficiency**
- **Adjacent channel noise**
- **Out of band noise, spurs and harmonics**
- **PA switching and battery output impedance**



(a)

Receiver:

(1) Sensitivity (NF), Dynamic range (IP3),…
(2) In-band interference rejection
(3) Out of band interference rejection
(4) Band selection vs. channel selection



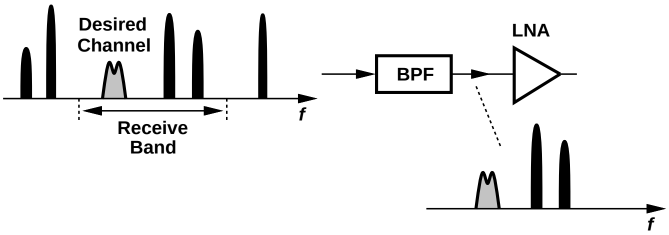
(b)

General Issues (II)

Band and channel:

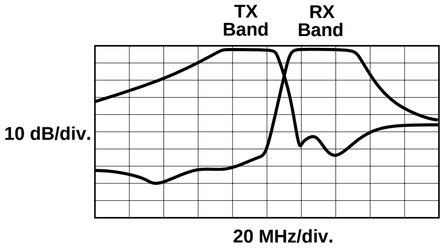
For GSM receive band spans from 935MHz to 960 MHz. Each channel occupies 200 kHz.

“band selection” → rejects out-of-band interference.
“channel selection” → rejects in-band interference



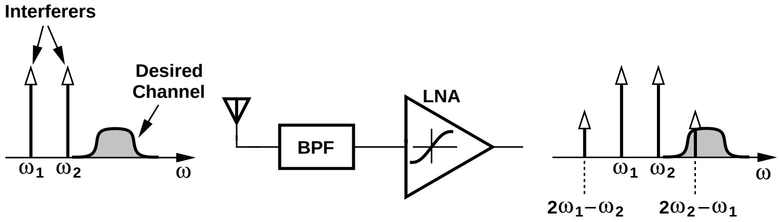
Typical duplexer frequency response:

20 MHz → 30 dB suppression



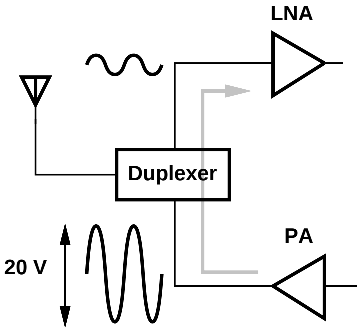
General Issues (III)

Effect of nonlinearity in the front end:

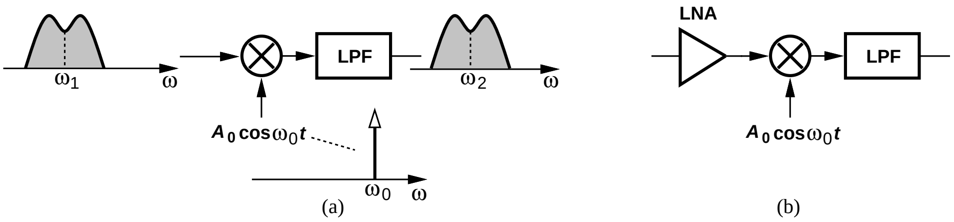


Desensitization of LNA by PA:

DR of signal can be up to 100 dB.



Heterodyne Receivers (I)



(a) (b)

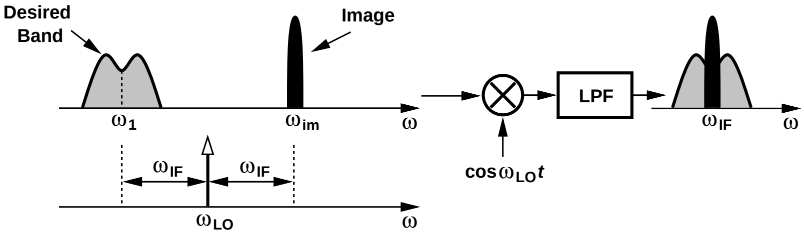
Full channel selection: may be possible if channel spacing is large enough.

Partial channel selection: may have to lower the interference to some extent so we can have a reasonable linearity in the following stage.

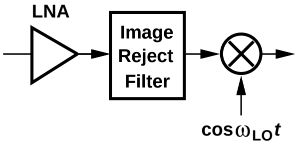
Heterodyne Receivers (II)

Problem of image:

A simple multiplier (mixer) does not preserve the polarity of the difference between its two input frequencies:

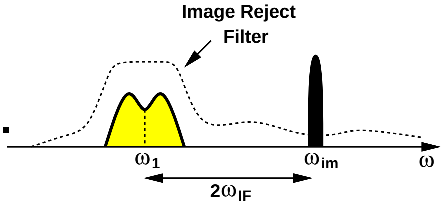


Why important?
→ The air is full of RF signal.



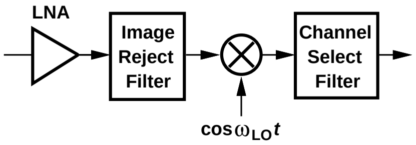
So we use an "image-reject" filter.
→ $2\omega_{If}$ is large → image rejection can be enough.

The choice of IF depends
(1) The amount of noise image.
(2) Space between the desired band and image.
(3) The loss of image reject filter.

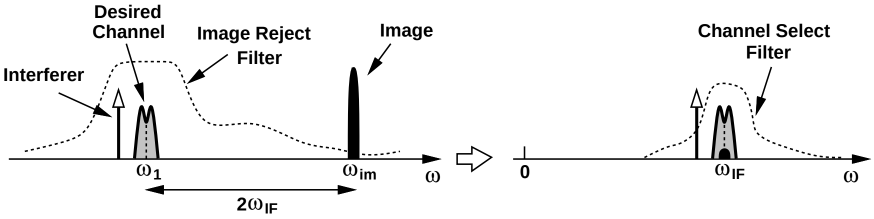


Heterodyne Receivers (III)

Sensitivity-Selectivity "Trade-off":
To suppress the image, we need a high IF. However, as IF increases and becomes comparable with the RF input, the premise of heterdyning is violated.

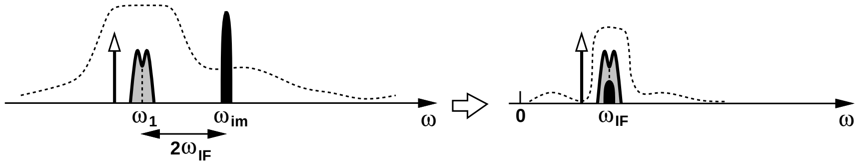


High IF



(a)

Low IF



(b)

IF filter depends availability of SAW filter such as 10.7 MHz.

Heterodyne Receivers (IV)

- **High-side & low-side injection:**

- If $\omega_{LO}>\omega_{in}$, we call it "high-side injection". If this case, the image frequency > ω_{LO}.
- If $\omega_{LO}<\omega_{in}$, we call it "low-side injection". In this case, the image frequency < ω_{LO} .

The choice depends on the frequency bands needed in other parts of the system (e.g. TX), and the noise in the image.

- **Problem of Half IF:**

If the RF signal path, I.e., the LNA and the mixer, exhibit second-order distortion and the local oscillator also contains a significant "second harmonic", then an interesting effect arises:

Heterodyne Receivers (V)

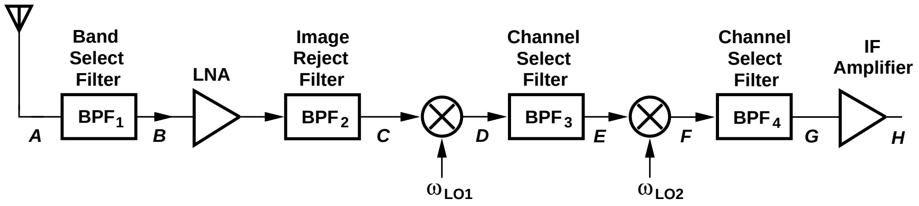
Another mechanism is that the interference is translated to $\frac{\omega_{LO}-\omega_{in}}{2}$ And subsequently experiences second-order distortion in the IF amplifier.
→ Image-reject filter must suppress components at $\frac{\omega_{in}+\omega_{LO}}{2}$ as well.

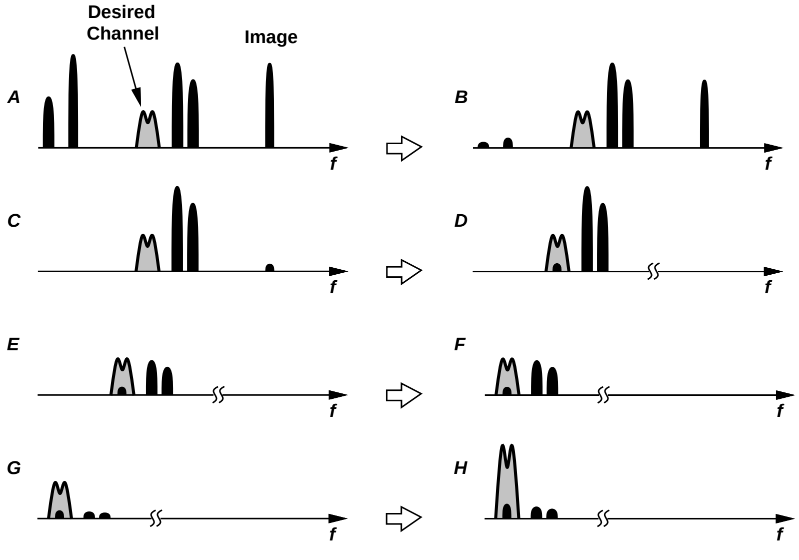
- **Double-conversion heterodyne receivers:**

To relax the trade-off between sensitivity and selectivity, we use two downconversions, each followed by partial channel selection.

Heterodyne Receivers (VI)

- **Double-conversion heterodyne receivers (dual-IF topology):**





Homodyne Receivers (I)

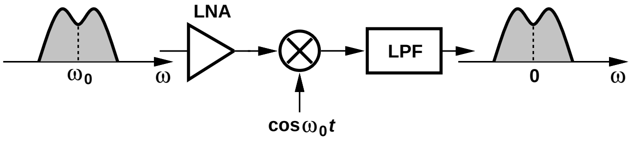
- Homodyne receiver (direct conversion receivers):

  Need quadrature downconversion in frequency- and phase modulated systems.

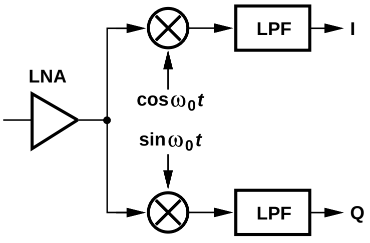
(1) Only OK dor AM.

(2) FM requires quadrature

Output.



(a)



(b)

Advantages over heterodyne:

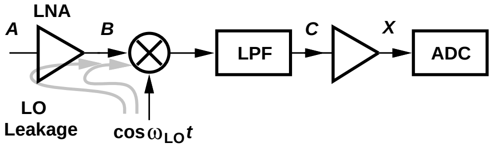
1. **No image.**
2. **LNA need not drive 50 Ω.**
3. **Channel selection is performed at low frequencies. In other words, direct conversion appears to be a good candidate for monolithic implementation.**

Homodyne Receivers (II)

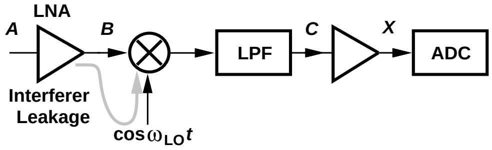
But, there are many issues as well.

• DC offset:
Since the downconverted band extends to zero frequency, extraneous offsets corrupt the signal and, more importantly, saturate the following stage. The sources of DC offset arise from

1. Device mismatch
2. LO leaks to RX and self-mixing.
3. Signal reflects due to non-stationery channel.



(a)



(b)

Homodyne Receivers (III)

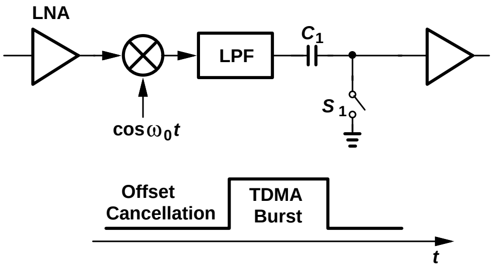
Thus, we need to remove or cancel the offset.

- **AC coupling:**

A high-pass RC filter can block the DC signal.

But, it corrupts the data unless $\frac{1}{2\pi RC} < 0.1\% R_b$**, where** R_b **is the data rate**

→ for 200-kHZ channel BW, f_{HPF} **=20 Hz.**

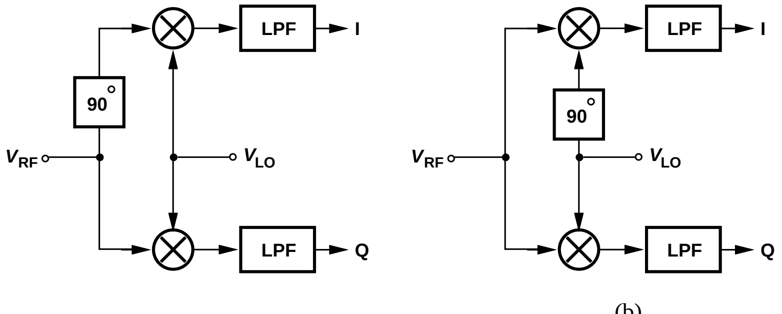


- **Offset cancellation:**

→ 1-μV_{rms} received, 30 dB gain → requires 200 pF so as $\sqrt{\frac{kT}{C}}$ **can be 15 dB below the signal.**

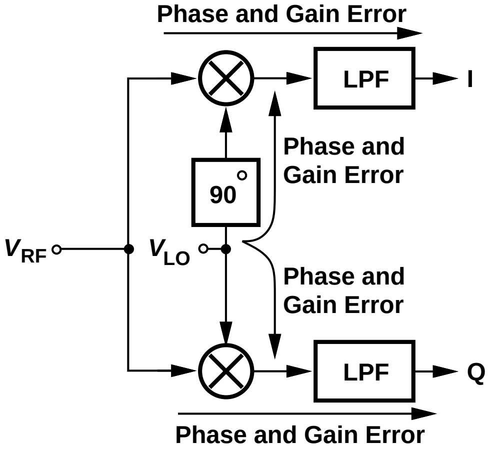
But kt/C significant. C~200 pF. What's the total cap?
→ for I/Q with differential circuits, it requires 4 large cap.

I/Q Mismatch in DCR



(a) (b)

Mismatches are more significant here than in the second downconverter of heterodyne receivers.



I/Q mismatch distorts the constellation and leads to cross-talk between the two downconverted signals.

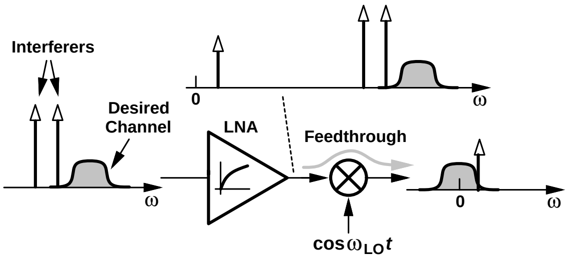
Acceptable phase mismatch is < 5° in most cases. Gain mismatch of a few *dB* may be tolerable.

Even-Order Distortion in DCR (I)

If the LNA or mixer exhibit even-order distortion, e.g. $y(t) = \alpha_1 x(t) + \alpha_2 x^2(t)$ **then two interferers create a "beat" signal.**

$$x(t) = A_1 \cos\omega_1 t + A_2 \cos\omega_2 t$$

$$\Rightarrow y(t) = 2A_1A_2\frac{\alpha_2}{2}\cos(\omega_1 - \omega_2)t$$



The beat signal leaks through the mixer if the latter has mismatches or is driven by an LO signal having a non-50% duty cycle.

Second-order distortion is characterized by IP$_2$.

Even-Order Distortion in DCR (II)

Solutions:

1. Differential Circuits:
The problem is that the antenna and duplexer are usually single-ended. → Need single-end/differential conversion.

The other problem is that a differential LNA has higher noise (for a given power dissipation).

2. Block the beat: What's the problem?

Other Distortion in DCR

- **Flicker noise:**

Since the gain of LNA/mixer is ~ 30 dB, the baseband signals are still quite small (tens of mV). Thus, the input noise of the following stages is still critical. Particularly, the 1/f noise of CMOS circuits.

- **LO leakage:**

The leakage of the LO signal to the antenna creates interference in the band of other uses. FCC and wireless standards impose upper limits of ~ -50 dB to –80 dBm.

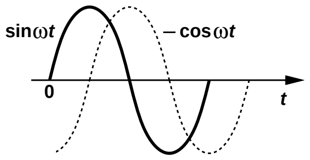
If the oscillator is integrated on the same chip and designed as a fully-differential circuit, the leakage can be acceptably low.

Image-Rejection Receivers (I)

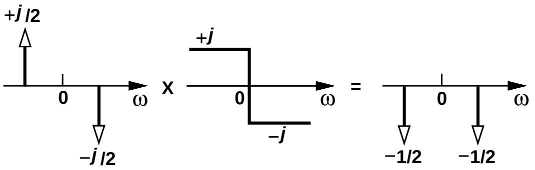
The idea here is to design the circuit topology so that it can distinguish between the signal and the image and somehow cancel the later.

But, first some concepts.

- Shift by 90^o operation: A narrow-band signal is shifted by 90^o if its spectrum is multiplied by $G(\omega) = -j\,\mathrm{sgn}(\omega) \leftarrow$ **Hilbert Transform.**

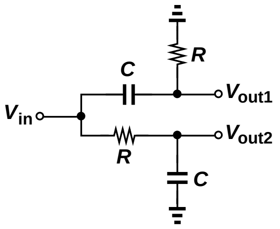


(a)



(b)

- Simple 90^o circuit:



For V_{out1}: $\phi_1 = \tan^{-1} RC\omega$

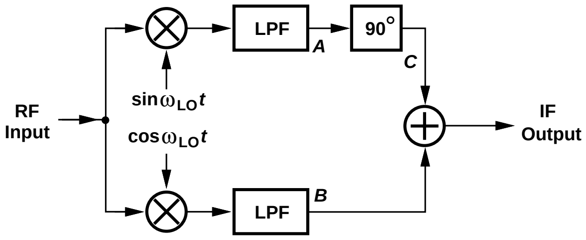
For V_{out2}: $\phi_2 = \tan^{-1} \frac{1}{RC\omega}$

$\rightarrow$ **V_{out1} and V_{out2} have different gain.**

Hartley Architecture (I)

The phase difference between V_{out1} and V_{out2} is equal to 90^o for all frequencies.

- **Hartley architecture:**



- Simple analysis: $x(t) = A_{RF}\cos\omega_{RF}t + A_{im}\cos\omega_{im}t$

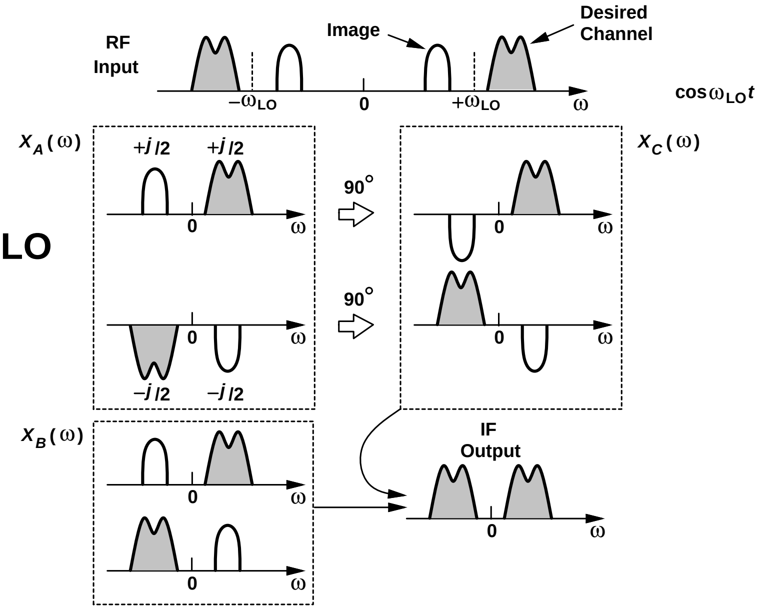
$$\Rightarrow \begin{cases} x_A(t) = \dfrac{A_{RF}}{2}\sin(\omega_{LO}-\omega_{RF})t + \dfrac{A_{im}}{2}\sin(\omega_{LO}-\omega_{IM})t \\ x_B(t) = \dfrac{A_{RF}}{2}\cos(\omega_{LO}-\omega_{RF})t + \dfrac{A_{im}}{2}\cos(\omega_{LO}-\omega_{IM})t \end{cases}$$

How do we shift $x_A(t)$ by 90^o? Recall that $-j\text{sgn}(\omega)$ multiplies negative and positive frequencies by opposite factors.

Hartley Architecture (II)

Thus, $x_C(t) = \dfrac{A_{RF}}{2}\cos(\omega_{LO}-\omega_{RF})t - \dfrac{A_{im}}{2}\cos(\omega_{LO}-\omega_{im})t$

- Graphical Analysis:



- The principle issue is sensitivity to mismatches: LO phase imbalance; gain and phase mismatch in the two signal paths.

Image Rejection Ratio (I)

For simplicity, we lump all the phase and gain mismatch in the LO signals: $A_{LO}\sin\omega_{LO}t$ **and** $\left(A_{LO}+\varepsilon\right)\sin\left(\omega_{LO}t+\theta\right)$

After multiplication and LPF:

$$x_A(t)=\frac{A_{LO}A_{RF}}{2}\sin\left(\omega_{LO}-\omega_{RF}\right)t+\frac{A_{LO}A_{im}}{2}\sin\left(\omega_{LO}-\omega_{im}\right)t$$

$$x_B(t)=\frac{\left(A_{LO}+\varepsilon\right)A_{RF}}{2}\sin\left[\left(\omega_{LO}-\omega_{RF}\right)t+\theta\right]+$$

$$\frac{\left(A_{LO}+\varepsilon\right)A_{im}}{2}\sin\left[\left(\omega_{LO}-\omega_{im}\right)t+\theta\right]$$

Thus, $x_C(t)=A_{LO}\left[\frac{A_{RF}}{2}\cos\left(\omega_{LO}-\omega_{RF}\right)t-\frac{A_{im}}{2}\cos\left(\omega_{LO}-\omega_{im}\right)t\right]$

At output,

$$\begin{cases} x_{sig}(t)=\dfrac{A_{LO}+\xi}{2}A_{RF}\cos(\omega_{LO}-\omega_{RF})t+\dfrac{A_{LO}}{2}A_{RF}\cos(\omega_{LO}-\omega_{IM})t \\ x_{img}(t)=\dfrac{A_{LO}+\xi}{2}A_{img}\cos(\omega_{LO}-\omega_{RF})t-\dfrac{A_{LO}}{2}A_{img}\cos(\omega_{LO}-\omega_{IM})t \end{cases}$$

Image Rejection Ratio (II)

We define the image rejection ratio as: $IRR=\dfrac{\left.\dfrac{\text{Image}}{\text{Signal}}\right|_{out}}{\left.\dfrac{\text{Image}}{\text{Signal}}\right|_{in}}=\left(\dfrac{A_{img}}{A_{RF}}\right)^2$

$$\left.\frac{\textbf{Image}}{\textbf{Signal}}\right|_{out}=\frac{A_{im}^2}{A_{RF}^2}\frac{\left(A_{LO}+\varepsilon\right)^2-2A_{LO}(A_{LO}+\varepsilon)\cos\theta+A_{LO}^2}{\left(A_{LO}+\varepsilon\right)^2+2A_{LO}(A_{LO}+\varepsilon)\cos\theta+A_{LO}^2}$$

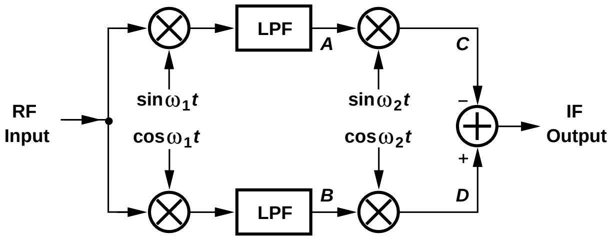
$$IRR=\frac{A^2-2AB\cos\theta+B^2}{A^2+2AB\cos\theta+B^2}\qquad\begin{cases}A=A_{LO}\\B=A_{LO}+\varepsilon\end{cases}$$

If $\theta<<$ **1rad,** $\dfrac{\Delta\mathbf{A}}{\mathbf{A}}<<1, IRR\cong\dfrac{\theta^2+\left(\dfrac{\Delta A}{A}\right)^2}{4}$

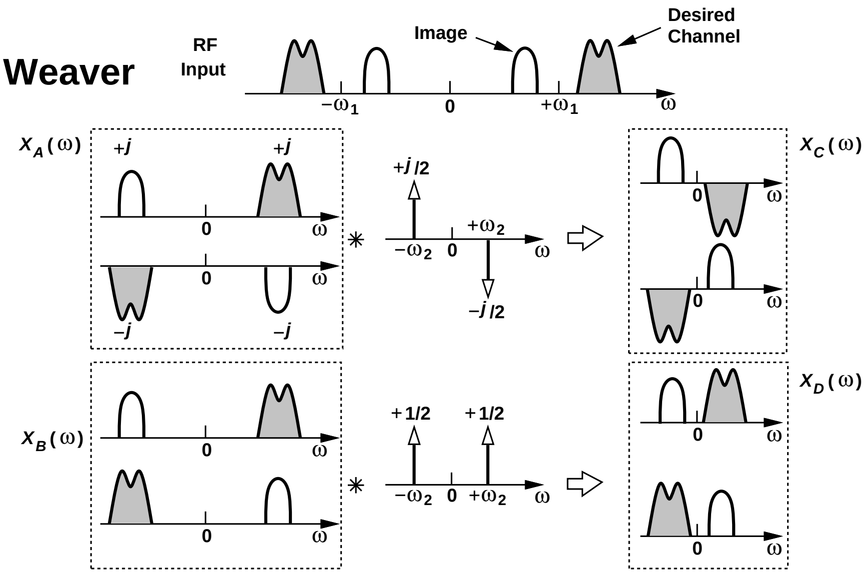
Other design issues: 1. Noise and attenuation of the 90º circuit.
2. Noise and linearity of the adder.
3. IRR value is insensitive to the absolute value of RC.

Weaver Architecture (I)

Multiplication by quadrature phases of w2 is similar to a 90^{o} phase shift. Analytical and graphical proofs are the same as those for Hartley architecture.

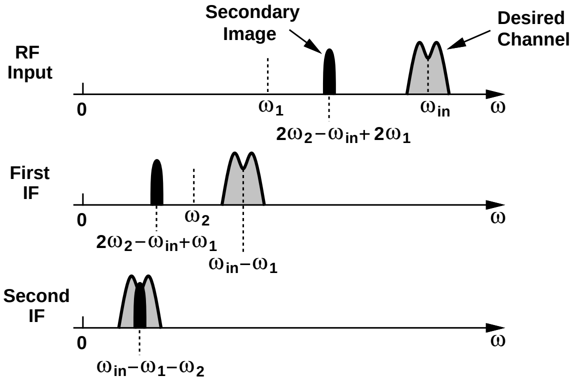


-Graphical analysis of Weaver architecture:



Weaver Architecture (II)

-Problem of secondary image
The second quadrature mixing operation entails an image problem



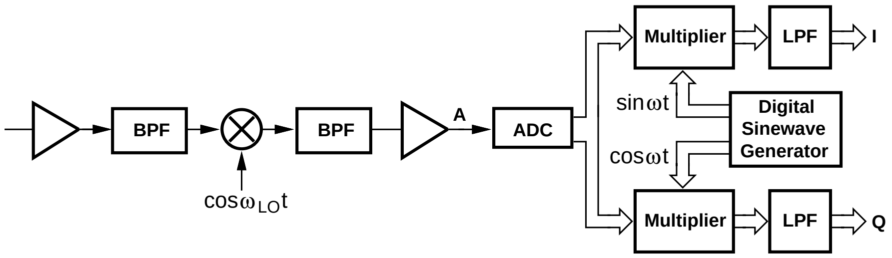
→ **We can choose LO frequency such that it translates the spectrum into baseband.**

$$\rightarrow \omega_{in} = \omega_1 \pm \omega_2$$

→ **The image becomes iteself..**

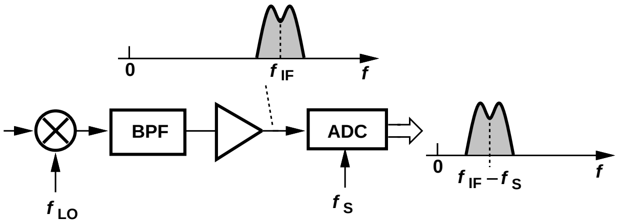
Digital IF

- **Second set of mixing and filtering can be performed more efficiently in the digital domain.**



Typical issue is that we need very high-speed ADC → 100 to 400 MHz 14-bit resolutions. Ex: Typical IF = 50 ~ 200 MHz.

- **Sampling IF architecture:**

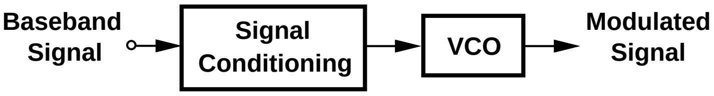


Transmitter Architectures (I)

General Issues:

1. Baseband/RF interference:

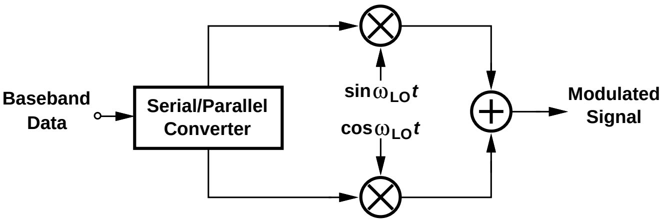
- FM:



Signal conditioning shapes the baseband spectrum and amplitude such that the VCO output has acceptably low out-of-channel power.

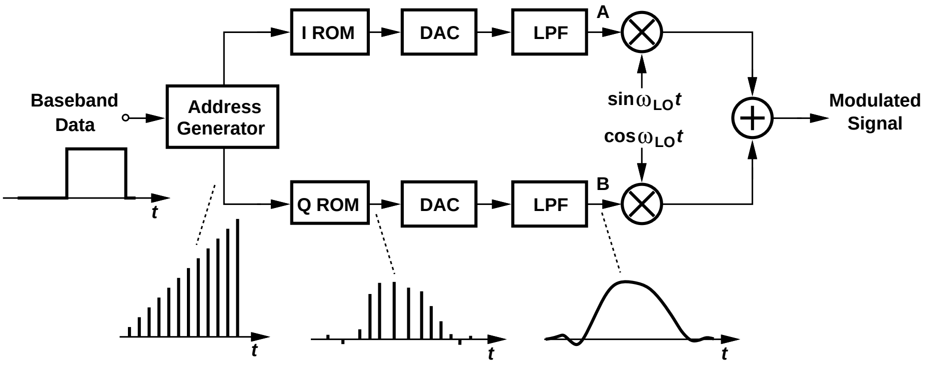
The VCO is usually embedded in a "frequency synthesizer" to stabilize its center frequency.

- Quadrature modulation:

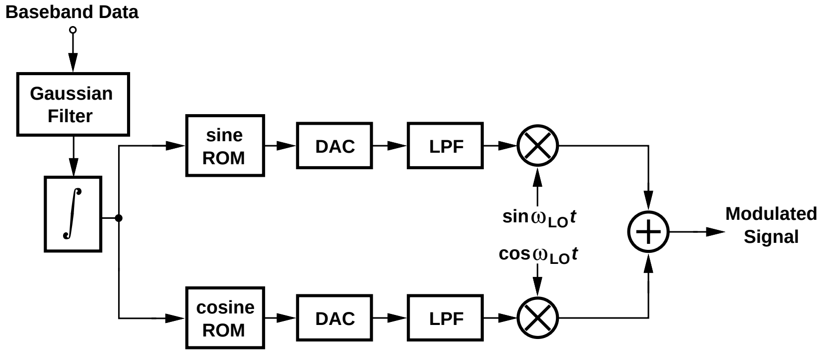


Transmitter Architectures (II)

Baseband pulse shaping:

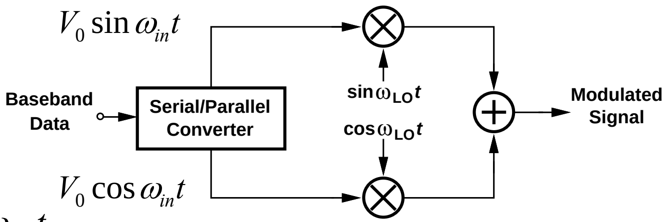


Baseband shaping in GMSK system



Transmitter Architectures (III)

Phase and gain mismatch: Apply baseband quadrature sinusoids and measure the unwanted sideband.
Example: Single-sideband mixer



$$V_{out} = V_0 \sin\omega_{in}t \sin\omega_{LO}t + V_0 \cos\omega_{in}t \cos\omega_{LO}t$$

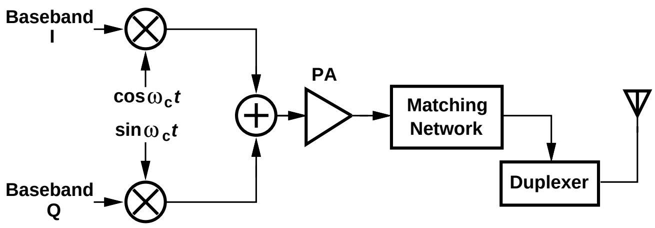
$= V_0 \cos(\omega_{LO} - \omega_{in})t$ **in ideal case**

Gain mismatch ε and phase mismatch θ:

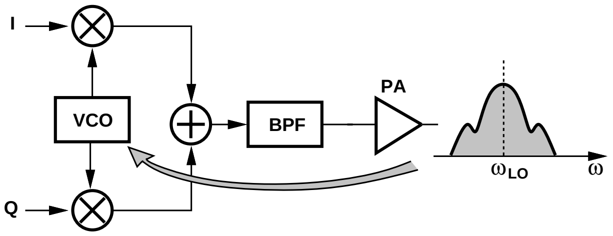
$$\frac{P^+}{P^-} = \frac{1-(1+\varepsilon)\cos\theta + \varepsilon}{1+(1+\varepsilon)\cos\theta + \varepsilon}$$

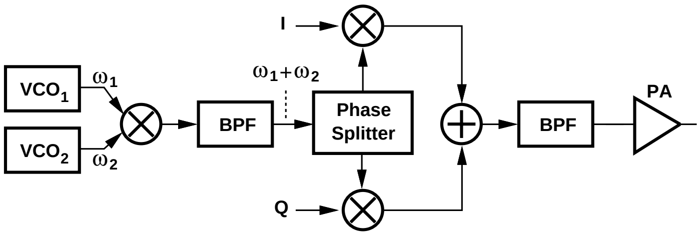
Direct Conversion Transmitters

If the transmitted carrier frequency is equal to the LO frequency, the architecture is called "direct conversion".



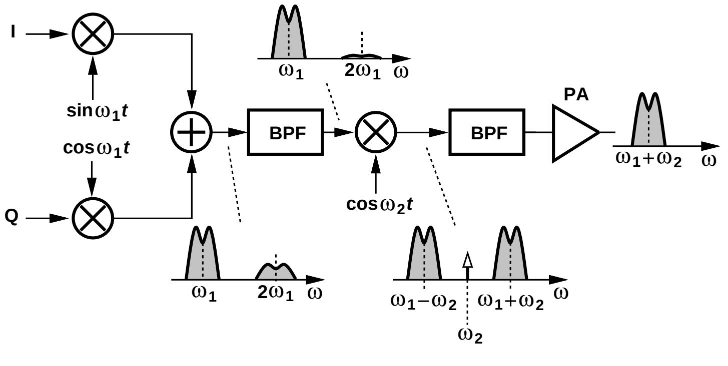
The major drawback is that the noise generated by the PA appears in the vicinity of the LO frequency, corruptiong the LO through a mechanism called "injection pulling" or "injection locking". → One remedy is to use "offset VCOs".





Two-Step Transmitters

To avoid LO pulling, we perform the upconversion in two steps:



The second BPF must reject the unwanted sideband.

The first BPF suppresses the harmonic of IF signal. 2nd BPF requires 50-60 dB suppression.

$\omega_1+\omega_2$ is at high freq and requires expensive off-chip device.

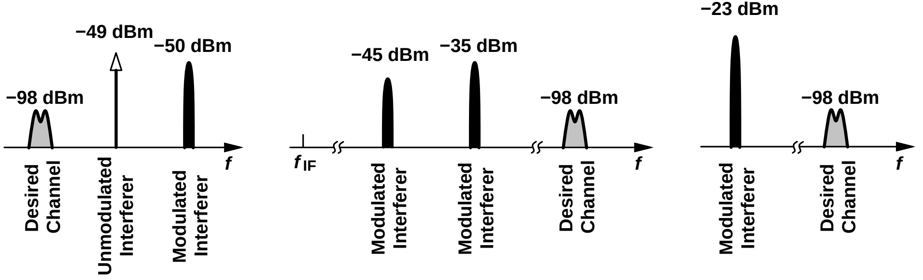
Transceiver Performance Tests

In most systems, a minimum detectable signal level (in the absence of interference is specified. The GSM standard, for example, requires an MDS of -102 dBm with an SNR of 9~12 dB.

$$P_{MDS} = -174dBm + NF\big|_{dB} + 10\log B + SNR_{\min}$$

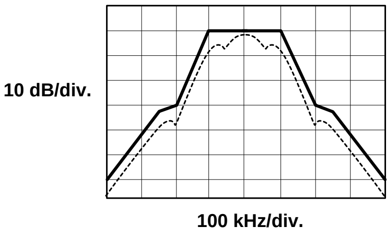
NF usually requires max NF 7~10 dB

Typical blocking test in GSM



(a) (b) (c)

Unwanted emission of GSM:



RF Building Blocks

Tai-Cheng Lee
Electrical Engineering/GIEE, NTU

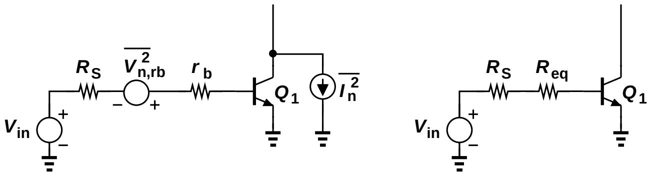
LNA

<u>Performance metrics</u>:

(1) NF~ 2dB	**(4) Input resistance ~ 50 Ω**
(2) IIP$_3$ ~ -10 dBm	**(5) Reverse Isolation ~ 20 dB**
(3) Gain ~ 15-20 dB	**(6) Power dissipation ~ 20 mW**

In heterodyne receivers, the LNA must drive a 50- Ω load.

<u>Example</u>:



At low frequencies,

$$\overline{v_n^2} = 4kT\left(r_b + \frac{1}{2g_m}\right) = 4kT\left(r_b + \frac{V_T}{2I_C}\right)$$

$$NF = 1 + \frac{\overline{v_n^2}}{4kTR_S} = 1 + \frac{R_{eq}}{R_S}, R_{eq} = r_b + \frac{1}{2g_m}$$

For NF=2dB, R_{eq}< 29 Ω

So why not design the antenna for a higher output resistance?

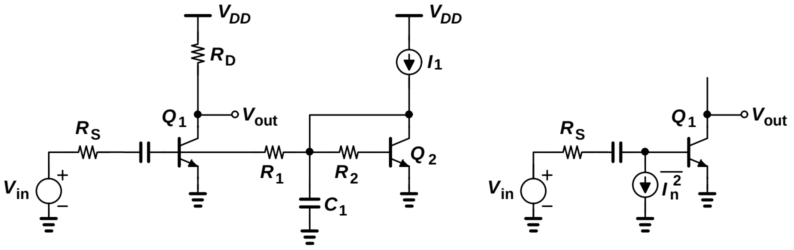
Stability of LNA

Stability of LNAs, especially in heterdyne architectures, is a major issue. The source and load impedance presented to the circuit vary from sample to sample, requiring "unconditional stability". A stability factor used to characterize circuits is

$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |D|^2}{2|S_{12}||S_{21}|} \qquad D = S_{11}S_{22} - S_{12}S_{21}$$

For unconditional stability, k>1. This must be guaranteed over <u>all</u> frequencies.

<u>Bipolar LNAs:</u>
Simple example



(a) (b)

Bipolar LNA (I)

Transistor Q_1 must be large enough and biased at a relatively high current to achieve a low noise. Increasing device size raises the input and output parasitic capacitances, and larger bias current increases the base shot noise and base-emitter diffusion capacitance.

If we include bias shot noise current: $NF = 1 + \frac{r_b}{R_s} + \frac{1}{2g_m R_s} +$

$$NF_{\min} \cong 1 + \sqrt{\frac{(1+2g_m r_b)}{\beta}} \qquad R_{S,opt} = \sqrt{\frac{\beta(1+2g_m r_b)}{g_m}} \neq 50\Omega$$

Important conclusion: conjugate matching does not necessarily yield minimum noise figure.

So, what do we do? → We still do 50-Ohm matching.

Bipolar LNA (II)

- **IIP_3 calculation:**

$$I_C = I_S \exp\left(\frac{V_{BE0} + V_{in}}{V_T}\right)$$

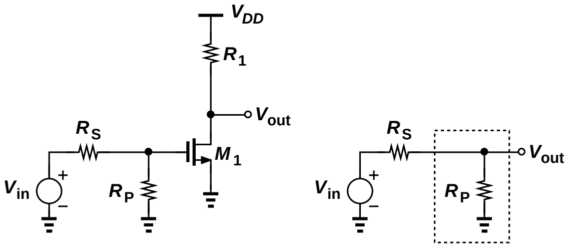
$$\approx I_S \exp\left(\frac{V_{BE0}}{V_T}\right)\left(1 + \frac{V_{in}}{V_T} + \frac{1}{2}\left(\frac{V_{in}}{V_T}\right)^2 + \frac{1}{6}\left(\frac{V_{in}}{V_T}\right)^3 + \cdots\right)$$

$$\Rightarrow \alpha_1 \cong \frac{1}{V_T}, \alpha_3 \cong \frac{1}{6}\frac{1}{V_T^3} \Rightarrow IIP_3 = \sqrt{\frac{4\alpha_1}{3\alpha_3}} = 2\sqrt{2}V_T = -12.7dBm$$

→ To achieve -10 dBm IIP3, another linearization is required.

MOS LNA

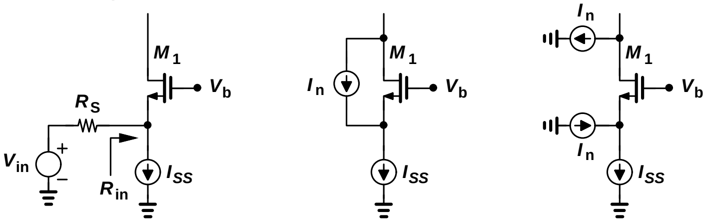
- **Common-source stage**



(a) (b)

$$\Rightarrow NF = 1 + \frac{R_S}{R_P}$$

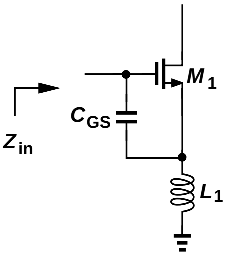
- **Common-gate stage**



(a) (b) (c)

$$\gamma = \begin{cases} 2/3, \text{ for long-channel MOSFET} \\ 1/2, \text{ for BJT} \end{cases} \qquad \Rightarrow NF = 1 + \gamma$$

Inductive Degeneration



$$\left(g_m \frac{I_X}{C_{GS}s} + I_X \right) L_1 s + \frac{I_X}{C_{GS}s} = V_X$$

$$\Rightarrow Z_{in} = \frac{g_m L_1}{C_{GS}} + L_1 s + \frac{1}{C_{GS}s}$$

- **Two problems:**

1. L_1 has significant loss if it is integrated.
2. L_1 has to be connected to a low-inductive ground.
3. The equivalent transconductance of M_1 may magnify the noise at the drain of M_1.

<u>Design examples</u>:

Downconversion Mixers (I)

Performance metrics:

(1) NF~ 8-12dB	(5) LO-RF isolation
(2) IIP_3 ~ 0~+5 dBm	(6) RF-LO isolation
(3) Gain ~ 10-15 dB	(7) LO-IF isolation.
(4) Input resistance ~ 50 Ω	(8) RF-IF isolation.

Voltage and power conversion gains:

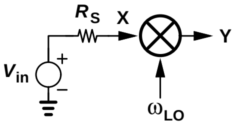
$$A_V = \frac{V_{IF}}{V_{RF}} \qquad A_P = \frac{P_{IF}}{P_{RF}}$$

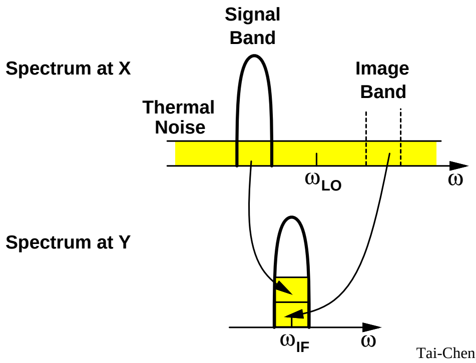
Note that A_v and A_p are not equal in dB because the source and load impedances are different.

DSB and SSB noise figure:

$$SNR_{in} = \frac{P_S(source)}{P_n(noise)}$$

$$SNR_{OUT} = \frac{P_S}{2P_n} \Rightarrow NF_{SSB} = 3dB$$





Downconversion Mixers (II)

(1) What are the sources of noise at IF
Because the noise from image band adds to desired signal after mixing → NF of mixer tends to be high.

(1) What is the spot noise density at the input?

$\rightarrow 4kTR_S$ **(DSB)**

(2) What is the spot noise density at the output?

$\rightarrow 8kTR_S$ **(SSB)**

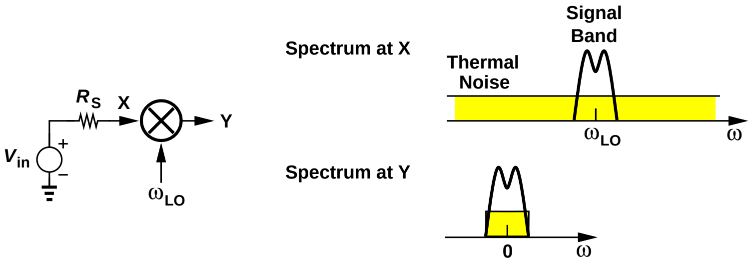
In summary, the noise figure of a (heterodyne) downconversion mixer is obtained by including the source noise power

- only in the RF band for calculating SNR_{in}.
- both in the RF band and the image band for the output SNR.

This is called "single-sideband" noise figure with the idea that the input signal is carried only in one band around LO frequency.

Downconversion Mixers (III)

- **SSB NF of a noiseless mixer:**



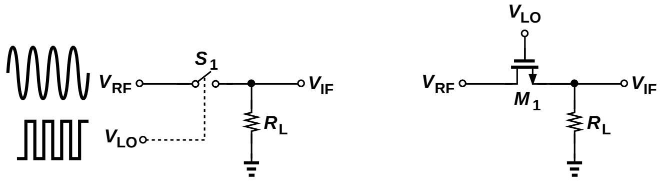
$$SNR_{in} = \frac{P_S}{P_n} \qquad SNR_{out} = \frac{P_S}{P_n} \qquad \Rightarrow NF_{SSB} = 1 = 0dB$$

The principle difficulty with NF of mixers is that typical noise measurement systems know nothing about the actual signal spectrum and hence assume DSB.

The result of this measurement is called the "double sideband" noise figure. If the input band is flat from RF to image, NF_{SSB}=2NF_{DDB}.(NF_{SSB}=NF_{DDB}+3dB)

Passive Mixers

- **Passive mixer:**



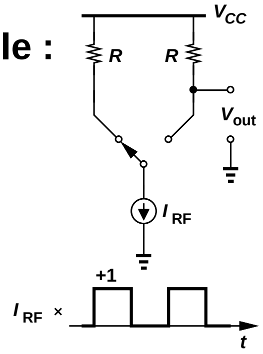
(a) (b)

If the LO signal has a 50% duty cycle :

$$V_{IF} = V_{RF} \cdot s(t)$$

Thus, the voltage conversion gain is equal to $\sin(\pi/2)/\pi = 1/\pi$

$$\Rightarrow \frac{V_{IF}}{V_{RF}} = \frac{1}{\pi}$$

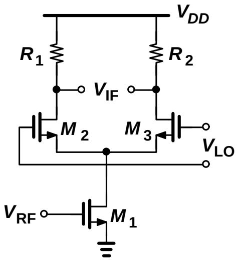


(a)

Which one is better: sinusoidal LO or square LO?
→ Square LO is better (1) Better conversion gain. (2) better NF.

Active Mixers

- **Active mixer:**



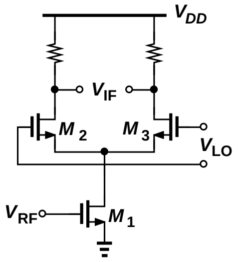
$$i_D = g_{m1} \cdot V_{RF} \Rightarrow V_{IF} = g_{m1} \cdot V_{RF} \cdot \frac{1}{\pi} \cdot 2R_D \Rightarrow \frac{V_{IF}}{V_{RF}} = \frac{2g_{m1}R_D}{\pi}$$

Which one is better: sinusoidal LO or square LO?

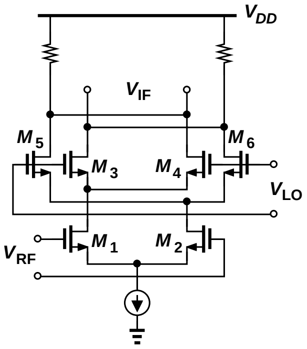
(1) Again, we want LO switch to be square wave to chop the signal very fast alternatively.
(2) From linearity issue, it is still better to turn the LO signal ON/OFF very fast.
(3) Make LO very large such that the center part of the sine wave look like square wave.

Single-Balanced and Double-Balanced Mixers

- **Single-balanced mixer:** **Double-balanced mixer**



(a)



(b)

Pros & Cons:

(1)Noise:	**Low**	**High**
(2) LO-IF feedthrough:	**Very bad**	**Small, because they cancel.**
(3) Even-order distortion:	**Bad**	**OK**

In either topologies, the output can be sensed as either a single-ended signal or a differential signal with differential output, we have:

- (1) higher gain (2) less RF-IF feedthrough (critical in homodyne) (3) potentially less noise. → so why doesn't everyone take the output differentially? → single-ended filter.

CMOS Mixer (I)

- **Most of design concepts and issues described for bipolar mixers apply to CMOS counterparts as well.**

An important difference is the required LO drive.

(a)

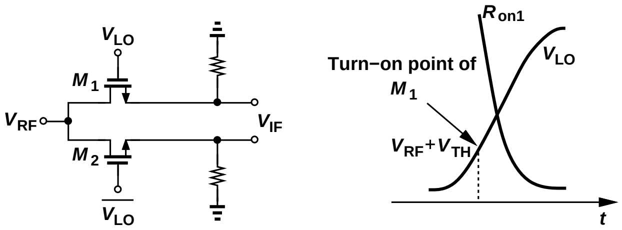
- A small overdrive leads to : lower conversion gain, higher noise, and even higher nonlinearity.
- For a given LO drive, the switching can be made mode abrupt by increasing the width of M_2 and M_3 or perhaps reducing their bias current.

CMOS Mixer (II)

- With an overdrive voltage of 300-400 mV in M_1, relatively high IP_3 can be achieved.

- **Passive Mixers**

$$\text{voltage gain} = \frac{2}{\pi}$$



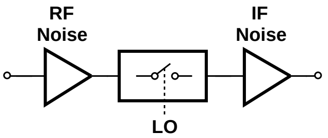
(a) (b)

With large LO drive, this circuit achieves a relatively high IP_3. It also consumes a small power.

BUT: - Loss “magnifies” noise of following stage.
- The following low-pass filter loads the RF input.
- Since *Ron* is chosen to be small, C_1 and C_2 are quite large.

Noise in Mixer (I)

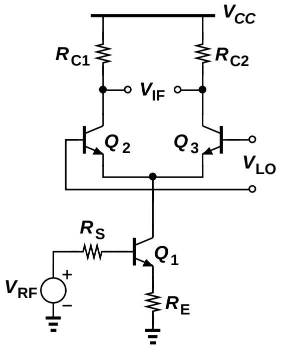
The time-variant and frequency translation in mixers make it difficult to calculate the NF. Conceptually:



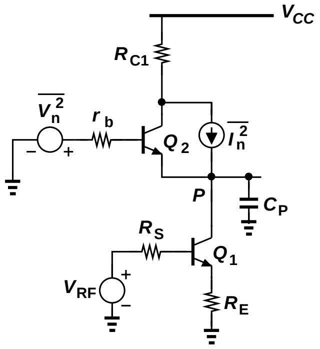
- **Qualitative analysis: (source of noise)**
  (1) RF path:r_{b1}, R_E and Q_1 shot noise.
  (2) IF path: R_C introduces noise.

How about noise of Q_2 and Q_3?

- Abrupt LO switching:
Cp provides finite impedance to GND. The RF noise of Q_2 is translated to IF due to LO switching.



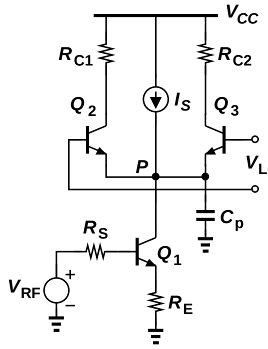
(a)



(b)

Noise in Mixer (II)

- Realistic LO: Q_2 and Q_3 are simultaneously on for part of the period, injecting noise to the output.
(How about noise of Q_1 during this time?) The shot noise of I_{C1} has less effect.



Remedies:
1. Large LO swings.
2. Low capacitance at node *P*.
3. Low base resistance in $Q_1 – Q_3$.
4. Low collector current in Q_2 and Q_3 .

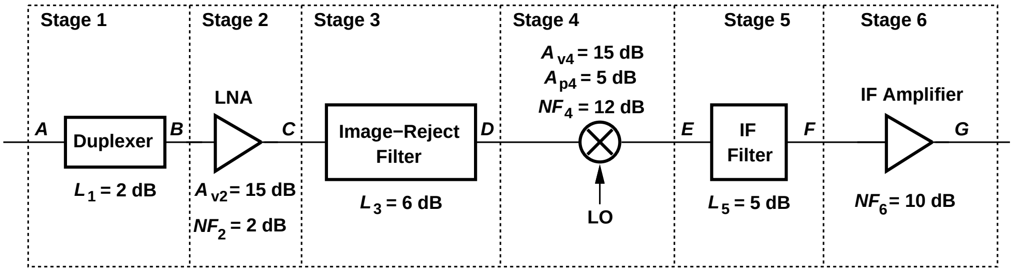
This technique, however increases the $1/g_m$ of Q_2 and Q_3 contributes noise through I_1.

Other considerations:
- The output thermal noise of LO increases the noise figure.

- If the mixer output is sensed in a single-ended form, then low-frequency noise also passes through the mixer.

Cascaded Stages (II)

- **Calculation of noise figure in a cascade of stages:**

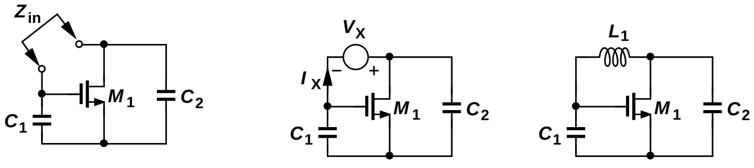


Level diagram corresponding to the cascade of the above figure:

	A	Duplexer	B	LNA	C	Image−Reject Filter	D	Mixer	E	IF Filter	F	IF Amplifier
Stage Gain (dB)												
Voltage		−2		15		−6		15		−5		
Power		−2		15		−6		5				
Cumulative Voltage Gain (dB)			−2		13		7		22		17	
Stage NF (dB)		2		2		6		12		5		10
Cumulative NF (dB)	8.79		6.79		20.1		14.1		15		10	
Stage IP_3		+100 dBm		−12 dBm		+100 dBm		+5 dBm		1000 V_{rms}		700 mV_{rms}
Cumulative IP_3	−10.6 dBm		−12.6 dBm		+11 dBm		+5 dBm		22.1 V_{rms}		700 mV_{rms}	

One-Port View of LC Oscillator

- **One-port representation of Colpitts and Hartley oscillator:**

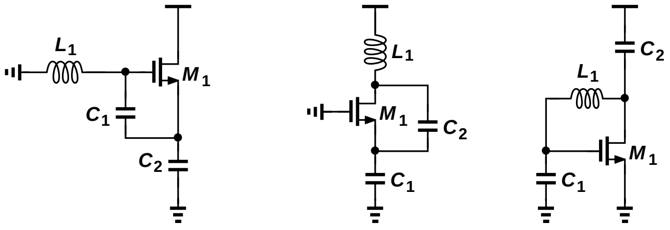


(a) (b) (b)

$$\frac{-I_X}{C_1 s} g_m + \left(\frac{-I_X}{C_1 s} + V_X\right) C_2 s = -I_X \quad \Rightarrow \frac{V_X}{I_X} = \frac{g_m}{C_1 C_2 s^2} + \frac{1}{C_1 s} + \frac{1}{C_2 s}$$

$$s = j\omega \Rightarrow -\frac{g_m}{C_1 C_2} + \left(\frac{1}{C_1} + \frac{1}{C_2}\right)\frac{1}{j\omega}$$

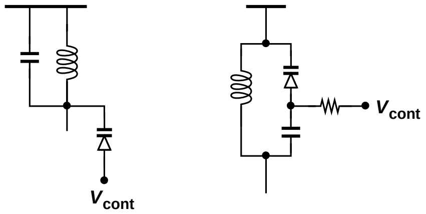
- **Three possible topologies for LC tank: (No ground is required In above analysis).**



(a) (b) (c)

Voltage-Controlled Oscillators (I)

- **Most of RF systems require “well-defined” steps for channel selection → VCO (voltage-controlled oscillator) is required.**
- **Though CCO (current-controlled oscillator) are also feasible, they are not widely used in RF systems because of difficulties in varying the value of high-*Q* storage elements by means of a current.**
- **How do we vary the frequency?**



The PN junction is reversed biased so the control voltage can tune the capacitance.

- **The VCO output frequency characteristics:**

$$\omega_{out} = \omega_{FR} + K_{VCO} V_{cont}$$

→ **The output of a sinusoidal VCO can be expressed as**

$$y(t) = A\cos(\omega_{FR} t + K_{VCO}\int_{-\infty}^{t} V_{cont}\,dt + \phi_0)$$

Voltage-Controlled Oscillators (II)

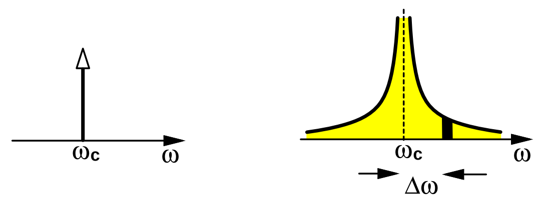
- **VCO is essentially a FM modulation. If** $V_{cont}(t) = V_m \cos\omega_m t \rightarrow$

$$y(t) = A\cos(\omega_{RF} t + \frac{K_{VCO}}{\omega_m} V_m \sin\omega_m t)$$

(1) We can use narrow-band approximation if $\left|\frac{K_{VCO}}{\omega_m} V_m\right| << 1$

(2) VCO has tendency to reject high-frequency noise.

- **Phase noise**



A periodic sinusoidal signal can be expressed as:

$x(t) = A\cos[\omega_c t + \phi_n(t)]$, **where** $\phi_n(t)$ **is a small random excess phase.**

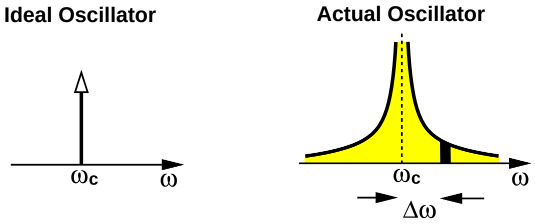
Phase Noise (I)

$x(t) = A\cos[\omega_c t + \phi_n(t)]$, **where** $\phi_n(t)$ **is a small random excess phase.**

$\phi_n(t)$ **is called "phase noise".**

If $\phi_n(t) << 1\text{rad} \rightarrow x(t) \approx A\cos\omega_c t - A\phi_n(t)$

→ **The spectrum of ϕ_n(t) is translated to around ω_c.**

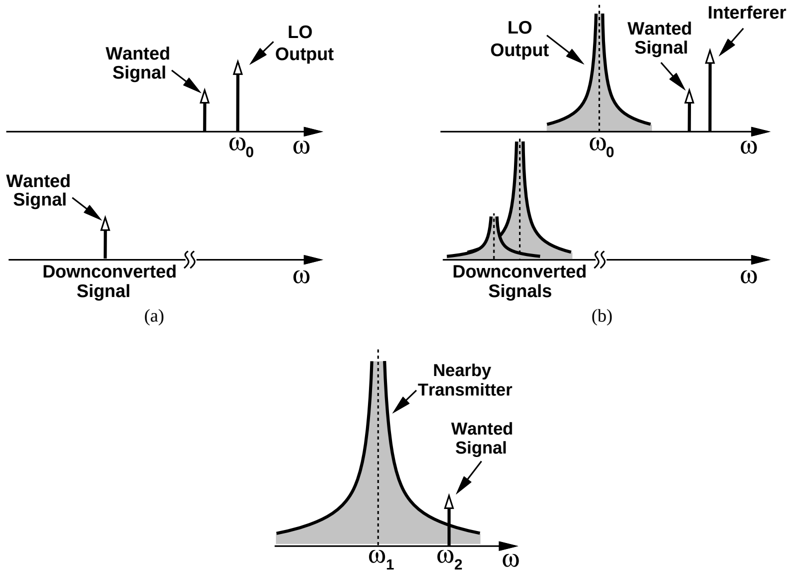


In RF applications, phase noise is usually characterized in the frequency domain. For an ideal sinusoidal oscillator operating at ω_c, the spectrum assumes the shape of an impulse, whereas for an actual oscillator, the spectrum exhibits "skirts" around the carrier frequency.

How do we quantify phase noise? (It has something to do with the resolution BW). → Noise power at an offset $\Delta\omega$ divided by average carrier power.

Phase Noise (II)

Effect of phase noise in RF communications:



(a) (b)

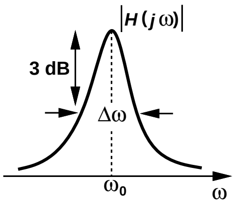
(c)

Reciprocal mixing: both wanted and interference signal are corrupted.

And are very close (few tens of KHz around GHz) → low phase noise is required. (-100~ -120 dBc/Hz at 100 kHZ offset).

Q of an Oscillator

- **Conventional definition of a bandpass systems:**



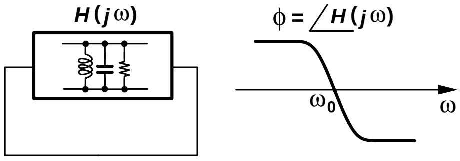
(1) 2π* (energy stored)/(energy loss)
(2) center frequency/3-dB bandwidth.

$$\frac{\omega_0}{\Delta\omega}$$

→ **Definition (1) (2) yields small value for LC oscillator.**

- **In a feedback system and the phase of the open-loop transfer function is examined:**

$$Q=\frac{\omega_0}{2}\left|\frac{d\phi}{d\omega}\right|$$

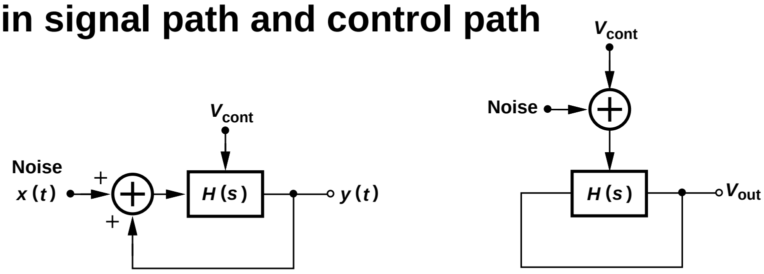


***Q*: How much the closed-loop system opposes variation in the frequency of oscillator.**

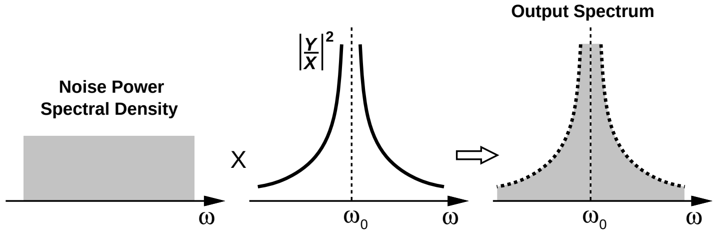
- **Loaded *Q*: the resistive component introduced by the transistor and any buffer stage following the oscillator. It is different from the tank *Q* and usually is smaller.**

Phase Noise Mechanisms (I)

- **Phase noise can be in signal path and control path**



☐ **Leeson's equation: noise in signal path**



$$\frac{Y(s)}{X(s)}=\frac{H(s)}{1-H(s)},H(j\omega)\approx H(j\omega_0)+\Delta\omega\frac{dH}{d\omega}$$

At oscillation frequency, $H(j\omega_0)=1$ **and** $\left|\Delta\omega\frac{dH}{d\omega}\right|<<1$

Phase Noise Mechanisms (II)

$$\frac{Y}{X}(\omega_0+\Delta\omega)\approx\frac{-1}{\Delta\omega\dfrac{dH}{d\omega}}\quad\rightarrow$$ **shaping function**

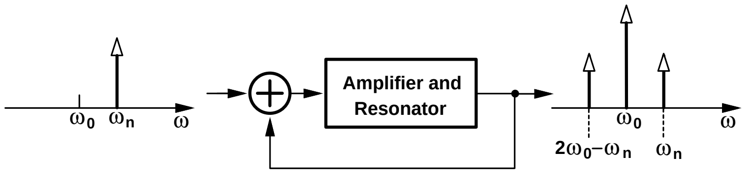
$$\left|\frac{Y}{X}(j\omega)\right|^2\approx\frac{1}{4Q^2}\left(\frac{\omega_0}{\Delta\omega}\right)^2$$

Three interesting properties of LC VCO (increasing *Q*):
(1) the noise shaping function becomes sharper.
(2) the power dissipation decreases.
(3) noise injected by active devices decreases.

Phase noise depends on
(1) Device noise $\propto\sqrt{I_{C1}}$
(2) amplitude. $\propto I_{C1}R_P$

Phase Noise Mechanisms (III)

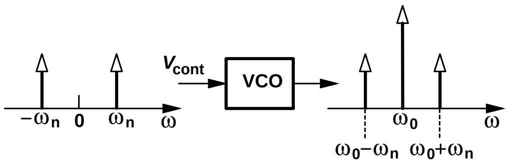
Noise folding: amplitude limiting in VCO fold the noise components.



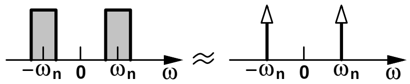
Modified Leeson's equation $$\Rightarrow\left|\frac{Y}{X}(j\omega)\right|^2\approx\frac{A}{4Q^2}\left(\frac{\omega_0}{\Delta\omega}\right)^2$$

→ **A is the actual loop small-signal gain. Around 2~3.**

- **Noise in control path: The noise on the control line can translate low-frequency noise components in the control path to the region around the carrier.**



(a)



(b)

$$\Rightarrow v_{out}(t)=A_0\cos\omega_0 t+\frac{A_0V_mK_{VCO}}{2\omega_m}\left[\cos(\omega_0+\omega_m)t-\cos(\omega_0-\omega_m)t\right]$$

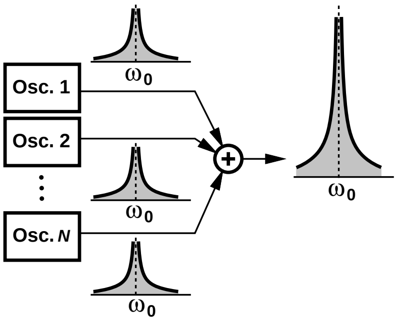
Phase Noise Mechanisms (IV)

The noise power with respect to the carrier is

$$\Rightarrow \frac{V_m^2\left(K_{VCO}/\omega_m\right)^2}{4}$$

$\rightarrow$ **1/f noise in the control path particularly detrimental.**

- **Noise power trade-off**



If the output voltages of N identical oscillators are added in phase:
(1) The total carrier power is *N*^{2}.
(2) The total noise power is *N*.
$\rightarrow$ **Total noise drops by *N*.**
Three parameters must be taken into account:
(1) center frequency ω_0
(2) power dissipation *P*
(3) offset frequency $\Delta\omega$:

$\Rightarrow \left(\frac{\omega_0}{\Delta\omega}\right)^2 / P$ **for fair comparison.**

Frequency Multiplication and Division

For a periodic sinusoid signal,

$x(t) = A\cos[\omega_c t + \phi_n(t)]$, **where $\phi_n(t)$ is a small random excess phase.**

$\rightarrow$ **A frequency divider simply divides the total phase by a factor of N**

$$x_{1/N}(t) = A\cos\left[\frac{\omega}{N}t + \frac{\phi_n(t)}{N}\right]$$

$\rightarrow$ **The magnitude of phase noise at a given frequency offset is:** $\left(\frac{1}{N}\right)$
(The phase noise power becomes : $\left(\frac{1}{N}\right)^2$

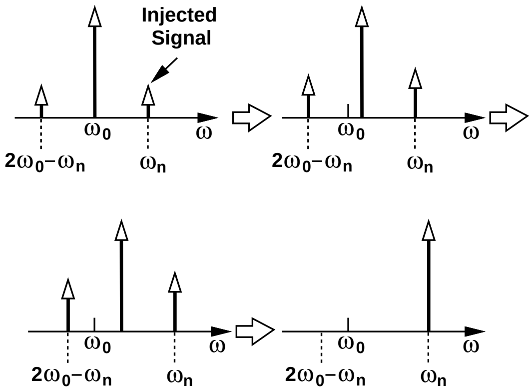
- **If the frequency is multiplied by a factor of *N***

$\rightarrow$ **The phase noise increases by a factor of *N*^{2}.**

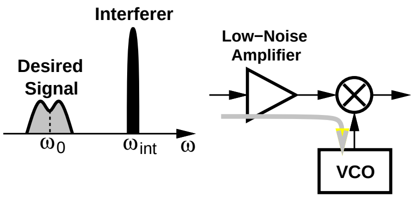
Oscillator Pulling and Pushing

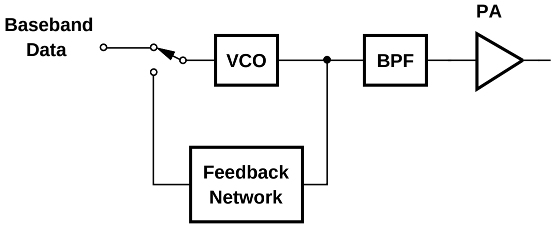
- **Injection pulling:**

If the injected component is close to the carrier frequency and has a comparable magnitude. → As the magnitude of the noise increases, the carrier frequency may shift toward the noise frequency and eventually "lock" to the frequency.



- **Injection pulling due to the large interference:**
- **Load pulling:**



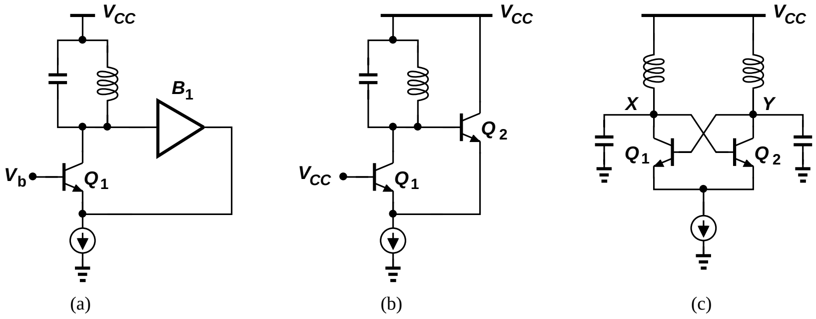


Negative-G_m Oscillators (I)

- **LC oscillator:**

(1) Low power supply → relatively "high" phase noise.
(2) Limited tuning range.
Note: smaller K_{VCO} → less "sensitive" to the noise of the control line.

- **Colpitts and Hartley oscillators with "active feedback"**



(a) (b) (c)

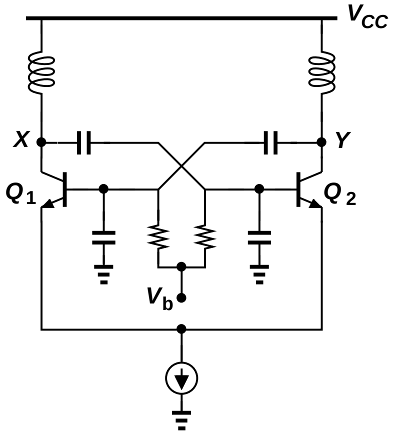
→ What is the small-signal impedance of Q_1 and Q_2? $-\frac{2}{g_m}$

Negative-G_m Oscillators (II)

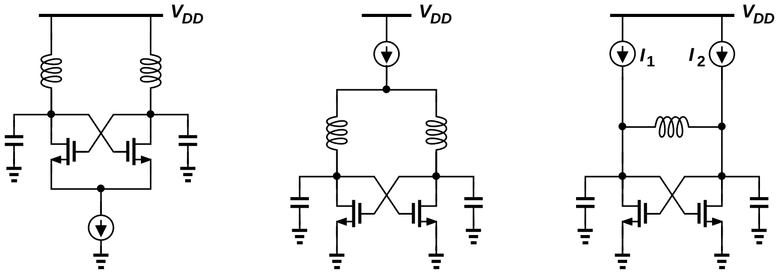
- **LC oscillator:**

  → To avoid Q_1 and Q_2 operates at heavy saturation, a capacitive feedback circuits can alleviate the saturation problem.

  → C_1 and C_2 capacitive division.



- **MOS LC oscillator:**



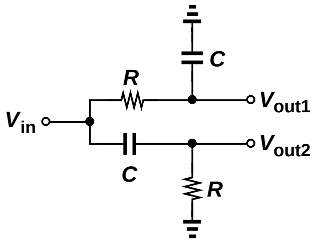
(a) (b) (c)

Quadrature Signal Generation (I)

- **Applications:**

(1) Quadrature LO
(2) 90^o phase shift in image-reject RXs.

- **RC-CR network:**



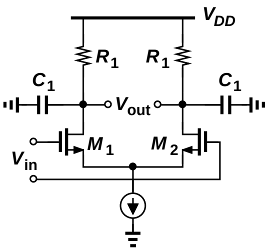
Mismatches introduce phase imbalance and absolute errors cause gain imbalance.

For LO signals, we can try to equalize the amplitude by limiting stage (limiting amplifier or limiter).

What’s wrong with different amplitude in quadrature signal?
→ One switch change faster than the other one → cause different conversion gain. →Not enough image rejection ratio.

Quadrature Signal Generation (II)

- **Limiting stage problem:**
(AM/PM conversion)



(1) If V_{in} is a small sinusoid, the phase shift is equal to
→ $-\tan^{-1}\omega R_1C_1$

(2) If V_{in} is a large sinusoid, the delay is
→ **the delay is** $R_1C_1\ln 2$

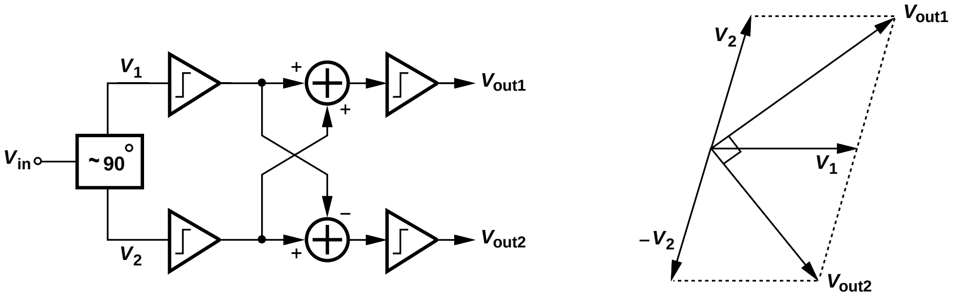
The key point here is that the difference in amplitudes translates to phase imbalance. $\frac{\tan^{-1}\omega R_1C_1}{\omega} > R_1C_1\ln 2$

- **The mismatch in RC/CR network creates the phase error:**

- **In the RC-CR network, harmonics of the input can also introduce phase and gain mismatch.**

Havens' Technique (I)

- **Koullias, ISSCC 93**



(a) (b)

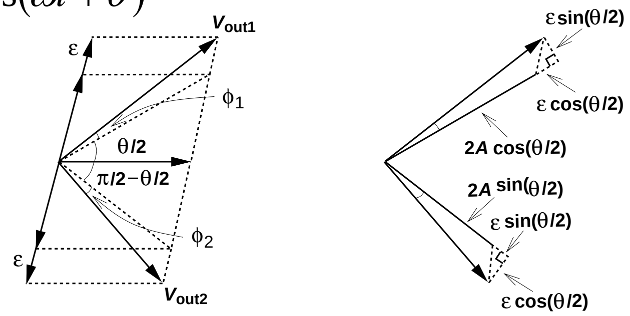
- **If V_1 and V_2 have mismatch in amplitude and phase:**

$$V_1(t) = A\cos\omega t, V_2(t) = (A+\varepsilon)\cos(\omega t+\theta)$$

$$\phi_1 + \phi_2 \cong \frac{\varepsilon}{A}\frac{1}{\sin\theta}$$

$\Rightarrow 1\%$ **amplitude mismatch,**

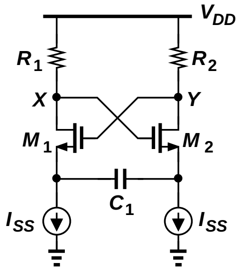
0.6° phase error.

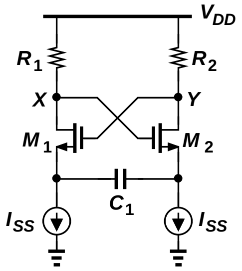


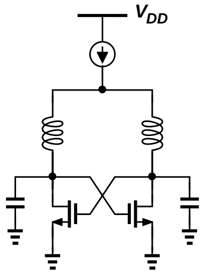
(a) (b)

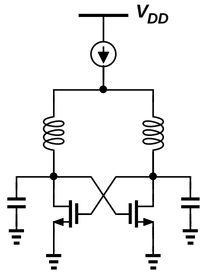
Quadrature VCO

- **Coupled Oscillators (Verhoeven, JSSC, July 92)**





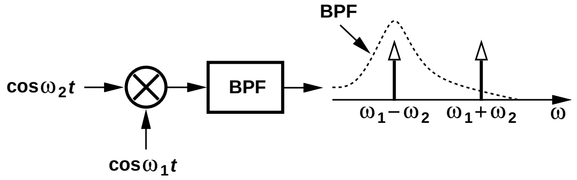




Rofougaran etal, ISSCC 95

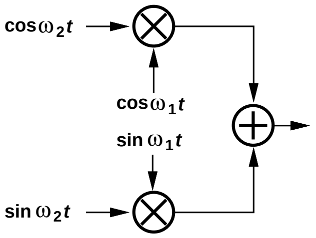
Single-Sideband Generation

- **Transceivers often require the addition or subtraction of the output frequencies of two or more LOs.**



(a)

What if ω_1 is much smaller than ω_2 ?
BPF must have very sharp corner frequency.

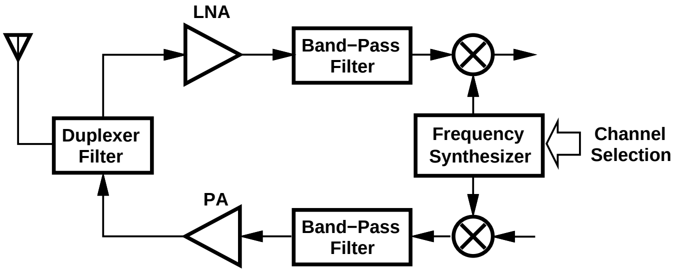


(b)

Mixers are usually designed such that LO port experiences abrupt switching. Thus, LO port is so nonlinear that the RF signal is multiplies by a rectangular waveform.
→ Output has rich components of cross-products.

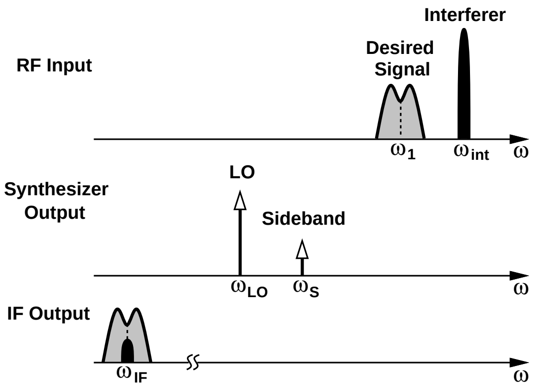
General Considerations

- How do we generate 30 kHz spacing around 900 MHz or 1.8 GHz in the following transceiver?



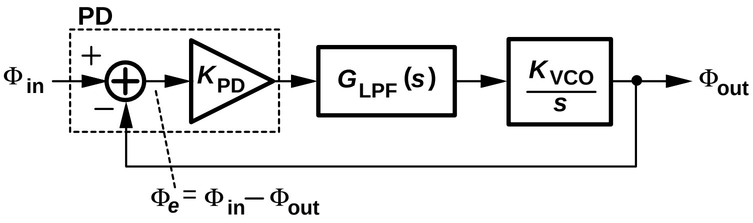
- Three major considerations for RF frequency synthesizers

(1) Phase noise.
(2) Spurs.
(3) Lock time.



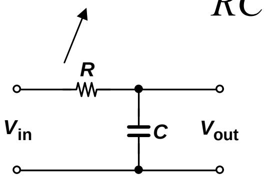
Dynamics of Simple PLL (I)

Linear model of the PLL



Φ_{in} and Φ_{out} denote the excess phases of the input and output waveform. For example, if the total input phase experiences a step change, ϕ_1 $u(t)$, then $\Phi_{in}(s)=\phi_1/s$.

$$\omega_{LPF} = -\frac{1}{RC}$$



The open loop transfer function is given by

$$H(s)\Big|_{open} = \frac{\Phi_{out}}{\Phi_{in}}(s)\Bigg|_{open} = K_{PD} \cdot \frac{1}{1+\frac{s}{\omega_{LPF}}} \cdot \frac{K_{VCO}}{s}$$

It only contains one pole at $s=-\omega_{LPF}$ and another one at origin, the system is called "Type I.":

Dynamics of Simple PLL (II)

The closed loop transfer function of Type I PLL is

$$H(s)\big|_{closed}=\frac{K_{PD}K_{VCO}}{\frac{s^2}{\omega_{LPF}}+s+K_{PD}K_{VCO}}$$

Recall that the instantaneous frequency of a waveform is equal to the time derivative of the phase: $\omega=\frac{d\phi}{dt}$

What is $\frac{\omega_{out}}{\omega_{in}}(s)=\frac{K_{PD}K_{VCO}}{\frac{s^2}{\omega_{LPF}}+s+K_{PD}K_{VCO}}$

The above closed loop transfer function can be simplified as:

$$H(s)\big|_{closed}=\frac{\omega_n{}^2}{s^2+2\xi\omega_n s+\omega_n{}^2}$$

$$\Rightarrow \omega_n=\sqrt{\omega_{LPF}K_{PD}K_{VCO}}$$

$$\xi=\frac{1}{2}\sqrt{\frac{\omega_{LPF}}{K_{PD}K_{VCO}}}$$

ω_n is the natural frequency and ζ is the damping ratio.

Dynamics of Simple PLL (III)

The two poles of the closed-loop system are given by

$$\begin{aligned}s_{1,2}&=-\xi\omega_n\pm\sqrt{(\xi^2-1)\omega_n{}^2}\\&=(-\xi\ \pm\sqrt{(\xi^2-1)})\omega_n\end{aligned}$$

If ζ>1, both poles are real, the system is underdamped and the transient contains two exponentials with time constants *$1/s_1$* and *$1/s_2$*. On the other hand, if ζ<1, the poles are complex and The response to an input frequency step *$\omega_{in}=\Delta\omega u(t)$* is equal to

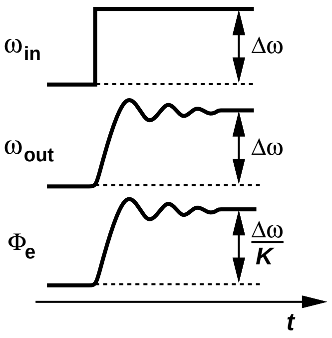
$$\omega_{out}(t)=\left\{1-e^{-\xi\omega_n t}[\cos(\omega_n\sqrt{(\xi^2-1)}t)+\frac{\xi}{\sqrt{1-\xi^2}}\sin(\omega_n\sqrt{(\xi^2-1)}t)\right\}\Delta\omega u(t)$$

$$=\left[1-\frac{1}{\sqrt{1-\xi^2}}e^{-\xi\omega_n t}\sin\omega_n\sqrt{(\xi^2-1)}t+\theta)\right]\Delta\omega u(t)$$

Decay time constant is equal to $(\xi\omega_n)^{-1}=\left(\frac{1}{2}\omega_{LPF}\right)^{-1}$

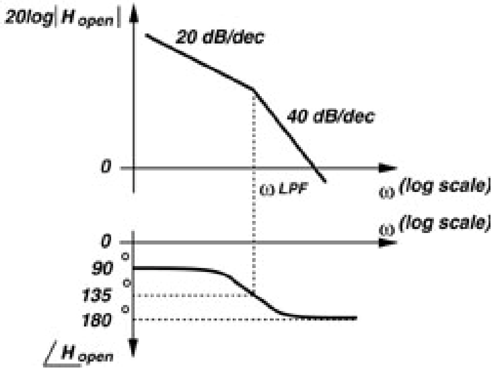
Dynamics of Simple PLL (IV)

The settling behavior of the type I PLL



The choice of ζ entails trades-off. First, ω_{LPF} is reduced to minimize the ripple on the control voltage, the stability degrades. Second, phase error and ζ is inversely proportional to $K_{PD}K_{VCO}$.

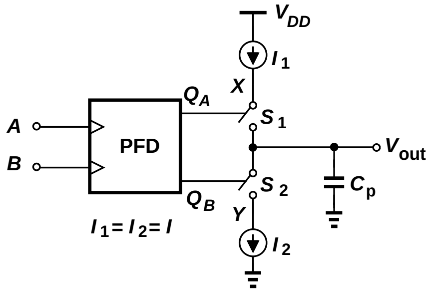
The bode plot of the loop gain:

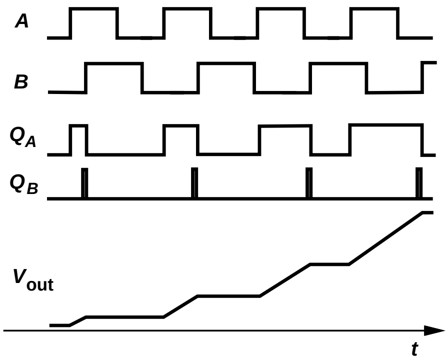


What happens if a higher $K_{PD}K_{VCO}$ is chosen to minimize ϕ_{in}-ϕ_{out} ?
→ The curve is up. → Unity-gain crossover shifts right. → Less phase margin. → Less stable.

Charged-Pump PLL (I)

Phase-detector with charge-pumped circuit: A leads B, then Q_A continues to produce pulses and V_{out} rises steadily. Called UP and DOWN currents, respectively, I_1 and I_2 are nominally equal.





$$V_{out}(t) = \frac{I_p}{2\pi C_p} t \cdot \phi_0 u(t)$$

$$h(t) = \frac{I_p}{2\pi C_p} u(t)$$

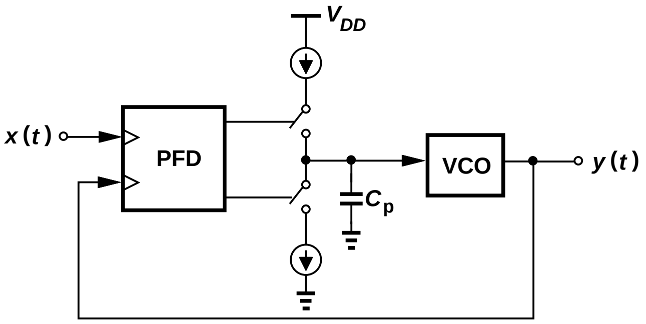
$$\frac{V_{out}}{\Delta\phi}(s) = \frac{I_p}{2\pi C_p} \cdot \frac{1}{s}$$

$$\left.\frac{\phi_{out}}{\phi_{in}}(s)\right|_{open} = \frac{I_p}{2\pi C_p} \cdot \frac{K_{VCO}}{s^2}$$

$$H(s)|_{close} = \frac{\frac{I_p K_{VCO}}{2\pi C_p}}{s^2 + \frac{I_p K_{VCO}}{2\pi C_p}}$$

Charged-Pump PLL (II)

A type II PLL→ It's unstable because two poles occur at origin.

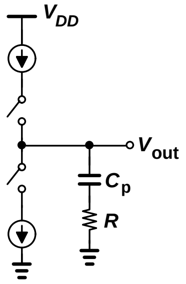


The gain of PFD/CP combination is infinite, i.e., a nonzero (deterministic)difference between ϕ_{in} and ϕ_{out} leads to indefinite charge buildup on C_p. → The input phase error must be exactly zero in ideal case.

If $\phi_{in} - \phi_{out}$ drops to zero, the PFD simply produces $Q_A = Q_B = 0$. The charge pump thus remains idle and C_p sustains a constant control voltage. What happens? VCO begins to drift and PLL is back to work.

Charged-Pump PLL (III)

Adding a zero in the loop transmission to improve the phase margin

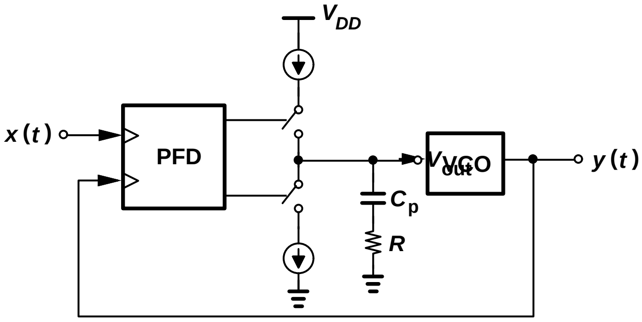


$$\frac{V_{out}}{\Delta\phi}(s) = \frac{I_p}{2\pi} \cdot (R_p + \frac{1}{C_p s})$$

$$\left.\frac{\Phi_{out}}{\Phi_{in}}(s)\right|_{open} = \frac{I_p}{2\pi}(R_p + \frac{1}{C_p s})\frac{K_{VCO}}{s}$$

The Dynamics of Type II PLL (I)

A complete block diagram for type II PLL



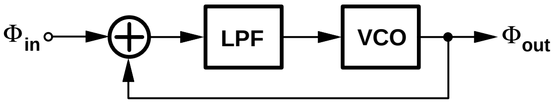
$$H(s)=\frac{\frac{I_pK_{VCO}}{2\pi C_p}(R_pC_ps+1)}{s^2+\frac{I_pK_{VCO}}{2\pi}R_ps+\frac{I_pK_{VCO}}{2\pi C_p}}\rightarrow \textbf{zero } s_z=-1/(R_pC_p)$$

$$\omega_n=\sqrt{\frac{I_pK_{VCO}}{2\pi C_P}} \qquad \xi=\frac{R_p}{2}\sqrt{\frac{I_pC_pK_{VCO}}{2\pi}}$$

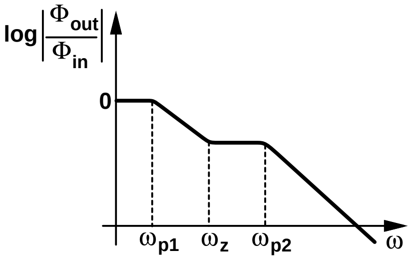
time constant $1/(\xi\omega_p)=\dfrac{4\pi}{R_pI_pK_{VCO}}$

Phase Noise in PLL

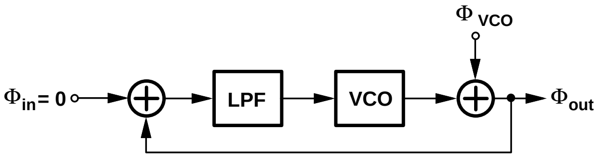
- **Phase noise from input**



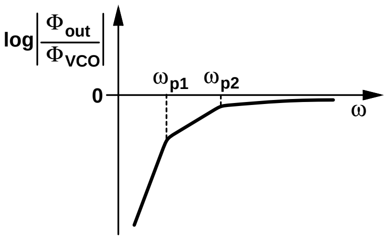
$$\frac{\phi_{out}}{\phi_{VCO}}(s)=\frac{\omega_n^{\ 2}(1+s/\omega_Z)}{s^2+2\xi\omega_ns+\omega_n^{\ 2}}$$



- **Phase noise of VCO**

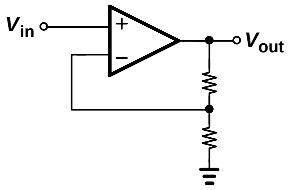


$$\frac{\phi_{out}}{\phi_{VCO}}(s)=\frac{s^2}{s^2+2\xi\omega_ns+\omega_n^{\ 2}}$$

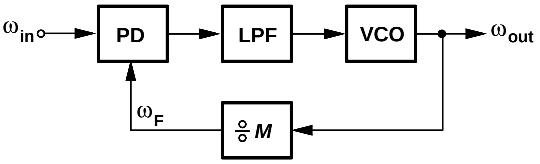


Frequency Multiplication

Frequency multiplication and synthesis: for example, 30 kHz from 900 MHz to 925 MHz.



(a)



(b)

Design parameters:

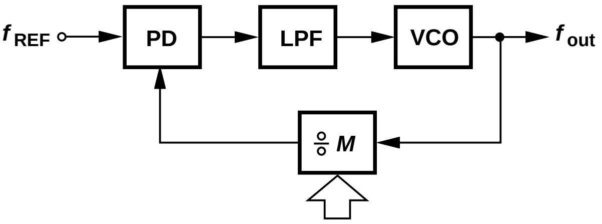
$$H(s)=\frac{\frac{I_pK_{VCO}}{2\pi C_p}(R_pC_ps+1)}{s^2+\frac{I_p}{2\pi}\frac{K_{VCO}}{M}R_ps+\frac{I_p}{2\pi C_p}\frac{K_{VCO}}{M}}$$

$$\omega_{out}=\frac{\omega_0}{M}+\frac{K_{VCO}}{M}V_{cont}$$

$$\omega_n=\sqrt{\frac{I_p}{2\pi C_P}\frac{K_{VCO}}{M}}\qquad \xi=\frac{R_p}{2}\sqrt{\frac{I_pC_p}{2\pi}\frac{K_{VCO}}{M}}$$

Integer-*N* RF Synthesizer Architectures

Issues:
(1) Reference spurs
(2) Lock time
(3) Buffering between VCO and divider
(4) Divider



Modulus Selection

What is the relationship between f_{out} and f_{REF}?

$f_{out}=Mf_{REF}$, **but in reality, we want** $f_{out}=f_0+kf_{CH}$

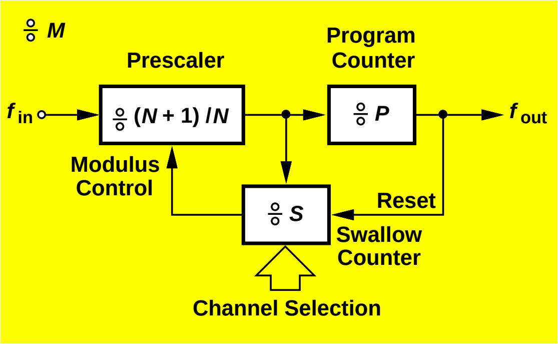
$$\begin{cases}Mf_{REF}=f_0\\(M+1)f_{REF}=f_0+f_{CH}\end{cases}\Rightarrow f_{CH}=f_{REF}$$

$$\Rightarrow f_{out}=M_Lf_{REF}+kf_{REF}\Rightarrow M=M_L+k$$

Integer-*N* Architectures (I)

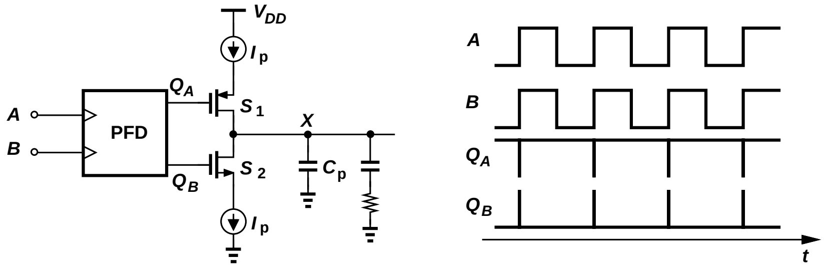
- **Pulse-swallow counter:**

(1) Prescaler divides by N or N+1.
(2) Program counter always divides by P.
(3) The swallow counter can be programmed by divided ratio.



→ **What is the relationship between f_{out} and f_{REF}?** $f_{out} = f_{REF} /(NP+S)$

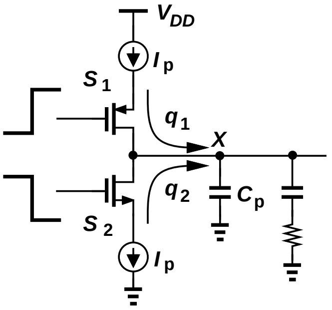
- **Reference spurs: the input reference frequency modulates the VCO, generating around the carrier.**



Integer-*N* Architectures (II)

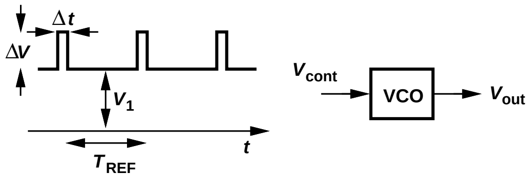
- **The charge injection mismatch of the charge pump circuits:**

$$v_{out} = v_0 \cos\left(\omega_{FR} t + K_{VCO}\int g(t)dt + K_{VCO}\int v_1 dt\right)$$



- **Estimation of VCO modulation due to charge pump feedthrough:**

$$g(t) = \frac{\Delta V \Delta t}{T_{REF}} + \sum_{n \neq 0} a_n \cos\left(n\omega_{REF} t + \theta_n\right)$$



$$\Rightarrow v_{out} = V_0 \cos\left(\omega_{FR} + \frac{\Delta V \Delta t}{T_{REF}} K_{VCO} + K_{VCO} V_1\right)t$$

$$- K_{VCO}\left[V_0 \sum_{n \neq 0} \frac{a_n}{n\omega_{REF}} \sin\left(n\omega_{REF} + \theta_n\right)\right] \sin\left(\omega_{FR} + \frac{\Delta V \Delta t}{T_{REF}} K_{VCO} + K_{VCO} V_1\right)t$$

- **Sideband spurs at** $\omega_{FR} \pm n\omega_{REF}$

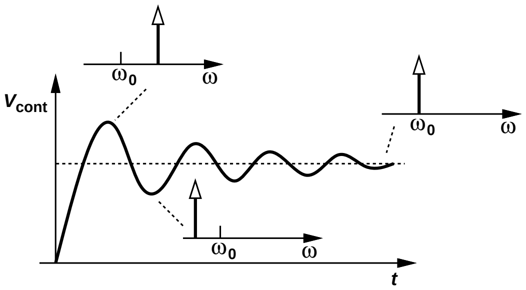
Integer-*N* Architectures (III)

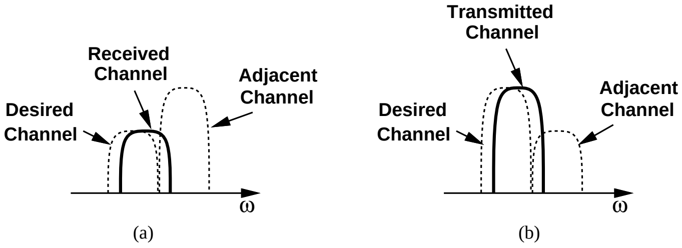
- **Loop bandwidth: For GSM, local oscillator needs to generate 200-kHz channel spacing around 900 MHz. → loop bandwidth is usually one tenths of f_{REF}.**

→ loop BW~ 20K, time constant= 50μs, settling time= 500μs

- **The definition of lock: when the phase difference between input and feedback drops to acceptably low value.**
  (for retimed or edge alignment application)

- **The effect of synthesizer settling to received and transmitted path**



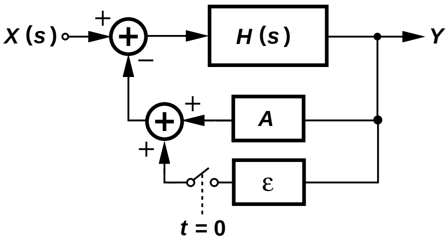


(a)

(b)

Integer-*N* Architectures (IV)

- **The modulus change in integer-*N* architecture.**



$$\frac{Y}{X}(s)=\frac{H(s)}{1+\left(A+\varepsilon\right)H(s)}\approx\frac{H(s)}{1+AH(s)}\cdot\frac{1}{1+\varepsilon/A}$$

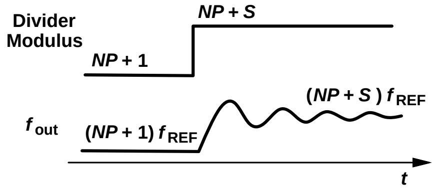
$$=\frac{H(s)}{1+AH(s)}\left(1-\frac{\varepsilon}{A}\right)X(s)$$

- **The worst case settling for integer-*N* architecture would happen when the modulus ratio changes from *(NP+1)* f_{REF} to *(NP+S)* f_{REF}**

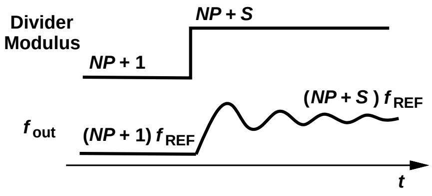
→ The feedback factor changes

→ a small change in feedback is equivalent to a step response from

$$x(t)\rightarrow\left(1-\frac{\varepsilon}{A}\right)x(t)$$



Integer-*N* Architectures (V)



→ **The settling time:**
Changing divide ratio from *M* →*M+k*
If *k<<M*
→ **Input frequency change from f_{REF} to (1+k/M) f_{REF}**

$$f_{out} = Mf_{REF} + \left[1 - \frac{1}{\sqrt{1-\xi^2}} e^{-\xi\omega_n t} \sin\omega_n\sqrt{(\xi^2-1)}t + \sin^{-1}\sqrt{1-\xi^2})\right]u(t)$$

$\Rightarrow$ **settle to** $(1\pm\alpha)(M+k)f_{REF}$

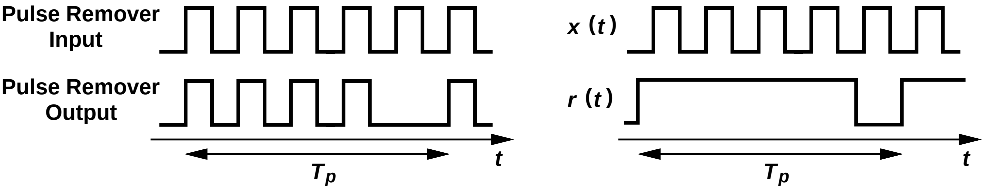
$$t_S \approx \frac{1}{\xi\omega_n}\ln\frac{k}{M|\alpha|\sqrt{1-\xi^2}}$$

- **Phase noise: Limited loop bandwidth results in higher close-in phase noise at output. For example, if the loop bandwidth of GSM system is 20 kHz → phase noise components at frequency offsets greater than a few kilohertz experience little attenuation. For CMOS implementation, *1/f* noise corner is higher than 20 kHz.**

Fractional-*N* Architectures (I)

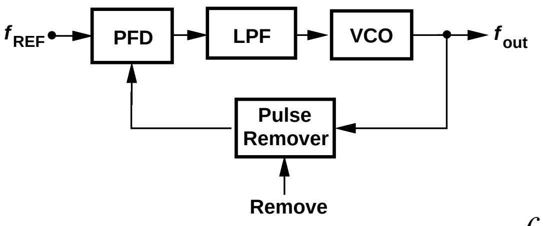
- **To resolve the limited bandwidth of integer-*N* architecture. What if we can generate “fraction” modulus?**

- **The “average” frequency:**

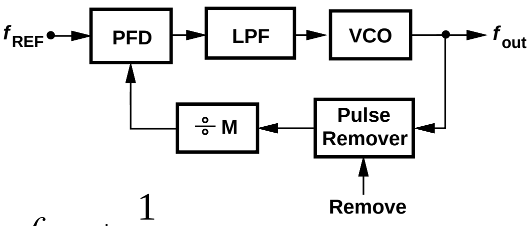


(a) (b)

- **A simple fractional-*N* architecture:**



(a)

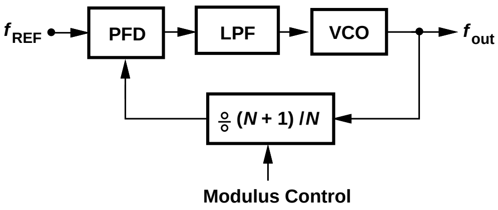


(b)

$$f_{out} = f_{REF} + \frac{1}{T_P}$$

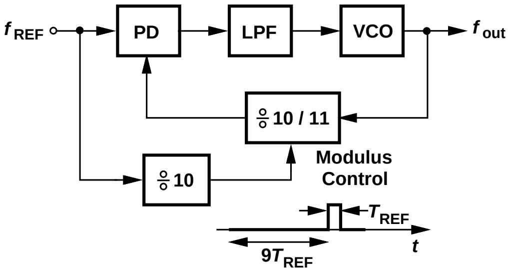
Fractional-*N* Architectures (II)

- **Modern implementation of fractional-*N* synthesizer:**



If we divides by *N* for *A* output pulses and *N+1* for *B* output pulses, → the equivalent divide ratio= $(A+B)/\left[\frac{A}{N}+\frac{B}{N+1}\right]$

- **Example:**



$f_{REF} = 1MHz$

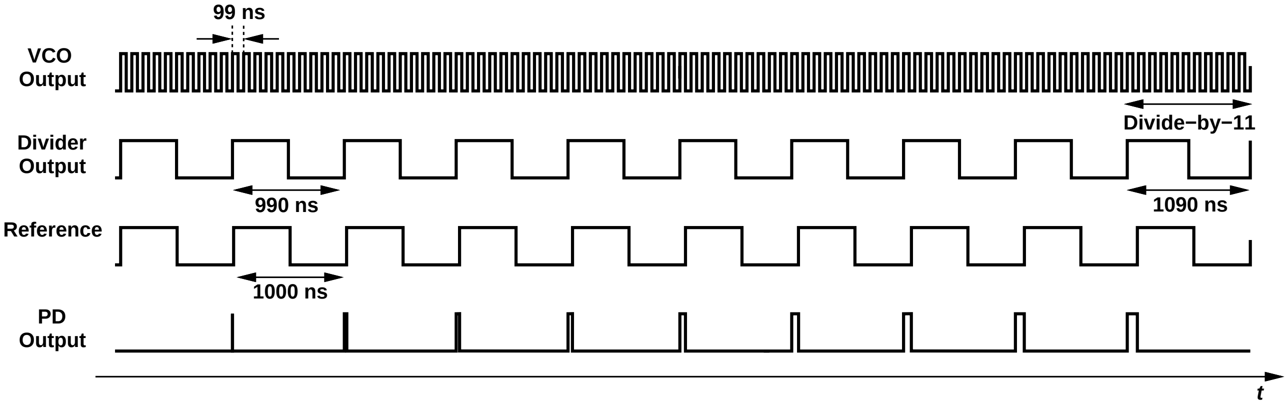
9 cycles for 10, and 1 cycle for 11 → $(9*10+11)/10 = 10.1$

- **The input frequency of fractional-*N* synthesizer can be in the range of MHz or tens of MHz → BW~ MHz**

(1) fast settling time. (2) Better close-in VCO noise.

Fractional Spurs

- **Effect of unequal instantaneous frequencies in a fractional-*N* synthesizers.**

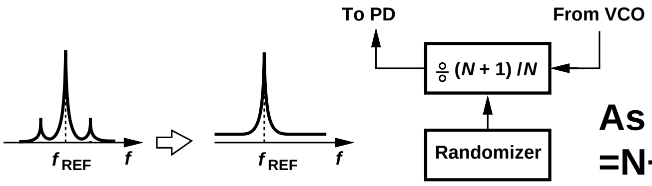


- **Fractional compensation:**

We can inject another current pulse with the same width but different polarity → It can be cancelled.

Σ-Δ Fractional-N Synthesizer (I)

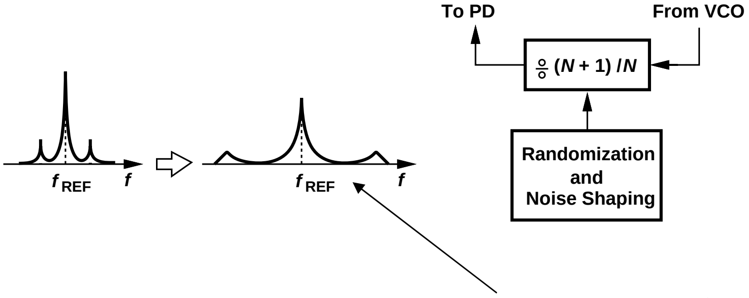
- Randomize the modulus but the "AVERAGE" modulus



As long as the average =N+α

→ The idea is to randomize the frequency divider such that the average of the modulus is equal to N+α, where 0<α<1.

- Noise shaping in modulus control



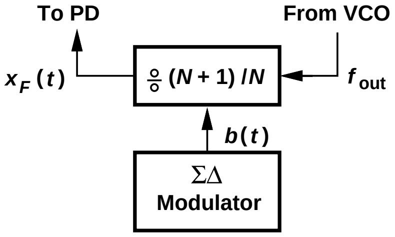
Null low-frequency noise

Σ-Δ Fractional-N Synthesizer (II)

- The basic concept of Σ-Δ noise shaping:

(1) Oversampling "samples" slow data for several times and uses its average to "estimate" it.

(2) The quantization noise in the "low-pass" feedback loop is pushed from low frequency toward high frequency.



The instantaneous division ratio can be written as $N + b(t)$

→ The instantaneous frequency of $x_F(t)$

$$f_F(t) = f_{out} / [N + b(t)]$$

$E[b(t)] = \alpha$ **, and the quantization noise *q(t)***

$$\rightarrow f_F(t) = f_{out} / [N + \alpha + q(t)]$$

$$\rightarrow n_F(t) = f_F(t) - \frac{f_{out}}{N+\alpha} = -\frac{f_{out}}{N+\alpha} \cdot \frac{q(t)}{N+\alpha+q(t)} \approx \frac{f_{out}}{N+\alpha} \frac{q(t)}{N}$$

$$\rightarrow S_{nf}(f) = \frac{f_{OUT}^2}{(N+\alpha)^2} \frac{|Q(f)|^2}{N^2}$$

Frequency Divider (I)

- **Design considerations:**

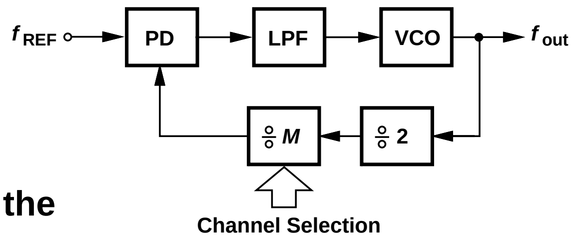
(1) power
(2) speed
(3) phase noise

- **Divide-by-2 circuit in PLL:**

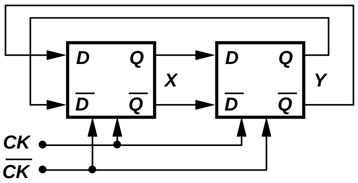
→ What happens to f_{REF}?

$$f_{out} = 2Mf_{REF} = M \cdot 2 \cdot \frac{f_{CH}}{2}$$

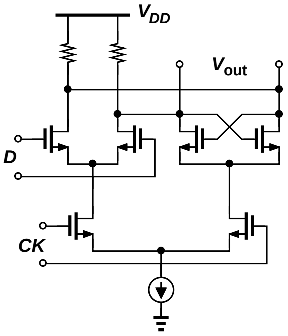
$$f_{REF} = \frac{f_{CH}}{2} \Rightarrow \text{channel spur is inside the close-in phase noise.}$$



- **Divide-by-2 circuit**



(a)

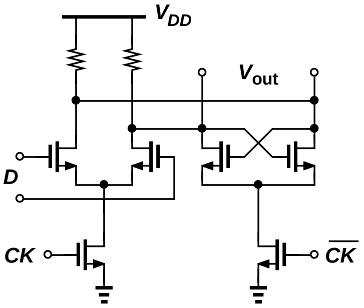


(b)

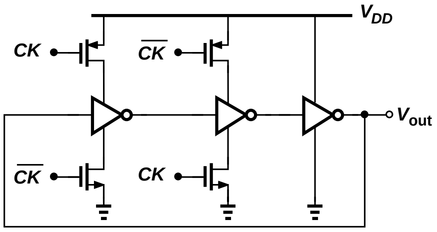
Frequency Divider (II)

- **MOS divide-by-2 circuit:**

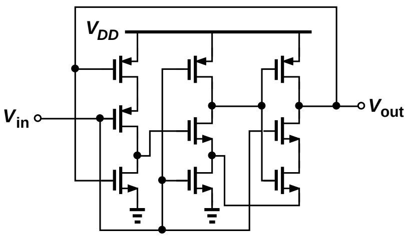
→ What is the output common-mode voltage?
(1) Preferable, $V_{out,CM}$=$V_{in,CM}$
(2) No current source.
(3) very high speed.



- **MOS divide-by-2 circuit for dynamic inverter and TSPC:**



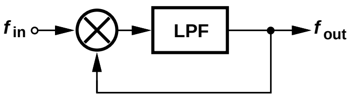
(a)



(b)

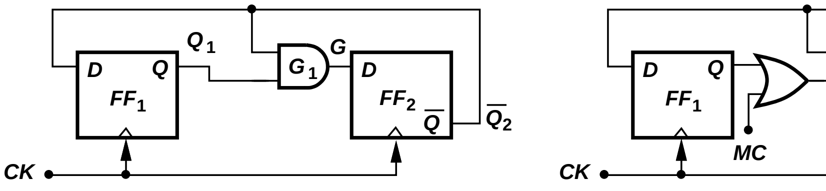
- **Miller divider:**

$$f_{in} - f_{OUT} = f_{OUT} \Rightarrow f_{OUT} = \frac{f_{in}}{2}$$



Dual-Modulus Dividers (I)

- Divide-by-3 circuits and divide-by-2/3 circuit:



(a) (b)

$$Q_1\overline{Q_2} = \{(01),(11),(10)\}$$

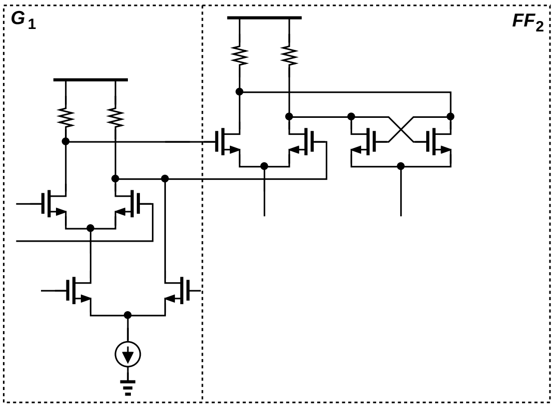
$$MC = High \Rightarrow \div 2$$

$$MC = Low \ \Rightarrow \div 3$$

- The implementation consideration of dual-modulus divider:

(1) /3 is much slower.

(2) /3 is about half of speed of /2.



A Delay-Line-Based GFSK Demodulator for Low-IF Receivers

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[2]National Taiwan University, Taipei, Taiwan

2007.02.12

Outline

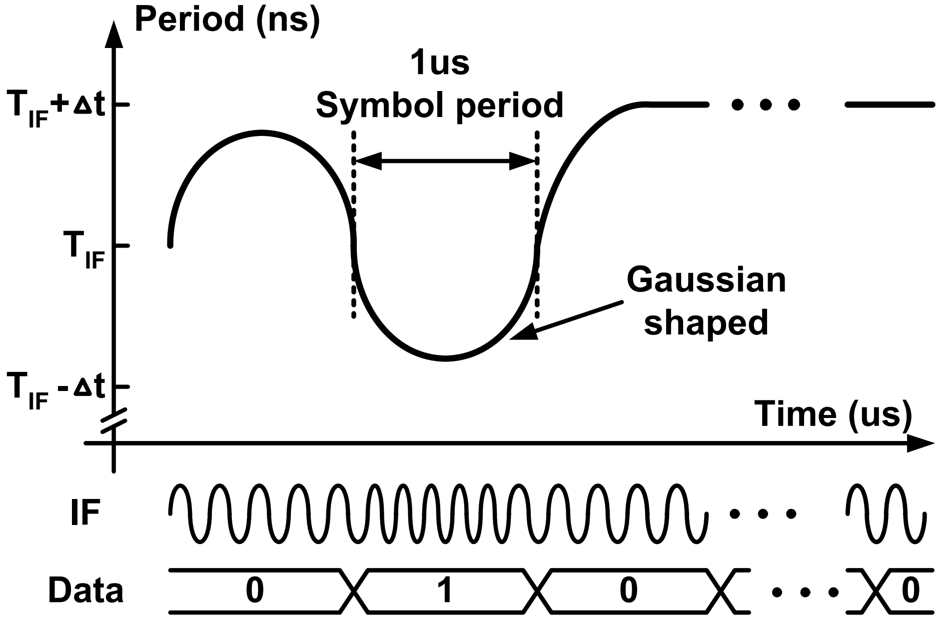
- Introduction
- Architecture
- Building Blocks
- Experimental Results
- Conclusion

Motivation

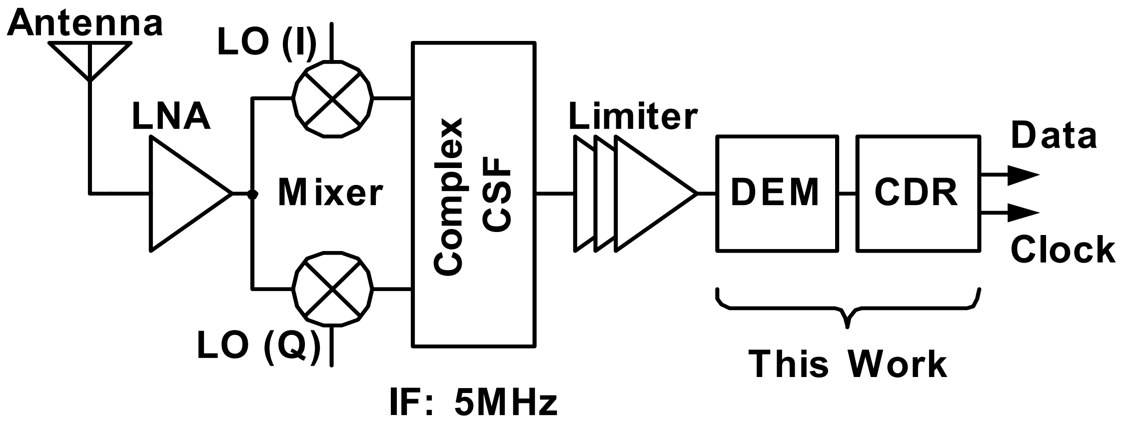
- Wireless personal area network (WPAN) demands:
  - Low power and low cost RF transceiver
- GFSK modulation offers:
  - No need for digital modulator/demodulator
  - Less linearity requirement
- Low-IF receiver offers:
  - High level integration
  - Low flicker noise
  - No DC-offset problem

GFSK Modulated Signal

GFSK with BT=0.5 and modulation index=0.28 ~0.35



Low-IF Receiver



Architecture

Pure analog GFSK demodulator

- Small frequency offset tolerance
- Sensitive to process variation

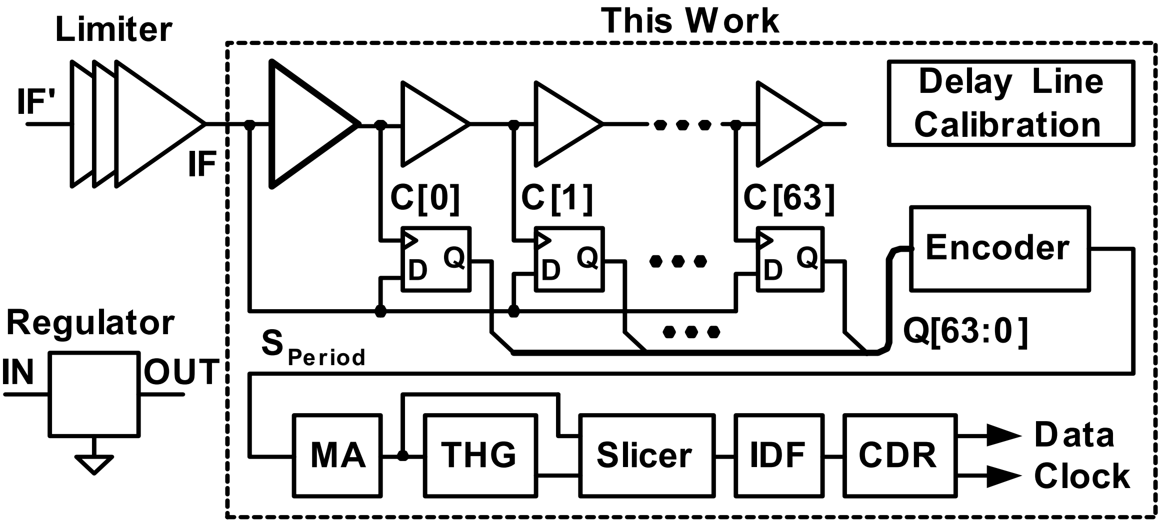
Fully digital GFSK demodulator

- 6b ADC and VGA are required
- Not a cost effective solution

Our approach: Mixed-signal

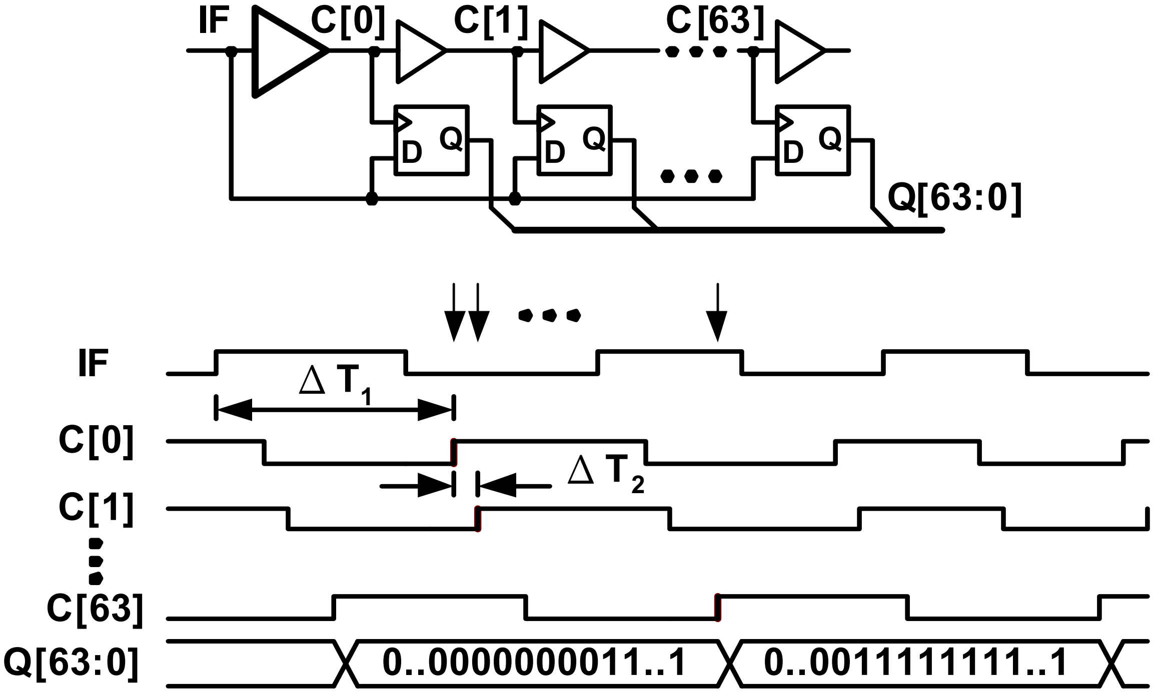
- Use robust TDC
- Slicer is implemented with DSP

Block Diagram

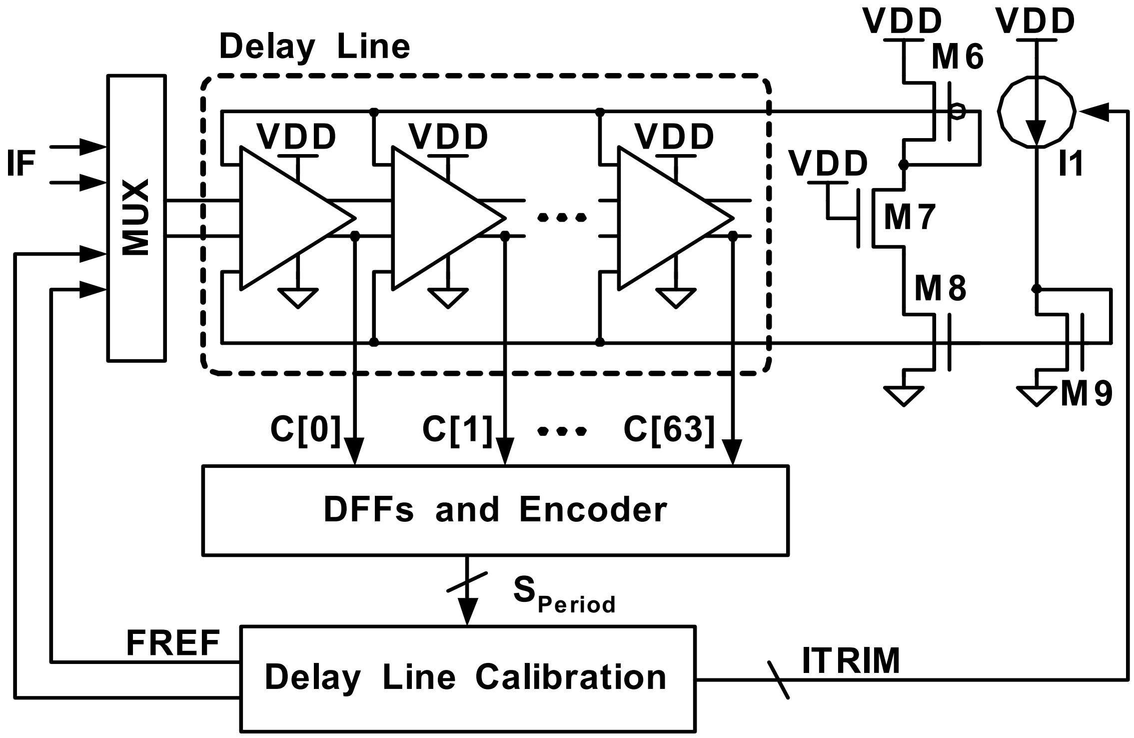


- **Limiter and regulator are integrated for test.**
- **TDC is mixed-signal and the others are digital design.**

Delay-Line Self-Sampler



Self-Calibrated Delay Line



Delay Line Details (I)

Design specification

- IF: 5MHz
- Frequency offset/drift tolerance: ±150kHz/±25kHz
- Frequency deviation: ±80kHz to ±175kHz

Period of the 5MHz GFSK signal

- 186.6ns to 215.5ns

The delay variation of the delay cell: ~5%

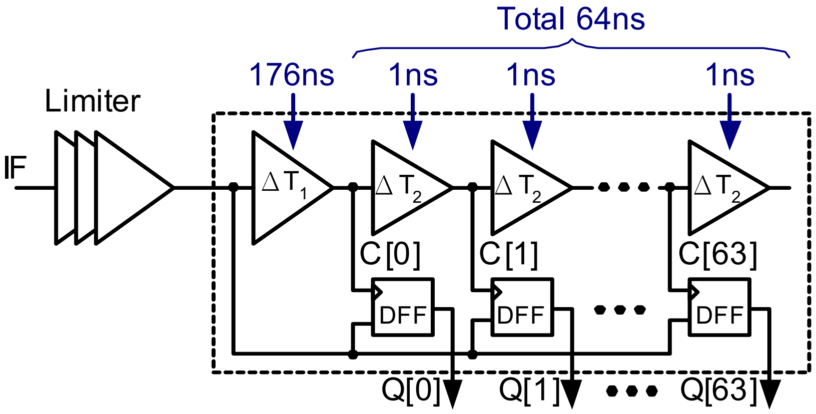
	Min. (Typ.x0.95)	Typ.	Max. (Typ.x1.05)
Coarse Delay Time (ΔT_1)	167ns	176ns	185ns
Total Fine Delay Time $(N \times \Delta T_2)$	49ns	52ns	55ns

$\geq$ 215.5ns

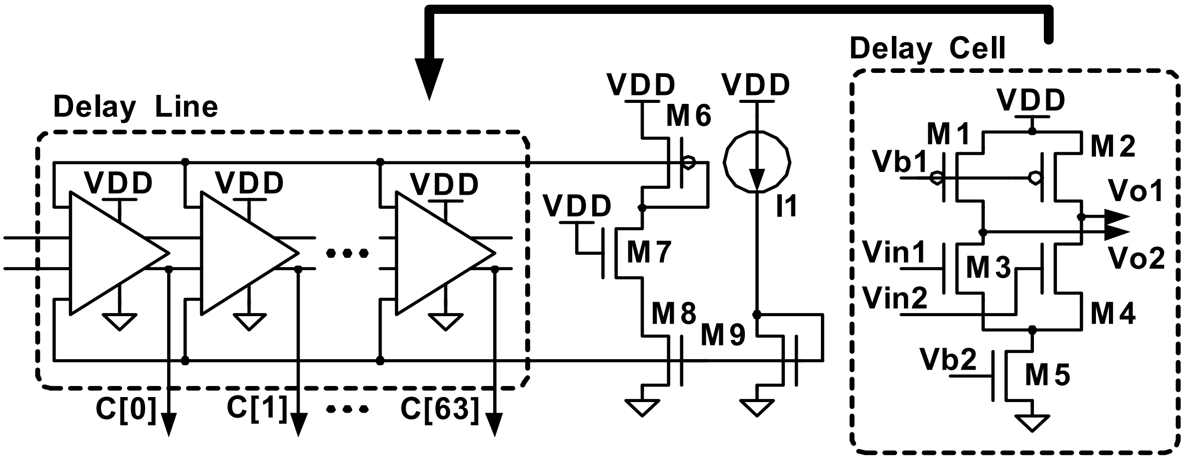
$\leq$ 186.6ns

Delay Line Details (II)

- **The delay of coarse delay line:176ns**
- **The delay of fine delay line:1ns**
- **64 fine delay cells and DFFs are adopted for this architecture.**

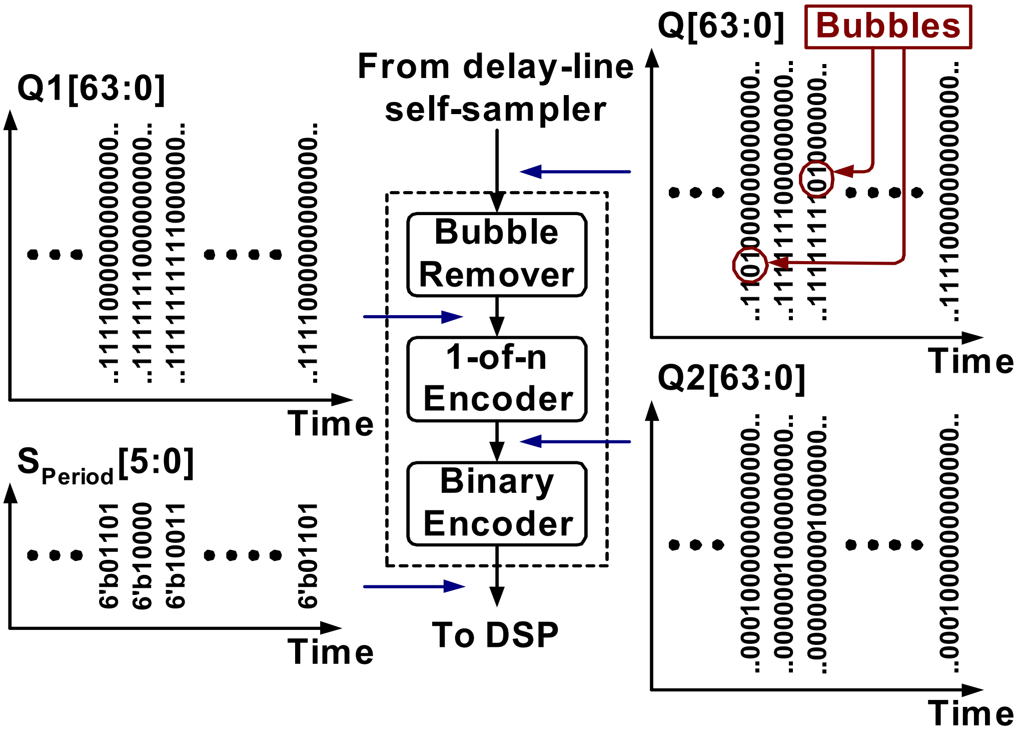


Delay Cell

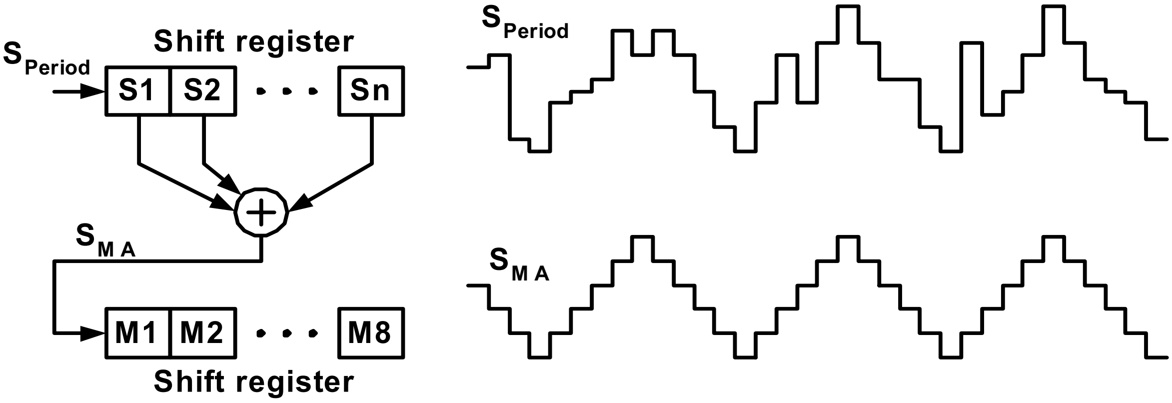


- **Differential structure is adopted to minimize the delay variation.**

Encoder

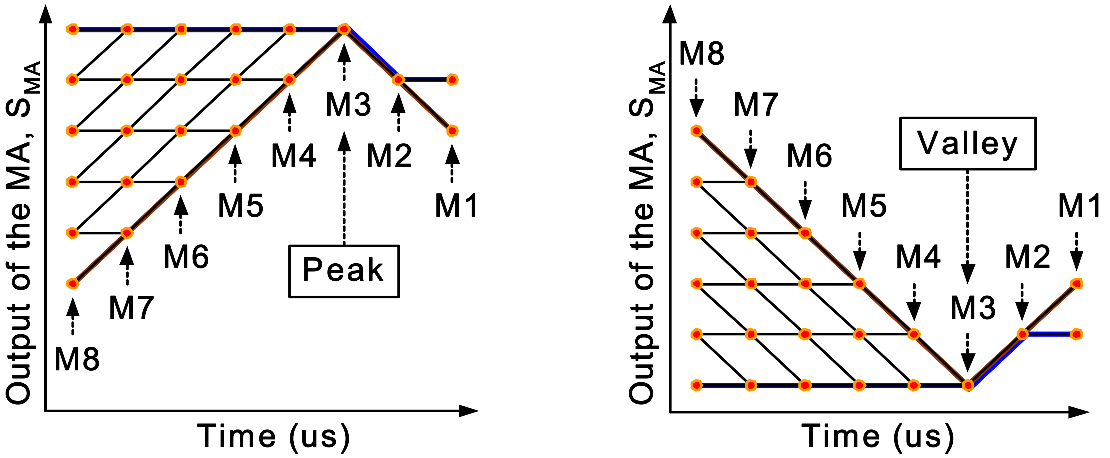


Moving Average



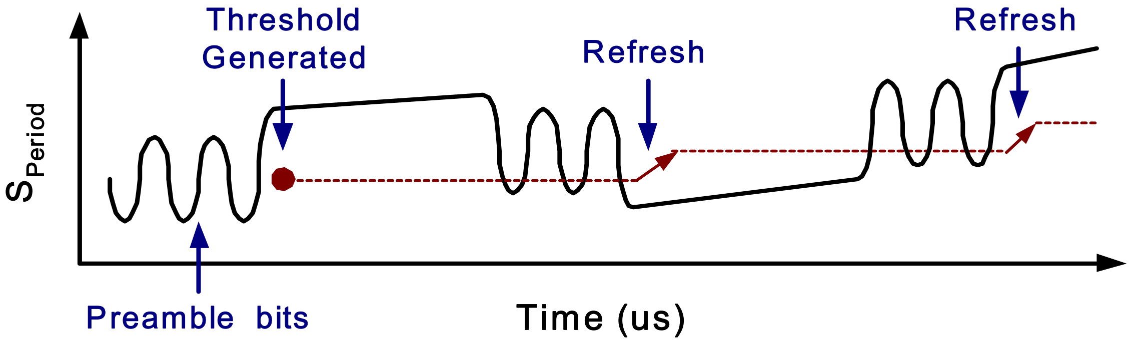
- **MA forms a low-pass filter to remove the high frequency noise.**
- **n is 5 for 1Mb/s and 20 for 250kb/s.**
- **Three continuous S_{MA} are kept for THG.**

Threshold Generator



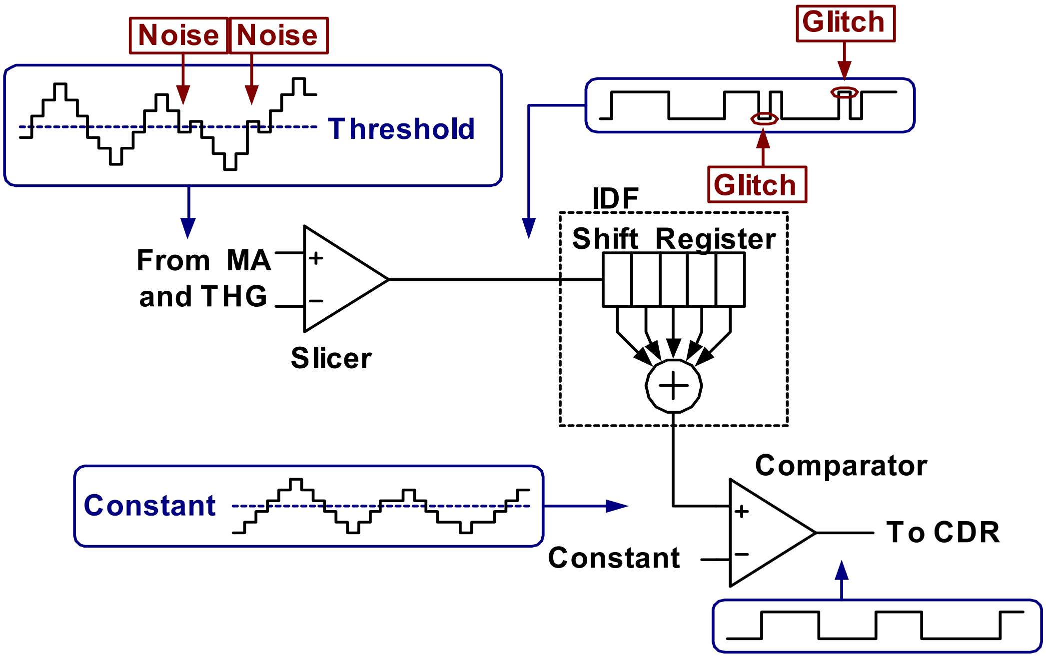
- **If M8<=M7<=M6<=M5<=M4<=M3>M2>=M1, M3 is the Peak.**
- **If M8>=M7>=M6>=M5>=M4>=M3<M2<=M1, M3 is the Valley.**
- **Threshold=(Peak+Valley)/2**

Threshold Value Refresh



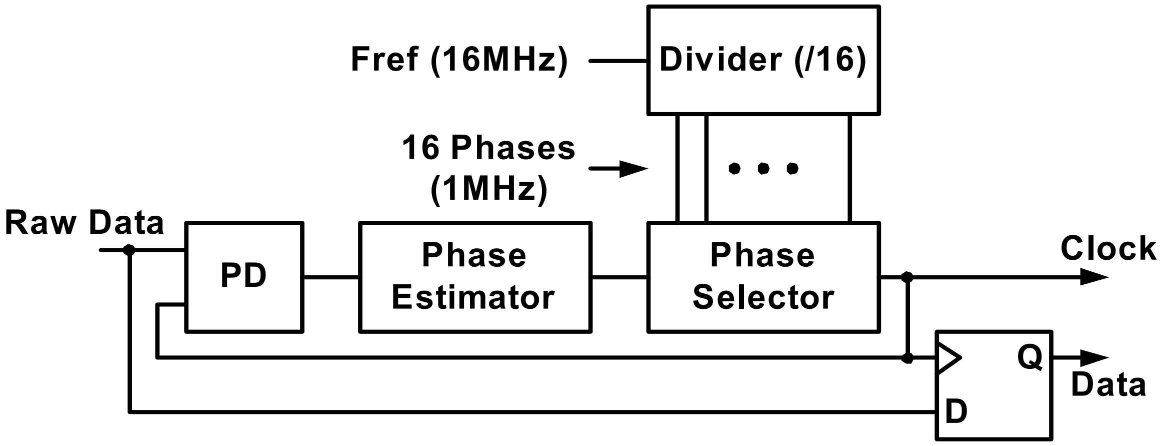
- **Find the preamble pattern, then compute the initial threshold.**
- **Find the pattern 01010 or 10101, then compute the new threshold and refresh the threshold.**

Slicer and IDF



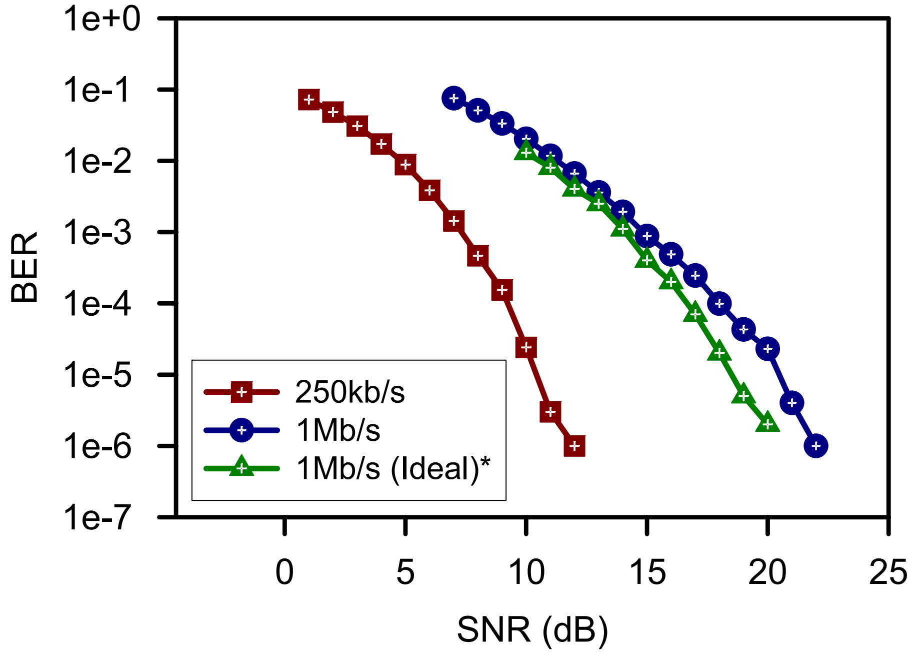
- Glitches are removed after IDF.

CDR



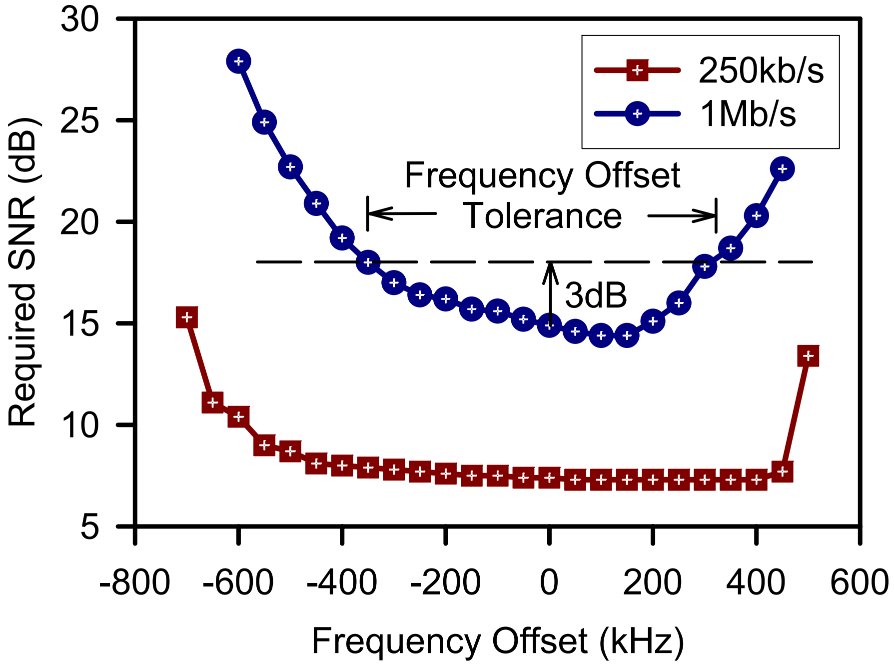
- All digital design
- After initial phase is determined, only the adjacent phase is allowed to change.

BER vs. SNR



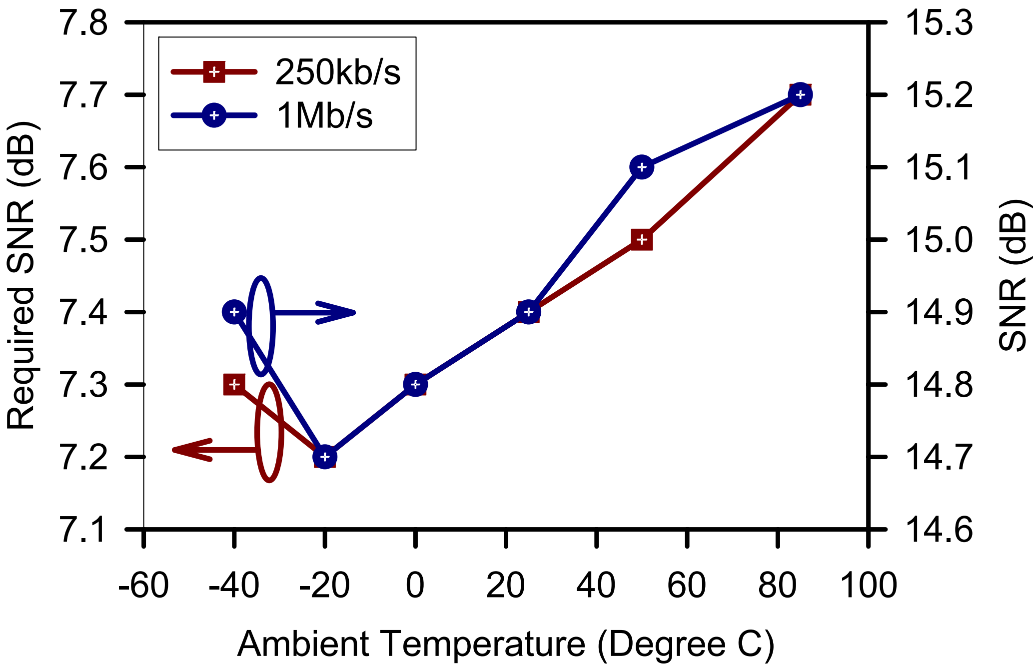
* T.-C. Tee, "A Mixed-Signal GFSK Demodulator for Bluetooth" IEEE TCASII, vol. 53, pp. 197-201, Mar. 2006.

Required SNR vs. Frequency Offset



- **The required SNR is measured at 0.1% BER.**

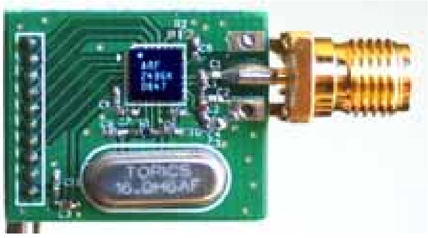
SNR vs. Temperature



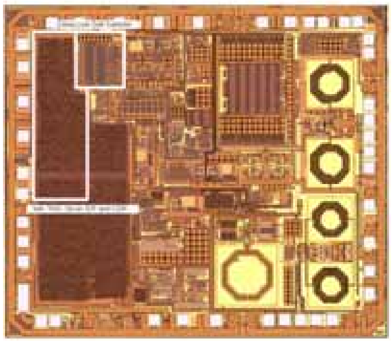
- **The required SNR is measured at 0.1% BER.**

Chip Micrograph

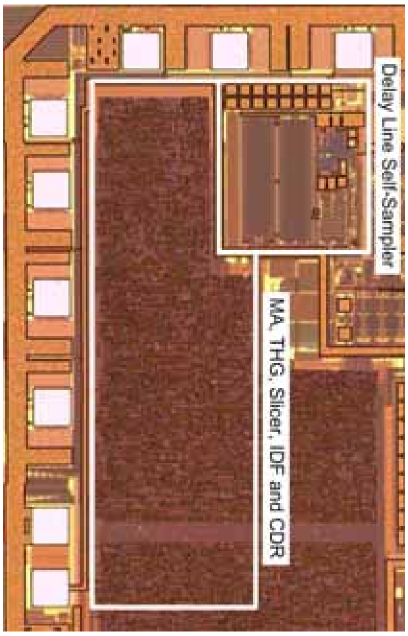
Transceiver Module



Transceiver Chip



- **Active area = 0.26mm²**
- **0.18μm 1P4M CMOS process**



Performance Summary

Technology	**0.18µm 1P4M CMOS**
Active Area	**0.26 mm^2**
Current Consumption	**2mA@1.8V**
IF Frequency	**5MHz**
Modulation Format	**GFSK (Bluetooth Format)**
Data Rate	**1Mb/s, 250kb/s**
Required SNR (1Mb/s, 250kb/s)	**14.9dB, 7.4dB**
C/Ico-channel (1Mb/s, 250kb/s)	**9.5dB, 4dB**
Frequency Offset Tolerance (1Mb/s, 250kb/s)	**+- 350kHz , - 600kHz to 450kHz**
Temperature Range	**-40°C to 85°C**

State-of-the-art Comparison

Reference	Required SNR	Freq. Offset Tolerance	C/Ico	Current Consumption	Chip Area
This work	**14.9dB**	**+-350kHz[3] /+240~-170kHz[4]**	**9.5dB**	**2mA@1.8V**	**0.26mm^2**
H. Darabi (CICC01)	18dB	+-150kHz[4]	12dB	3mA@2.7V	N.A.
B.-S. Song (CICC02)[1]	17.5dB	N.A.	N.A.	27.7mA@1.8V	5.6mm^2
S. Byun (JSSC03)	20dB	+-160kHz[5]	N.A.	N.A.	N.A.
K.-H. Huang (VLSI TSA01)	16.5dB	N.A.	N.A.	2mA@2.5V	0.22mm^2
T.-C. Lee (TCASII06)	16.5dB	+-200kHz[5]	N.A.	3mA@2V	0.3mm^2
S. Samadian (JSSC03)[2]	15.7dB	N.A.	9dB	N.A.	N.A.
B. Xia (JSSC03)	16.2dB	N.A.	11.2dB	3mA@3V	0.7mm^2

[1] Complex bandpass filter and limiter are included

[2] FPGA-based implementation

[3] SNR is 3 dB lower than the nominal value

[4] SNR is 1dB lower than the nominal value

[5] Test condition is not specified

Conclusion

- A delay-line-based GFSK demodulator is proposed.

- Self-calibrated circuits are employed to reduce the delay variation against temperature and supply voltage variation.

- Experimental results indicate that the proposed architecture can achieve the required SNR with 14.9dB.