Course Material
on
Switched Mode Power Conversion

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(for Private Circulation Only)

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Preface

Power electronics forms an important part of industrial electronics. Power electronics is defined as the application of electronic devices and associated components to the efficient conversion, control and conditioning of electric power. The modern power electronics technology traces its origin to the technology of rectifiers developed using mercury arc devices. From this beginning of simple ac-dc conversion of power, today the technology has grown to encompass the general definition given above. The conversion of power relates to the form of electric power namely ac or dc. The control application relates to the regulation of electrical quantities like voltage, current, power etc. or the regulation of non-electrical quantities such as the speed of a motor, the temperature in an oven, the intensity of lighting etc. The conditioning of electrical power relates to the quality of power quantified through harmonic content, reactive power in a system and so on.

The key aspect of power electronics is the efficiency of power processing. As bulk power is processed in power electronic systems, high efficiency of power conversion is vital for reasons of both the economic value of lost power as well as the detrimental effect of the heat that the lost power results in a power electronic system.

Traditionally the subject of power electronics is introduced in an undergraduate curriculam more as "Thyristor and its applications" than as the subject of power electronics proper [1]. The reason for this bias is understandable. Historically the first commercial solid state power switching device available was the silicon controlled rectifier (SCR). Initially the SCRs started replacing the ignitron tubes for ac-dc conversion and Ward-Leonard systems for the speed control of dc motors. With the availability of fast SCRs, the application of SCRs entered the area of dc-ac power conversion as well. The subject of power electronics practically grew with the application of SCRs. The undergraduate curriculum therefore centered around the SCR and broadly dealt with naturally commutated converters for ac-dc power conversion, and forced commutated converters for the dc-ac power converters [8]. The application area was broadly classified into natural commutated applications and forced commutated applications. This classification itself grew out of the limitation of the SCR that it cannot be turned off through the control gate. The focus of such a curriculum was on the SCR in the centre and its myriad applications based on the above classification.

However the monopoly of SCR as the power electronic switch was eroded from the mid 1970s. The newer devices arriving in the commercial scene were bipolar junction transistor (BJT), metal oxide semiconductor field effect transistor (MOSFET), and the insulated gate bipolar transistor (IGBT). These devices are fully controllable (both off/on transition and on/off transition), faster in switching, and easier to control compared to the SCR. These modern devices are getting closer and closer to the ideal properties of a switch. The

classification of applications based on the property of SCR (natural/forced commutation) has become dated.

Accordingly a curriculum addressing the under-graduate students under the title Switched Mode Power Conversion is presented in this book [14]. This is a sub-set of the broad subject matter of power electronics.

The subject matter is covered starting from the properties of ideal switches, real power semiconductor switches and their idealisation, realisation of different circuit topologies, thier operation, steady state performance, dynamic properties, analysis methods, idealised models, effect of non-idealities, control strategies, application of feedback and feedforward control to achieve overall performance and so on. This may be taken as a first course on Switched mode power conversion. The material covered are as follows.

- Power Switching Elements
- Reactive Elements in Power Electronic Systems
- Control, Drive and Protection of Power Switching Devices
- DC-DC Converters
- DC-DC Converters Dynamics
- Closed Loop Control of Power Converters
- Current Programmed Converters
- Soft Switching Converters
- Unity Power Factor Rectifiers

Each chapter has a full complement of exercises and a problem set. Advanced topics such as active filters, and simulation techniques applied to power converters will be topics covered in the next edition of this book

Subject material such as Switched Mode Power Conversion is an application subject. It will be very valuable to include in such a text book design examples and data sheets of power switching devices, magnetic materials, control ICs, manufacturer's application notes etc. This has been done and the material has been designed in the pdf format with links to all the necessary resource material embedded in the same. The appendices carry a number of sections which will enhance the understanding of the subject matter.

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Chapter 1

Power Switching Devices - Characteristics

1.1 Introduction

In Power Electronic Systems (PES), the most important feature is the efficiency. Therefore as a rule PES do not use resistance as power circuit elements. The function of dropping voltages and passing currents is therefore

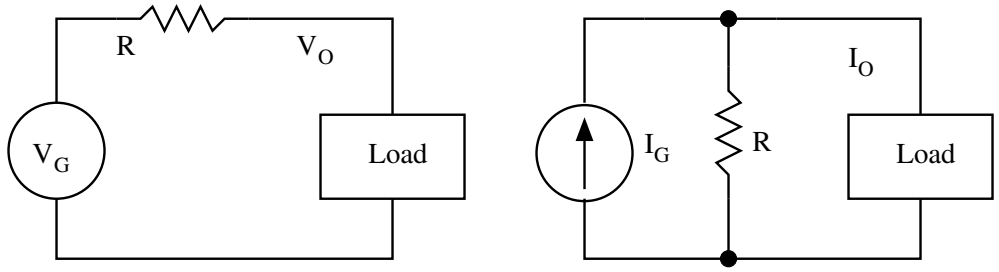

Figure 1.1: Linear Power Converter

achieved by means of switches. The ideal switch drops no voltage (zero resistance) while ON and passes no current (zero conductance) while OFF. When a switch is operated alternately between the two (ON and OFF) states, it may be considered to offer an effective resistance depending on the switching duty ratio. Effectively the switch functions as a loss-less resistance. In the circuit shown in Fig. 1, the resistor drops excess voltage ($V_G - V_O$) or diverts excess current ($I_G - I_O$). These functions are achieved at the cost of power loss in the resistor. The same function may be achieved by means of switches as shown in Fig. 2. It may be seen that the switch effectively drops certain voltage or diverts certain current from reaching the load ($V_O \leq V_G$ and $I_O \leq I_G$). However, the load voltage and current are not smooth on account of the switching process in the control. In general PES will consist of switches for the control

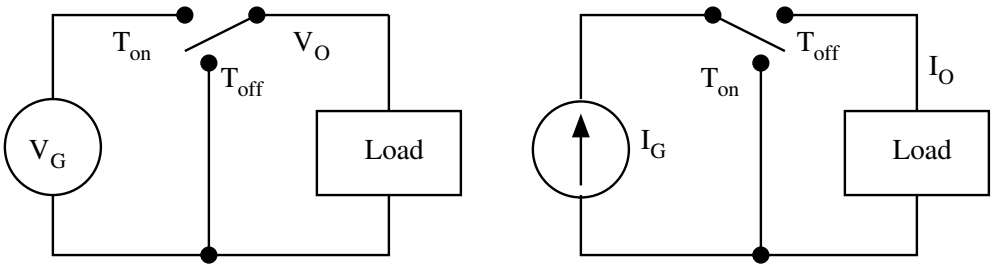

Figure 1.2: Switching Power Converter

of power flow and reactive elements (filters) to divert the effects of switching from reaching the load. The power circuit elements in PES are therefore

1. Switches — (to control transfer of energy)
2. Reactors — (Inductors and Capacitors) — (to smoothen the transfer of energy)

1.2 Ideal Switches

There are several electronic devices, which serve as switches. We may at first list out the desired features of ideal switches. The practical devices may then be studied with reference to these ideal characteristics. The features of ideal switches (with reference to the schematic shown in Fig. 3.) are

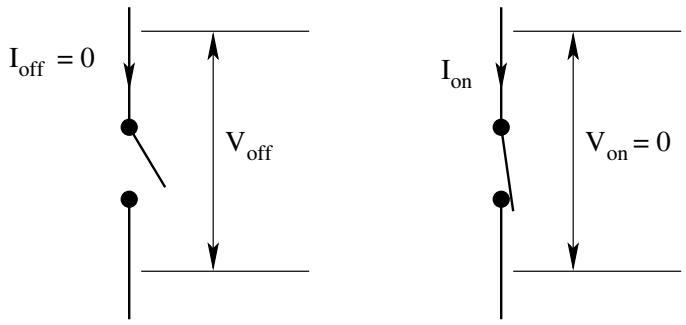

Figure 1.3: Ideal Switch

1. In the OFF state, the current passing through the switch is zero and the switch is capable of supporting any voltage across it.
   $I_{off} = 0; \qquad -\infty \leq V_{off} \leq +\infty;$
2. In the ON state, the voltage across the switch is zero and the switch is capable of passing any current through it.

$V_{on} = 0;$ $\quad -\infty \leq I_{on} \leq +\infty;$

The power dissipated in the switch in the ON and OFF states is zero.

3. The switch can be turned ON and OFF instantaneously.
   $t_{on} = 0;$ $\quad t_{off} = 0;$
4. The switch does not need energy to switch ON/OFF or OFF/ON or to be maintained in the ON/OFF states.
5. The switch characteristics are stable under all ambient conditions.

Features 1 and 2 lead to zero conduction and blocking losses. Feature 3 leads to zero switching losses. Feature 4 leads to zero control effort. Feature 5 makes the ideal switch indestructible. The operating points of the ideal switch on the VI plane lie along the axis as shown in Fig. 4. Practical devices, though not ideal, reach quite close to the characteristics of ideal switches.

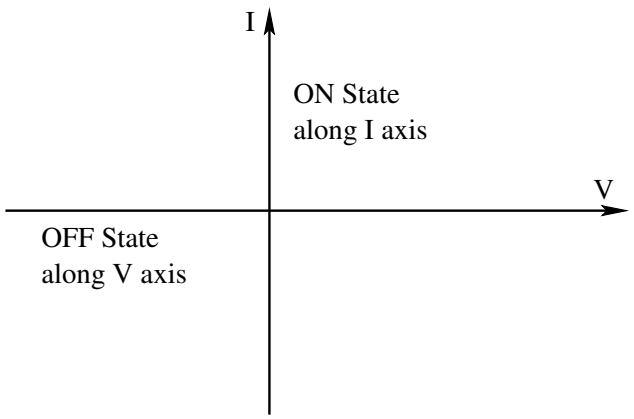

Figure 1.4: V-I Characteristics of the Ideal Switch

1.3 Real Switches

Real switches suffer from limitations on almost all the features of the ideal switches.

1. The OFF state current is nonzero. This current is referred to as the leakage current. The OFF state voltage blocking capacity is limited.
   $I_{off} \neq 0;$ $\quad V_{-} \leq V_{off} \leq V_{+};$
2. The ON state voltage is nonzero. This voltage is called the conduction drop. The ON state current carrying capacity is limited.
   $V_{on} \neq 0;$ $\quad I_{-} \leq I_{on} \leq I_{+};$

   There is finite power dissipation in the OFF state (blocking loss) and ON state (conduction loss).

3. Switching from one state to the other takes a finite time. Consequently the maximum operating frequency of the switch is limited.
   $t_{on} \neq 0$; $t_{off} \neq 0$;
   The consequence of finite switching time is the associated switching losses.

4. The switch transitions require external energy and so also the switch states.
   $E_{on} \neq 0$; $E_{on/off} \neq 0$;
   $E_{off} \neq 0$; $E_{off/on} \neq 0$;
   Real switches need supporting circuits (drive circuits) to provide this energy.

5. The switch characteristics are thermally limited. The power dissipation in the device is nonzero. It appears as heat and raises the temperature of the device. To prevent unlimited rise in temperature of the device external aids are needed to carry away the generated heat from the device.
   Real switches suffer from a number of failure modes associated with the OFF state voltage and ON state current limits.

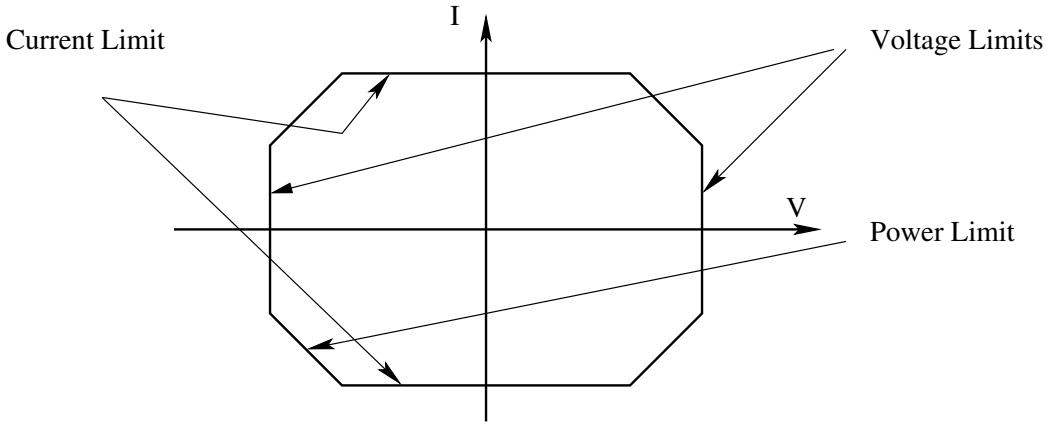

Figure 1.5: Operational Boundaries of a Real Switch

The operating points of real switches on the VI plane are shown in Fig. 5. The steady state operating points lie close to the axis within certain limits. Further there is a safe operating area (SOA) on the VI plane for transient operation.

1.4 Practical Power Switching Devices

There are several power switching devices available for use in PES. They may be classified as

A Uncontrolled switches

The state (ON/OFF) of the switch is determined by the state of the power circuit in which the device is connected. There is no control input to the device. Diodes are uncontrolled switches.

B Semi-controlled switches

The switch may be turned to one of its states (OFF/ON) by suitable control input to its control terminal. The other state of the switch is reachable only through intervention from the power circuit. A thyristor is an example of this type of switch. It may be turned ON by a current injected into its gate terminal; but turning OFF a conducting thyristor is possible only by reducing the main current through the device to zero.

C Controlled switches

Both the states of the switch (ON/OFF) are reachable through appropriate control signals applied to the control terminal of the device. Bipolar junction transistor (BJT), field effect transistor (FET), gate turn-off thyristor (GTO), insulated gate bipolar transistor (IGBT) fall under this group of switches.

The switches desired in PES are realized through a combination of the above devices.

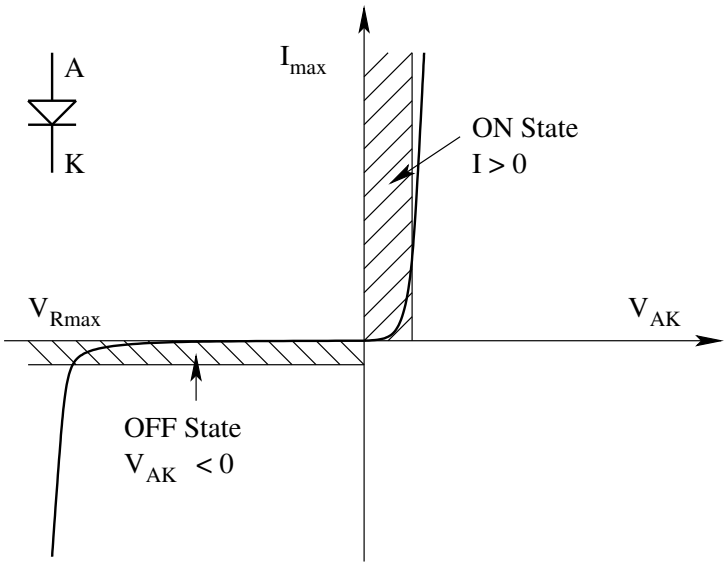

Figure 1.6: Static Characteristics of a Diode

1.5 Diodes

The diode is a two terminal device - with anode (A) and cathode (K). The v-i characteristic of the diode is shown in Fig. 6.

1. When the diode is forward biased ($V_{AK} > 0$), the diode approximates to an ON switch.
   $V_{on} = V_f \approx 0; I_{on}$ is decided by the external circuit.

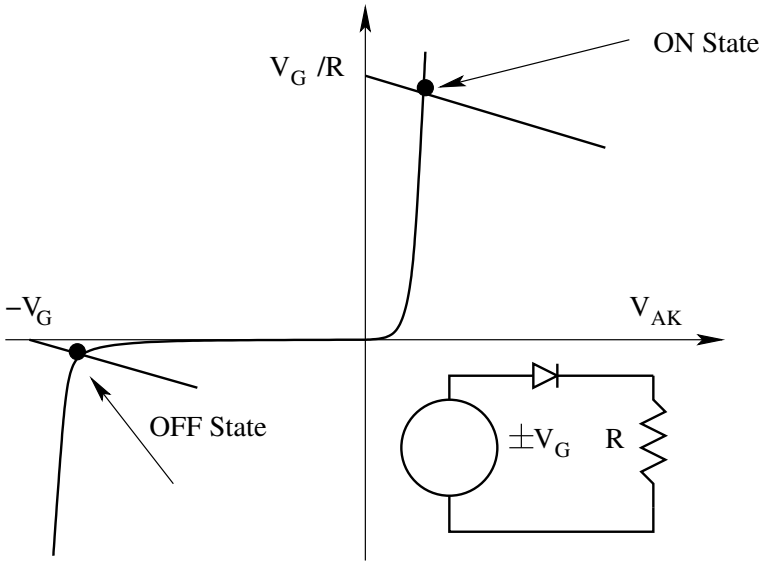

Figure 1.7: Half-Wave Rectifier Application of a Diode

2. When the diode is reverse biased ($V_{AK} < 0$), the diode approximates to an OFF switch.
   $I_{off} = I_{rev} \approx 0; V_{off}$ is decided by the external circuit.
   For a typical application, the forward and reverse biased operating points are shown in Fig. 7.

3. In the ON and OFF condition, the diode dissipates certain finite power.
   $P_{on} = V_f I_{on}$; (Conduction loss)
   $P_{off} = V_{off} I_{rev}$; (Blocking loss)

4. The diode does not have explicit control inputs. It reaches the ON state with a small delay (t_r) when the device is forward biased. It blocks to the OFF state after a small delay (t_{rr}) when the forward current goes to zero.
   t_r = forward recovery time
   t_{rr} = reverse recovery time
   The forward recovery time is much less than the reverse recovery time.

During the reverse recovery time a negative current flows through the device to supply the reverse charge required to block reverse voltage across the junction. The process is shown in Fig. 8. The reverse recovery time decides the maximum frequency at which the diode may be switched.

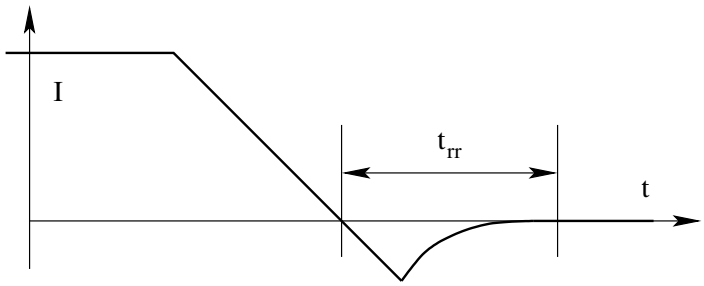

Figure 1.8: Reverse Recovery Time of a Diode

5. In order to limit the junction temperature from exceeding the permissible value, it is necessary to carry the heat away from the junction and pass it on to the ambient.
6. The diode does not need drive circuits. The state of the device depends on the power circuit conditions.
7. The diode is a unidirectional switch. It passes positive current and blocks negative voltage.
8. The short term surge energy, that the diode can withstand is given by its I^2t rating. In order to protect the diode, it will be necessary to use a series fuse to prevent surges of higher energy from passing through the diode.

The important specifications of the diode are

- Average forward current. (to assess suitability with a power circuit)
- Reverse blocking voltage. (to assess suitability with a power circuit)
- ON state voltage. (to assess conduction loss)
- OFF state current. (to assess blocking loss)
- Thermal impedance. (to help thermal design)
- Reverse recovery time. (to assess high frequency switching capability)
- I^2t rating. (to design short circuit protection)

The following are the three types of diodes available for PES applications.

1.5.1 Schottky diodes

These have low ON state voltage ($V_f \approx 0.4V$) with reverse blocking capacity of less than 100V. These are suitable for circuits where low conduction loss is desired. Sample data sheet of a schottky diode (Schottky Diode MBRP30060CT Motorola) is given in Appendix F.

1.5.2 Rectifier diodes

These are suitable as rectifier diodes in line frequency (50/60 Hz) applications. Recovery times are not specified. These are available for current/voltage ratings of a few thousands of amps/volts. Sample data sheet of a rectifier diode (Rectifier Diode 20ETS Series International Rectifier) is given in Appendix F.

1.5.3 Fast diodes

These diodes have very low recovery times and are suitable for high frequency switching applications. The recovery details are fully specified for these diodes. Typical recovery times are a few tens of nanoseconds. Sample data sheet of a fast rectifier diode (Fast Diode RHRG30120CC Harris) is given in Appendix F.

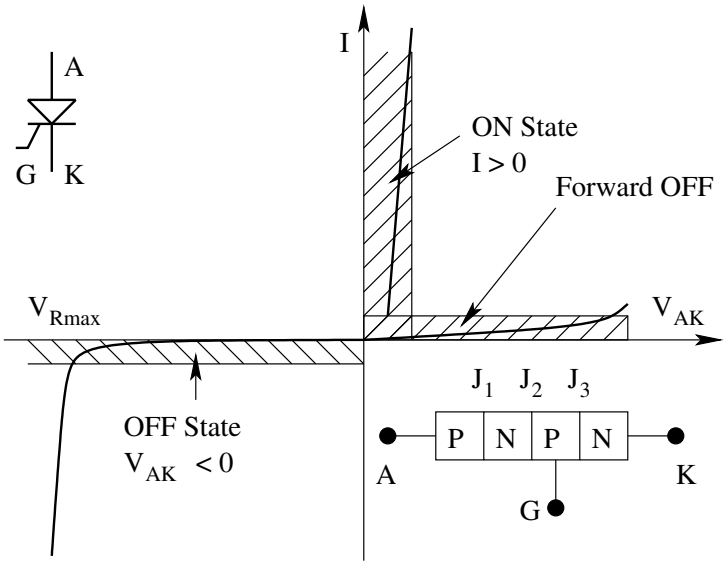

Figure 1.9: Static Characteristics of a Thyristor

1.6 Thyristor or Silicon Controlled Rectifier (SCR)

The Thyristor is a four-layer device. It has three terminals - anode (A), cathode (K), and gate (G). The anode and the cathode form the power terminal pair. The gate and cathode form the control terminal pair. The characteristic of the SCR without any control input is shown in Fig. 9. Under forward biased condition, junction 2 (J_2) supports the entire voltage. Under reverse biased condition the junction 1 (J_1) supports the entire voltage. Junction 3 (J_3) is the control junction and cannot support appreciable reverse voltage. The reverse and forward blocking currents for the SCR are of the same order (a few mA). The control action of the SCR is best understood from the classical two-transistor model shown in Fig. 10. The anode current in the model may be written as

$$I_A = \frac{\alpha_2 I_G + I_{cbo1} + I_{cbo2}}{1 - \alpha_1 - \alpha 2} \tag{1.1}$$

where α_1 and α_2 are the common base current gains of the transistors and I_{cbo1} and I_{cbo2} are their leakage currents; α_1 and α_2 are low at low anode currents. In the absence of control ($I_G = 0$), the anode current will be a small leakage current. There are several mechanisms by which the SCR may be triggered into conduction.

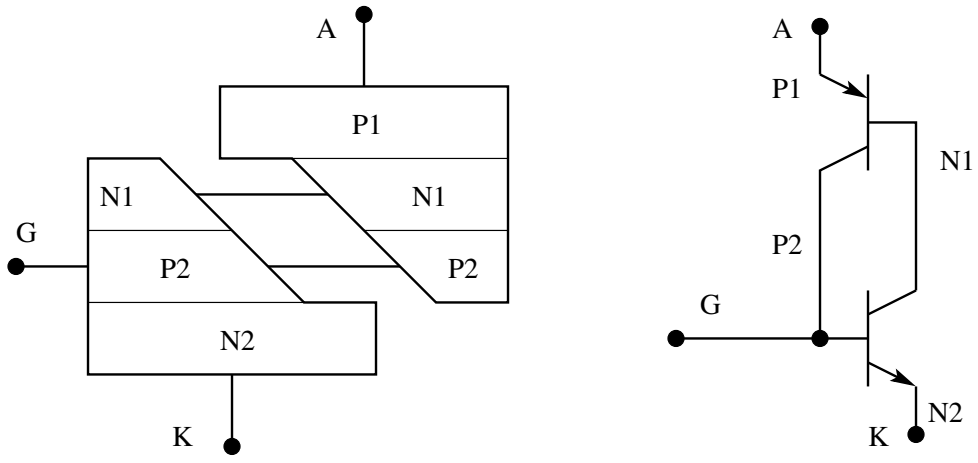

Figure 1.10: Two Transistor Model of the Thyristor

1.6.1 Gate turn-on

If gate current I_G is injected, the emitter currents of the component transistors increase by normal transistor action. The device switches regeneratively into conduction when I_G is sufficiently high. Once the device turns ON, the gate circuit has no further influence on the state of the SCR.

1.6.2 Voltage turn-on

If the forward anode blocking voltage is slowly increased to a high value, the minority carrier leakage current across the middle junction increases due to avalanche effect. This current is amplified by the transistor action leading to eventual turn-on of the SCR.

1.6.3 dV/dt turn-on

When the anode voltage rises at a certain rate, the depletion layer capacitance of the middle junction will pass a displacement current ($i = CdV/dt$). This current in turn will be amplified by transistor action leading to the turn-on of the device.

1.6.4 Temperature effect

At high junction temperature, the leakage currents of the component transistors increase leading to eventual turn-on of the device.

1.6.5 Light firing

Direct light radiation into the gate emitter junction will release electron-hole pairs in the semiconductor. These charge carriers under the influence of the field across the junction will flow across the junction leading to the turn-on of the device.

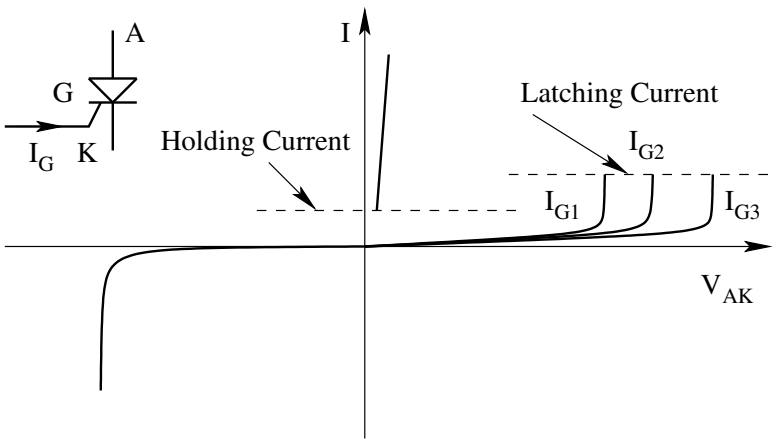

Figure 1.11: Control Characteristics of the Thyristor

The most convenient method of switching an SCR is by means of gate triggering (initiation of switching through a low level current injection across the gate-cathode junction). The control characteristic of an SCR is shown in Fig.

11. Once the anode current reaches the level of latching current following triggering, the device remains ON.

1.6.6 Turn-off of an SCR

To turn-off the SCR, the anode current must be reduced below the holding level and a relatively long time allowed for the Thyristor to regain its forward blocking capacity.

1.6.7 Switching Characteristics of the SCR

The switching operation of an SCR is shown in Fig. 12. The important features are

- Initially when forward voltage is applied across the device, the off state or static dV/dt has to be limited so that the device does not turn ON.
- When gate current is applied (with anode in forward blocking state), there is a finite delay time before the anode current starts building up. This delay time "t_d", is usually a fraction of a microsecond.
- After the delay time, the device conducts and the anode current builds up to the full value I_T. The rate of rise of anode current during this time depends upon the external load circuit.

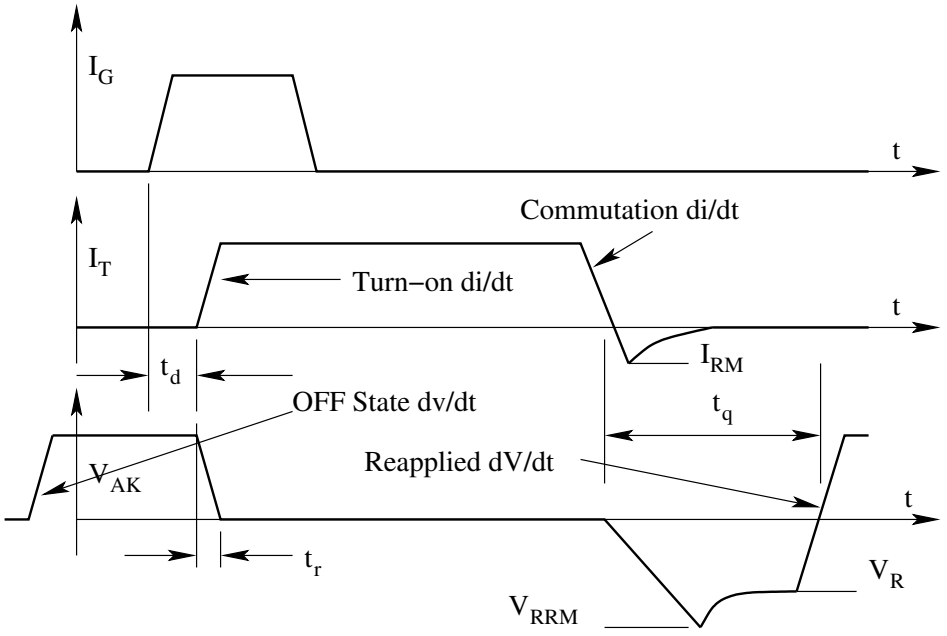

Figure 1.12: Switching Characteristics of a Thyristor

If during turn-on, the anode current builds up too fast, the device may get damaged. The initial turn-on of the device occurs near the gate cathode periphery and then the turn-on area of the device spreads across the entire junction with a finite velocity. If I_T rises at a rate faster than the spreading velocity, then the entire current I_T is confined to a small area of the device eventually causing overheating of the junction and destruction of the device. Therefore it is necessary to limit the turn-on di/dt of the circuit to less than the safe di/dt that can be tolerated by the device.

- During conduction, the middle junction is heavily saturated with minority carriers and the gate has no further control on the device. The device drop under this condition is typically about 1V.
- From the conducting state, the SCR can be turned OFF by temporarily applying a negative voltage across the device from the external circuit. When reverse voltage is applied, the forward current first goes to zero and then the current builds up in the reverse direction with the commutation di/dt. The commutation di/dt depends on the external commutating circuit. The reverse current flows across the device to sweep the minority carriers across the junction. At maximum reverse recovery current I_{RM}, the junction begins to block causing decay of reverse current. The fast decay of the recovery current causes a voltage overshoot V_{RRM} across the device on account of the parasitic inductance in the circuit. At zero current, the middle junction is still forward biased and the minority carriers in the vicinity must be given time for recombination. The device requires a minimum turn-off time t_q before forward blocking voltage may be applied to the device. The reapplied dV/dt has to be limited so that no spurious turn-on occurs. The device turn-off time "t_q" is a function of $T_j, I_T, V_R, V_{DRM}, dV/dt, di/dt$ and V_G.

Thyristors are available for PES applications with voltage ratings upto about 3000V and current ratings upto about 2000A.

1. When blocking forward or reverse voltages a small leakage current flows.
2. When conducting forward current a low voltage is dropped.
3. There are finite power losses in conduction and blocking.
4. The turn ON and turn OFF processes are not instantaneous.
5. The device losses warrant proper thermal design.
6. Turn-ON requires energy through gate circuit. Usually this is quite small.
7. Turn-OFF requires energy supplied through an external commutation circuit. This energy usually is much larger than the turn-on energy supplied through the gate.

8. SCR passes unidirectional current and blocks bi-directional voltage.

The following data are usually specified for an SCR.

- Average forward current (to assess suitability with a power circuit)
- Reverse blocking voltage (to assess suitability with a power circuit)
- Forward blocking voltage (to assess suitability with a power circuit)
- ON state voltage (to assess conduction loss)
- OFF state current (to assess blocking loss)
- Turn-on and commutating di/dt limit (to help in commutating circuit design)
- OFF state and reapplied dV/dt limit (to help in commutating circuit design)
- Thermal impedance (to help thermal design)
- Device turn-off time t_q (to assess high frequency switching capacity)
- I^2t rating (to design short circuit protection)

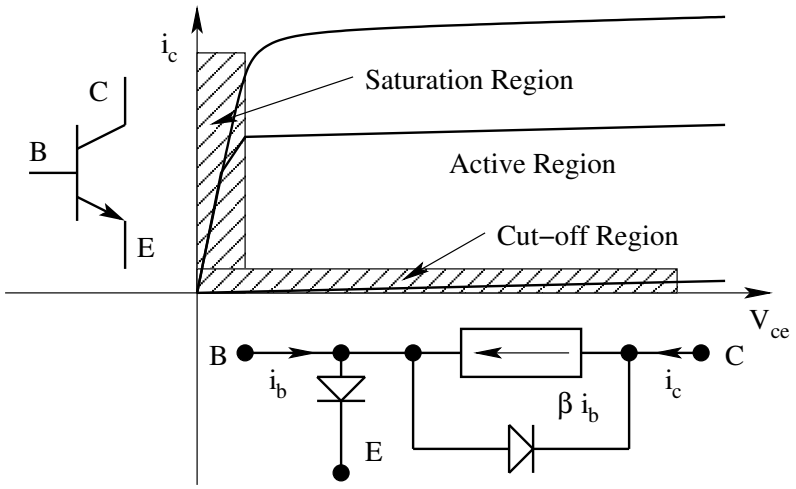

Figure 1.13: Static Characteristics of a Bipolar Junction Transistor

Sample data sheet of a standard thyristor (Thyristor MCR16 Motorola make SCR) and a bidirectional thyristor (Triac T2500 Motorola make Triac) are given in Appendix F.

1.7 Bipolar Junction Transistor (BJT)

The transistor is a three terminal device - emitter (E), collector (C), and base (B). The collector-emitter forms the power terminal pair. The base-emitter form the control terminal pair. The vi characteristics of the transistor is shown in Fig. 13. There are three distinct regions of operation. In the cut-off region, the base current is zero and the device is capable of blocking forward voltage. In the active region, the collector current is determined by the base current ($i_c = \beta i_b$). In the active region of operation the device dissipation is high. In the saturated region, the base is overdriven ($i_b \geq i_c/\beta$). The device drops a small forward voltage and the current is determined by the external circuit. When used as a switch, the transistor is operated in the cut-off and saturated regions to achieve OFF and ON states respectively. In the cut-off region (OFF state), both base-emitter and base-collector junctions are reverse biased. In the saturated region of operation (ON state), both base-emitter and base-collector junctions are forward biased ($i_b \geq i_c/\beta$). The features of the transistor in switching applications are:

1. The device passes a small leakage current while OFF. The OFF state voltage is limited.
   $I_{off} = I_{ceo} \neq 0;$ $\quad -V_{be} \leq V_{off} \leq V_{ceo};$

2. There is a small voltage drop across the device while ON. The ON state current is limited.
   $V_{on} = V_{ce(sat)} \neq 0;$ $\quad 0 \leq I_{on} \leq I_{cmax};$
   The device dissipation is (respectively the conduction and blocking loss)
   $P_{on} = V_{ce(sat)} I_{on};$ $\quad P_{off} = V_{off} I_{ceo};$

3. Steady state control requirements are
   $i_b = 0$ (OFF State); $\quad i_b \geq i_c/\beta$ (ON State);
   The base drive must be adequate to ensure saturation for the maximum current with the minimum guaranteed β of the device.

4. The switches take a finite time to switch ON and OFF after the base drive is established
   $t_{on} = t_d + t_r;$ $\quad t_d =$ delay time; $t_r =$ rise time;
   $t_{off} = t_s + t_f;$ $\quad t_s =$ storage time; $t_f =$ fall time;

5. The conduction, blocking and switching losses raise the junction temperature of the device. To limit the operating junction temperature of the device, proper thermal design has to be made.

6. The device requires drive circuits.

7. The transistor blocks positive voltage and passes positive current.

8. During transients (OFF/ON and ON/OFF), the operating point of the switch requires to be limited to stay within the safe operating area (SOA) of the v-i plane.

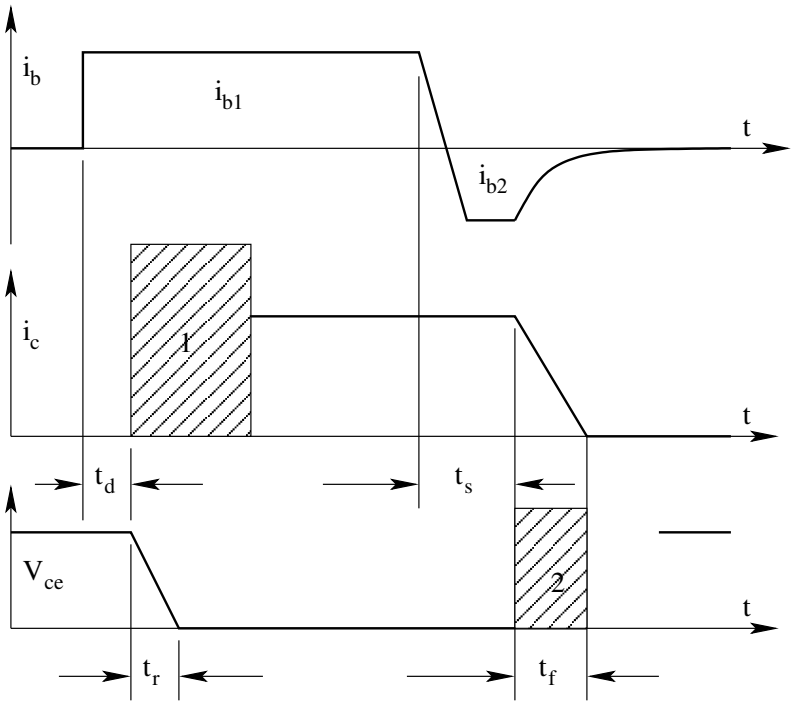

Figure 1.14: Switching Characteristics of a Bipolar Junction Transistor

1.7.1 Switching Characteristics of the Transistor

The switching performance of the transistor is shown in Fig. 14. The important features are

Turn On

To turn-on the device a forward base drive is established.

- The base gets charged.
- After a delay of "t_d", the collector junction starts conduction.
- In a time "t_r", the collector-emitter voltage drops (almost) linearly to $V_{ce(sat)}$.
- The collector current starts from the moment the collector-emitter voltage starts falling. The rise of collector current with time during (hatched region 1) this transient is decided by the external circuit.

Turn Off

To turn-off the transistor, the forward base drive is removed and a negative base drive is set up.

- The junctions (base-emitter and base-collector) remain forward biased for a duration "t_s". During this storage time, i_c continues to flow and the device voltage v_{ce} drop remains low. This is the time taken to remove the accumulated charge in the junction, so that the junction may start blocking. The storage time increases with i_{b1} and decreases with i_{b2}.
- After the storage time, in a time "t_f", the collector current falls (almost) linearly to zero. During the fall time (hatched region 2), the collector-emitter voltage $v_{ce(t)}$ is decided by the external circuit.

It may be seen from the switching process that the device losses are low during the transient intervals t_d and t_s. The switching losses occur during t_r and t_f. The collector current during t_r and the device voltage during t_f are dictated by the external circuit. This feature is used to reduce the switching losses in any application. The important specifications of the transistor are

- Peak and average current (to assess suitability with a power circuit)
- Peak blocking voltage V_{ceo} (to assess suitability with a power circuit)
- ON state voltage $V_{ce}(sat)$ (to assess conduction loss)
- OFF state current I_{ceo} (to assess blocking loss)
- Thermal impedance (to help thermal design)
- Switching times t_d, t_s, t_r and t_f (to design drive circuits I_{b1}, I_{b2} and to select the switching frequency)
- Forced beta (to design drive circuit)
- Safe operating area SOA (to design switching protection)

The links to data sheets of a standard BJT BUX48 and a darlington transistor MJ10015 are given in Appendix F.

1.8 MOS Field Effect Transistor(MOSFET)

MOSFET is becoming popular for PES applications at low power and high frequency switching applications (a few kW and a few 100s of kHz). It is a three terminal device - drain (D), source (S) and gate (G). Drain and source form the power terminal pair. Source and gate form the control terminal pair. The gate is insulated from the rest of the device and therefore draws no steady state current. When the gate is charged to a suitable potential with respect

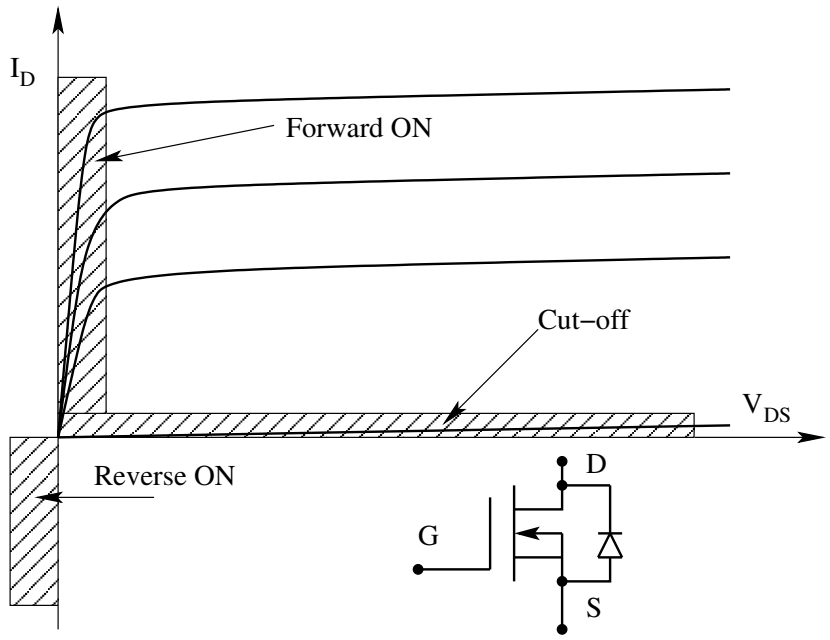

Figure 1.15: Steady State Characteristics of the MOSFET

to the source, a conducting path known as the channel is established between the drain and the source. Current flow then becomes possible across the drain and the source. MOSFETs used in PES are of enhancement type, i.e. the device conducts when a suitable gate to source voltage is applied. Whenever the gate to source voltage is zero, the device blocks. Both N and P channel MOSFETs are available. The N channel versions are more common. The v-i characteristic of a MOSFET is shown in Fig. 15. The two regions of operation are the cut-off region (OFF state) when V_{gs} is 0 and the resistance region (ON state) when V_{gs} is greater than $V_{gs(th)}$. The device has no reverse blocking capability on account of the body diode, which conducts the reverse current. The features of the MOSFET in switching applications are

1. The device passes a small leakage current while OFF. The OFF state voltage is limited.
   $$I_{off} = I_{DSS} \neq 0 \; ; \qquad 0 \leq V_{DSS} \leq BV_{DSS};$$
   In the ON state the device is equivalent to a resistance. The peak and the continuous drain current are limited.
   $$V_{on} = r_{ds(on)} I_{on} \neq 0 \; ; \qquad -I_{SD} \leq I_{on} \leq I_D;$$
   The negative current capability is on account of the body diode. The device being resistive in the ON state has a positive temperature coefficient enabling easy parallel operation of MOSFETs.

2. The device dissipation is
   $$P_{on} = I_{on}^2 r_{ds(on)} \text{ (Conduction loss)}$$

$P_{off} = V_{DS} I_{DSS}$ (Blocking loss)

3. Steady state control requirements are
   $V_{gs} < V_{gs(th)}$ (OFF state)
   $V_{gs} > V_{gs(th)}$ (ON state)

4. The switches take a finite time to switch ON and OFF after the gate drive is established.
   $t_{on} = t_{d(on)} + t_r$; $t_{d(on)}$ = on delay time; t_r = rise time;
   $t_{off} = t_{d(off)} + t_f$; $t_{d(off)}$ = off delay time; t_f = fall time;
   MOSFET being a majority carrier device, there is no storage delay time as in BJT. Further the switching times are atleast an order of magnitude better than those of BJT.

5. The conduction, blocking, and switching losses raise the junction temperature of the device. To limit the operating junction temperature of the device, proper thermal design has to be made.

6. The device needs a drive circuit. However the drive energy is smaller compared to a BJT because the steady state gate current requirement is zero.

7. The MOSFET blocks positive voltage and passes both positive and negative current (negative current through the body diode).

8. Being a majority carrier device, MOSFET does not suffer from second breakdown.

9. In some applications, the body diode of the MOSFET makes the device sensitive to spurious dV/dt turn-on.

1.8.1 Switching Charcteristics of the MOSFET

The switching performance of the MOSFET is shown in Fig. 16. The turn-on delay time $t_{d(on)}$ is the time for the gate source capacitance to charge to the threshold level to bring the device into conduction. The rise time t_r is the gate charging time to drive the gate through the control range of the gate voltage required for full condition of the device. At turn-off, the process is reversed. The turn-off delay time is the time $t_{d(off)}$ required for the gate to discharge from its overdriven voltage to the threshold voltage corresponding to active region. The fall time is the time required for the gate voltage to move through the active region before entering cut-off. The important specifications of the MOSFET are

- Average and peak current I_D and I_M (to assess suitability with a power circuit)
- Peak blocking voltage BV_{DSS} (to assess suitability with a power circuit)

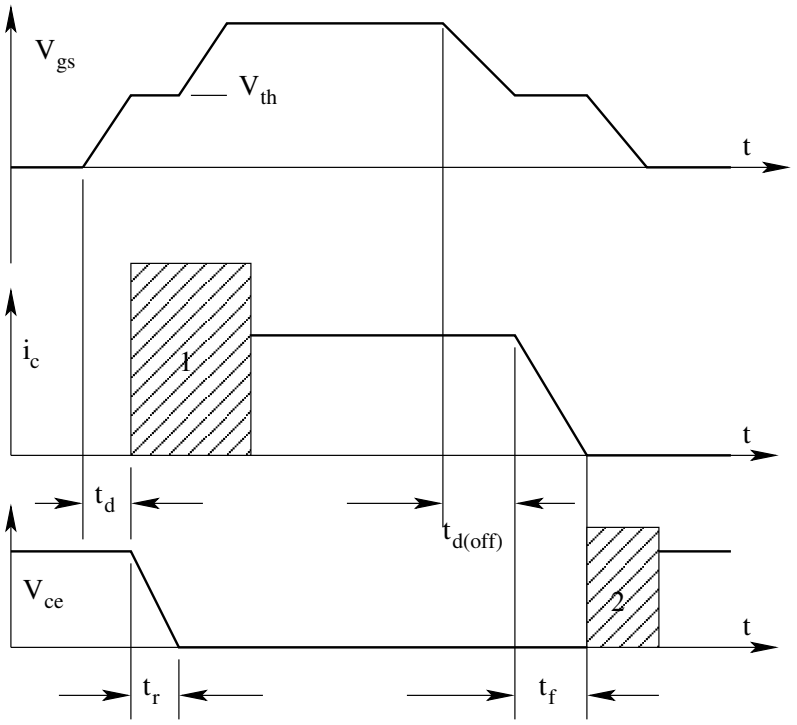

Figure 1.16: Switching Characteristics of the MOSFET

- ON state resistance $r_{ds(on)}$ (to assess conduction loss)
- OFF state current I_{DSS} (to assess blocking loss)
- Thermal impedance (to help thermal design)
- Switching times $t_{d(on)}, t_r, t_{d(off)}, t_f, V_{gs}, R_{gs}$
  (to design drive circuit and to select switching frequency)
- Threshold voltage $V_{gs(th)}$ (to design drive circuit)
- Body diode current I_{SD} (to evaluate conduction loss)
- Body diode recovery time t_{rr} (to assess high frequency capability)
- Input capacitances $C_{iss}, C_{oss}, C_{rss}$ (to design the drive circuit)

The link to data sheet of a typical MOSFET IRF540 is given in Appendix F.

1.9 Gate Turn-off Thyristor (GTO)

The Gate Turn-Off Thyristor was invented in 1960. The GTO, a 3 terminal 4-layer semiconductor device is similar in construction to the Thyristor. The additional feature of the GTO is that it can be turned off as well as turned

on through the gate. The two-transistor model of the GTO is shown in Fig. 17. The operating principle of a GTO, similar to the SCR is based on the regeneratively coupled switching transistor pair. The GTO on account of its construction, unlike an SCR, behaves like a large number of small Thyristors on a common substrate, with common anodes and gates, but individual cathodes. The turn-on mechanism of the GTO is identical to that of the SCR. However, in the case of the GTO, it is possible to turn-off the device by passing a reverse gate current. The ratio of anode current that can be turned-off to the reverse gate current necessary to carry out successfully the turn-off process is called the turn-off gain. The switching cycle of a GTO consists of four different phases. These are namely,

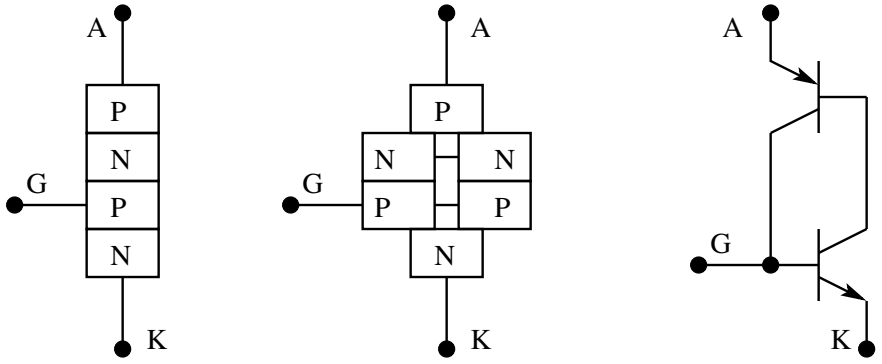

Figure 1.17: Two Transistor Regenerative Model of a GTO

- Turn-on
- Conduction
- Turn-off
- Blocking

1.9.1 Turn-on

The turn-on process of a GTO is initiated by triggering a current through the gate-cathode circuit. In the case of a Thyristor, a small gate current is adequate to initiate the regenerative switching on process. The conduction then spreads to a large silicon area. The on-state currents may be several thousands of amperes. The on state rate-of-rise-of-current, however, has to be limited to a few hundred amperes per microsecond. GTOs, on the contrary require a much larger current to initiate the regenerative turn-on process. On account of the segmented construction of the cathode, all the individual thyristors turn-on simultaneously. The anode current may rise at the rate of a few thousand amperes per microsecond. Turn-on gate current may vary and be orders of magnitude higher compared to SCRs.

1.9.2 Conduction

The conduction process is similar to that of a conventional SCR. The on-state voltage is low. Surge current capability is high and the conduction loss is low.

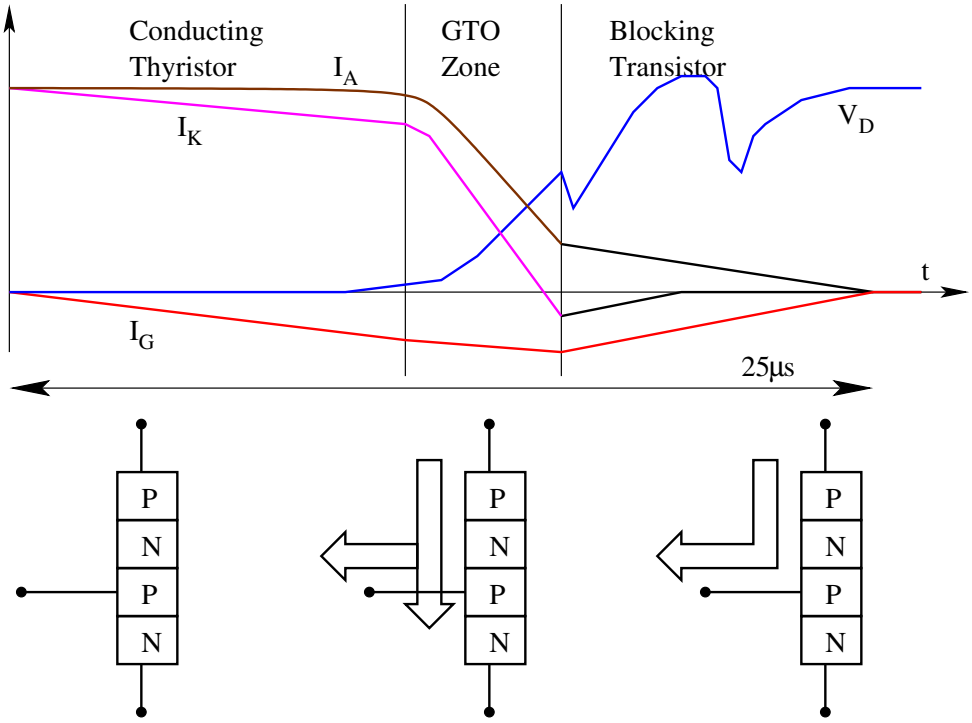

Figure 1.18: Conduction and Turn-off of GTO

1.9.3 Turn-off

The turn-off process in the GTO is initiated by passing a negative current through the gate cathode circuit. The cathode current is then constricted towards the centre of each cathode segment, thus pinching off the cathode current. As the cathode current is pinched, the anode current falls rapidly. During the pinch-off process the active silicon area reduces. Further, the cathode current tends to get redistributed away from the extinguishing gate current. This process takes place during the storage time. This process culminates with a rising anode voltage and a falling anode current. This phase is the most critical in the turn-off process and requires the presence of a snubber across the device to limit the reapplied rate-of-rise-of-anode-voltage to about 500 to 1000 v/μs. This process is shown in Fig. 18. The GTO zone in Fig. 18 is a vulnerable zone when both anode voltage and cathode current co-exist. In order to prevent the device from turning on again in this region, it is necessary

to use an appropriate snubber across the device.

1.9.4 Blocking

In the blocking state, the GTO behaves just like a PNP transistor. When the bias supply has negligible impedance, the GTO has practically unlimited dv/dt capability.

1.9.5 Gate Drive

The gate drive for the GTO has the following requirements.

- Turn the GTO on by means of a high current pulse (I_{GM}).
- Maintain conduction through provision of a continuous gate current during on state.
- Turn-off the GTO with a high negative current pulse (I_{GQ}).
- Maintain negative gate voltage during off state with sufficiently low impedance.

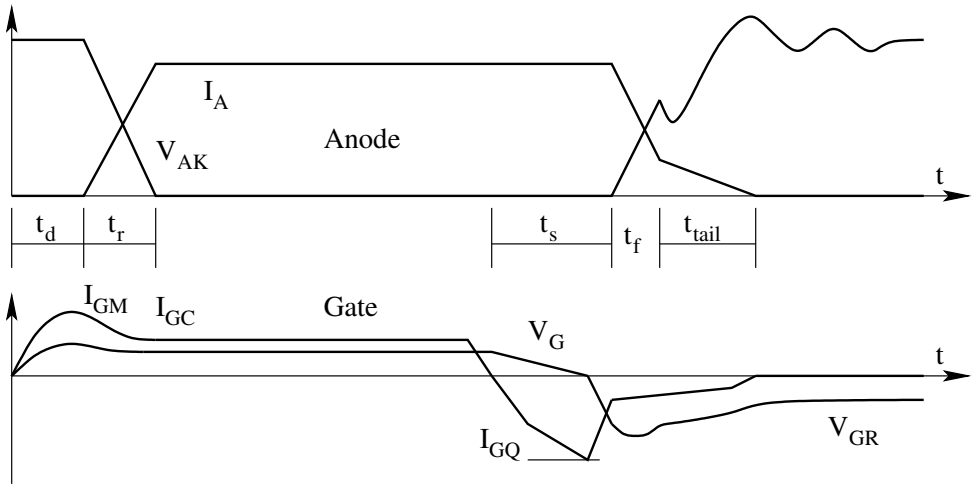

Figure 1.19: Drive and Power Circuit Waveforms for the GTO

Typical gate drive waveforms are shown in Fig. 19. GTOs require much more gate current than a similar rated SCR. The GTO structure is well suited for high-current pulsed applications on account of their large turn-on rate-of-rise-of-anode-current capability. The initial gate current I_{GM} and the recommended value of dI_G/dt can be taken from the data sheet. A rough guide to the required value of I_{GM} is that it is about 6 times I_{GT}. For a GTO with 3A I_{GT} at 25°C, I_{GM} is 20A at 25°C, or 60A at −40°C, for the values of anode voltage and di/dt cited on the data sheet (50% of V_{drm} and 300 to 500A/μS).

The rate of rise of this current is important. It should be atleast 5% of the anode di/dt, with a minimum duration equal to the sum of the delay time and rise time ($t_{gt} = t_d + t_r$).

In the conduction state, the GTO is like a Thyristor. Extra care must be taken such that the GTO does not partially unlatch following turn-on. This may happen in motor drive applications, where the load current may fall momentarily to a low value following turn-on. The continuous drive current is to overcome such eventualities. This current must be atleast 20% more than I_{GT}. This is all the more important when the load current becomes negative, when the load current flows through the freewheeling diode. In such a case the GTO returns to the off state. Then when the load current becomes positive, the GTO will not turn on. A typical 3000A GTO requires a continuous drive current of the order of 10A at $-40°C$. This need is highly temperature dependent. The turn-off of the GTO requires atleast 20% to 30% of anode current. Fig. 18 shows a critical period during which the anode voltage is positive and the cathode current is non-zero. The drive design must provide a large dI_{GN}/dt, to minimize this critical duration. In the blocking state, the preferred gate bias is about -5V or lower. This may be as high as the rated gate-cathode voltage. Under this situation, the device has practically no dv/dt limitation. The device behaves as a low gain BJT with open base.

1.10 Insulated Gate Bipolar Transistor (IGBT)

IGBT is a three terminal device - collector (C), emitter (E), and the gate (G). The collector and emitter form the power terminal pair. The gate and emitter form the control terminal pair. It combines the high current carrying capacity of the BJT with the low control power requirements of the MOSFET [3]. The control characteristics are similar to that of a MOSFET and the power characteristics to that of a BJT. Fig. 20 shows the forward characteristics of an IGBT. The operating points are either in the saturation region (ON state) or in the cut-off region (OFF state). The gate to emitter voltage of the device determines the state of the device ($V_{gs} > V_{gs(th)}$, ON state) ; ($V_{gs} = 0$, OFF state). With the gate emitter voltage above the threshold voltage, the control side MOSFET turns on and forward biases the output pnp transistor. The ON state voltage is considerably less than that of a MOSFET. The trade-off is in the switching speed. Another important point to notice is the presence of a parasitic SCR in the device structure. This can lead to a latch-up of the device in the ON state. The hazard of latch-up existed in the first generation IGBTs.

The features of the IGBT in switching applications are

1. The device passes a small leakage current while OFF. The OFF state voltage is limited.
$$I_{off} = I_{ces} \neq 0 \; ; \qquad 0 \leq V_{off} \leq V_{ces};$$

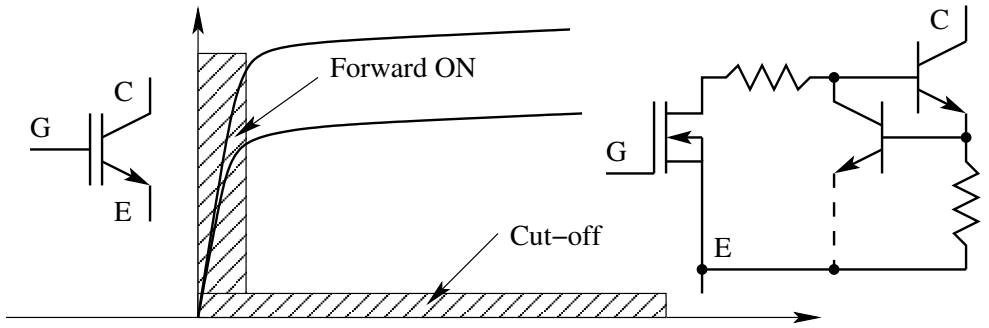

Figure 1.20: Forward Characteristics of IGBT

Usually IGBTs are made with a hybrid reverse diode integral to the device.

2. There is a small voltage drop across the device while ON. The ON state current is limited.
   $V_{on} = V_{ce(sat)} \neq 0$; $-I_D \leq I_{on} \leq I_c$;

3. The device dissipation is
   $P_{on} = V_{ce(sat)} I_{on}$ (Conduction loss)
   $P_{off} = V_{off} I_{ces}$ (Blocking loss)

4. Steady state control requirements are
   $V_{gs} \leq 0$ (OFF state)
   $V_{gs} > V_{gs(th)}$ (ON state)

5. The switches take a finite time to switch ON and OFF after the base drive is established.
   $t_{on} = t_d + t_r$;
   t_d = on delay time; t_r = rise time;
   $t_{off} = t_{s(off)} + t_f$;
   $t_{s(off)}$ = storage delay time; t_f = fall time;
   The switching times are designated the same way as those of BJTs.

6. The conduction, blocking, and switching losses raise the junction temperature of the device. To limit the operating junction temperature of the device, proper thermal design has to be made.

7. The device requires drive circuits. Turn-on is improved by a fast rising voltage source drive with low series impedance. Turn-off is improved by charging the gate to a negative voltage during OFF time.

8. The IGBT blocks positive voltage and passes positive current. With an integral hybrid reverse diode the device can also pass negative current.

9. During transients (OFF/ON and ON/OFF), the operating point of the switch requires to be limited to stay within the SOA of the v-i plane.

1.10.1 Switching Characteristics of the IGBT

The switching performance of the IGBT is shown in Fig. 21. The switching process may be seen to be a combination of the switching performance of a MOSFET and a BJT. Just as in a transistor, the current rise in region 1 and the voltage build up in the region 2 are determined by the external circuit.

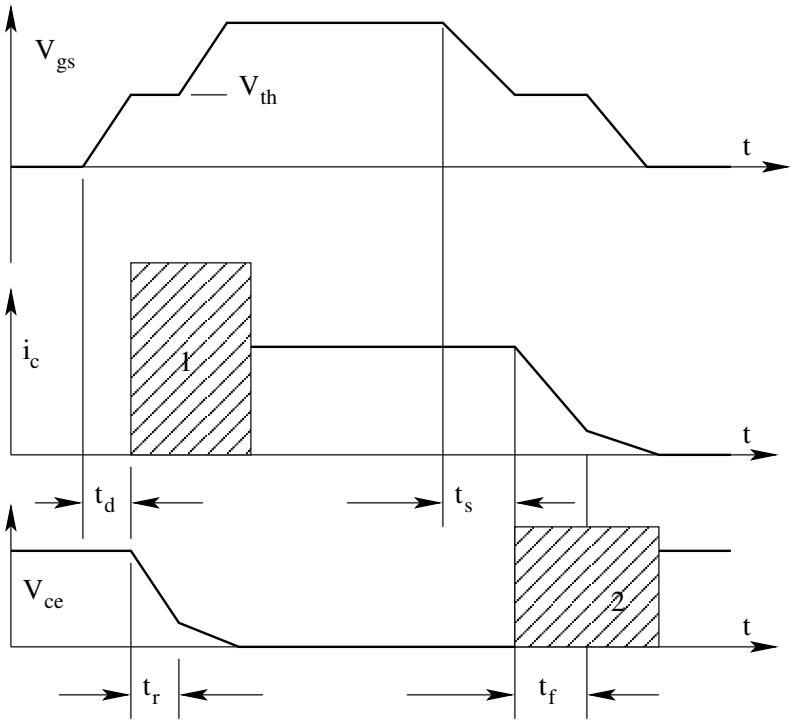

Figure 1.21: Switching Characteristics of IGBT

The important specifications of the IGBT are

- Peak and average current (to assess suitability with a power circuit)
- Peak blocking voltage V_{ces} (to assess suitability with a power circuit)
- ON state voltage $V_{ce(sat)}$ (to assess conduction loss)
- OFF stage current I_{ces} (to assess blocking loss)
- Thermal impedance (to help thermal design)
- Switching times t_d, t_r, t_s, t_f
  (to design drive circuit and to select switching frequency)

- Threshold voltage $V_{ge(th)}$ (to design drive circuit)
- Safe operating areas SOA (to design switching protection)

The links to data sheets of a typical IGBT HGTG30N120D2 and a two quadtant IGBT half bridge CM50DY28 are given in Appendix F.

1.11 Integrated Gate Commutated Thyristor (IGCT)

Developed in 1994 and announced in 1997, the Integrated Gate-Commutated Thyristor is the latest addition to the thyristor family. It combines the rugged on state performance of the thyristors and the positive features of the turn-off behaviour of the transistor. The Gate-Commutated Thyristor is a semiconductor based on the GTO structure, whose gate circuit is of such low inductance that the cathode emitter can be shut off instantaneously, thereby converting the device during turn-off to effectively a bipolar transistor. The basic principle of operation of the IGCT is illustrated in Fig. 22. In the conducting state the IGCT is a regenerative thyristor switch. It is characterized by high current capability and low on-state voltage. In the blocking state, the gate-cathode junction is reverse-biased and is effectively out of operation. The equivalent

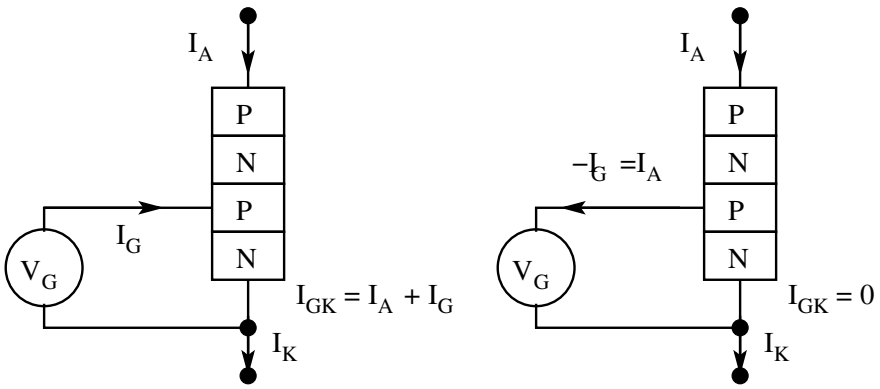

Figure 1.22: Conducting and Blocking IGCT

circuit of the blocking state is as shown in Fig. 23. Fig. 22 is identical to the conducting and blocking states of GTOs. The major difference with IGCT is that the device can transit from conducting state to blocking state instantaneously. The GTO does so via an intermediate state as illustrated in Fig. 18. In IGCT technology, elimination of the GTO zone is achieved by quickly diverting the entire anode current away from the cathode and out of the gate. The device becomes a transistor prior to it having to withstand any blocking voltage at all. Turn-off occurs after the device has become a transistor, no external dv/dt protection is required. IGCT may be operated without snubber like IGBT or MOSFET. Fig. 24 shows the turn-off process of an IGCT. Notice

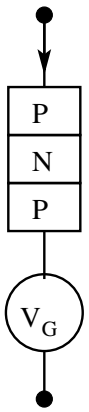

Figure 1.23: Equivalent Circuit of a Blocking IGCT

the absence of the GTO zone. The device behaves like a BJT right from the

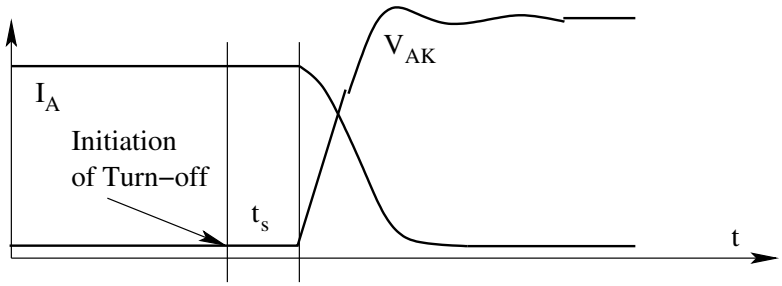

Figure 1.24: Turn-off Process of an IGCT

instant of initiation of turn-off. It is the pnp transistor of the IGCTs regenerative transistor pair which blocks after the npn transistor has been turned off with unity gain. On account of this unity gain turn-off, it is necessary for the gate drive circuit to handle the full anode current and to do so quickly. The key to IGCT design lies in very low inductance gate circuits. These may require coaxial devices and multilayer circuit boards. One more important feature of the IGCT is that it behaves more like a digital than an analog device. There is no control of the rate-of-change-of-anode voltage or current from the gate. The rate of rise of the anode voltage is caused by the turn-off of the open base pnp transistor and is typically set at about 3000V/μS. Thus the turn-off dv/dt cannot and need not be gate controlled (in contrast to GTO and IGBT). The inherent di/dt capability of IGCT is high. However, the parallel freewheeling diode does not have unlimited di/dt. It is for this reason that the turn-on di/dt of the IGCT has to be limited. This is one of the major differences between IGBT and IGCT. IGCT must have an external di/dt snubber. IGBT can limit di/dt via gate control. A typical snubber configuration is shown in

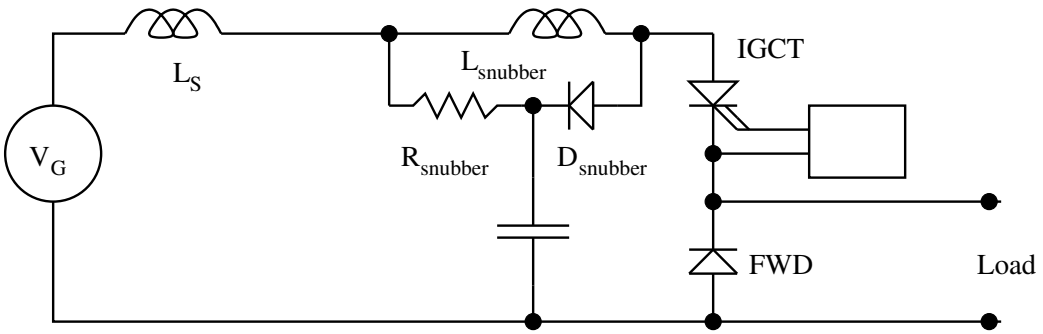

Figure 1.25: di/dt Snubber for the IGCT

Fig. 25. The IGCT can be turned on like a GTO with relatively low gate current. Then it is subject to the same di/dt limitations as a thyristor. It can also be turned on like a transistor, when the NPN transistor is driven hard. In such a case, the device has an order of magnitude better di/dt capability. Typically a hard turn-on IGCT exhibits a monotonically falling anode voltage, compared to a soft turn-on IGCT that exhibits an oscillatory drop in anode voltage during turn on.

1.12 Comparisons

Table 1 gives a comparison between GTO and IGCT devices. Table 2 gives the comparison of performance between IGCT and IGBT.

1.13 Thermal Design of Power Switching Devices

The cross section of a power switching device (a diode) and its thermal model are shown in Fig. 26. We have seen that the real power switching devices dissipate energy unlike the ideal switching devices. These losses that take place in the device are

- Conduction loss
- Blocking loss
- Turn-on loss
- Turn-off loss

All these energy losses in the device originate at the junction. Unless these losses are carried away from the junction, the temperature of the device junction will rise without limit and eventually destroy the device. In this section we see the basics of the thermal process in the device. The thermal model

Table 1.1: Comparison of GTO and IGCT

3 kA, 4500V, 125 $°C$	GTO 5SGA 30J4502	IGCT 5SGY30J4502
On State Voltage V_{tm}	4V	2.1V
Maximum Turn-on di/dt	500A/μs	3000A/μs
On State Loss at 1 kA dc	2600W	1500W
Turn-on Energy E_{on}	5 J	0.5 J
Turn-on Energy E_{off}	12 J at 6 μF	10 J at 0 μF
Snubber Requirement C_s	6 μF/300nH	0 μF
RMS Current I_{rms} at $T_C = 85°C$	1460A	1800A
Peak Turn-off Current I_{tgq}	3 kA at 6μF	3 kA snubberless 6 kA at 6μF
Gate Drive Power at 500 Hz, 1150A rms	80W	15W
Maximum Turn-off dv/dt	1000V/μs	3000V/μs
Storage time t_s	20μs	1μs
I_{gt} at 25$°C$	3A	0.3A
Gate Stored Charge Q_{gq}	8000μC	2000μC
Typical I_G at 40$°C$	12A	2A

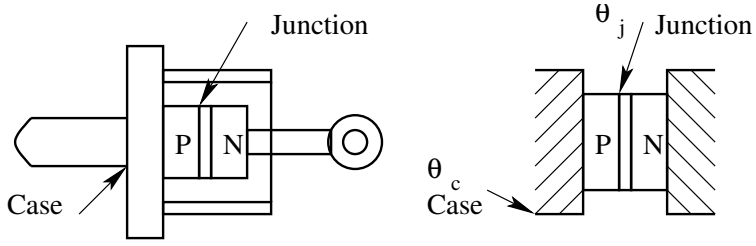

Figure 1.26: A PN Diode and its Thermal Model

thus established may be used to design heat sinks for the device to limit the temperature rise of the device junction. Part of this heat generated at the junction increases the temperature of the junction and the rest flows out of the junction onto the case of the device and therefrom to the environment of the device.

1.13.1 Thermal model of the device

Let P(t) be the power dissipated in the junction. Let the initial temperature of the junction and the case be $\theta_j(0)$ and $\theta_c(0)$ respectively in $°C$. In time "dt" let the increase in temperature of the junction and the case be $d\theta_j(t)$ and $d\theta_c(t)$ respectively in $°C$. J is the calorific equivalent of joule. For heat balance in time dt,

Table 1.2: Comparison of IGCT and IGBT

Parameter	IGCT Reverse Conducting 91 mm	IGBT 3x1200A Modules
On State Voltage at 3600 A	2.8V	5.7V
E_{on} at 1800V/3600A/(2000A/μs)	0.5 J	12-20 J
E_{off} at 1800V/3600A/0μF	9 J at 6 μF	9 J
Total Switching Loss	10J	20 - 30 J

- PJdt = Heat generated in the junction in time dt
- $msd\theta_j$ = Heat retained in the junction in time dt
- m = mass of the semiconductor material in Kg
- s = specific heat of the junction material Cal/Kg/°C.
- $K[\theta_j(t) - \theta_c(t)]$ = Heat taken away from the junction to case in time dt
- K = thermal conductivity from junction to case in Cal/°C/sec

The above heat balance equation may be rearranged as follows,

$$PJdt = msd\theta_j(t) + K[\theta_j(t) - \theta_c(t)]dt \tag{1.2}$$

$$P = \frac{ms}{J}\frac{d\theta_j}{dt} + \frac{K}{J}[\theta_j(t) - \theta_c(t)] \tag{1.3}$$

For the purpose of simple analysis we may assume that the case temperature $\theta_c(t)$ to be constant at θ_c (we will see how to achieve this later). We may further define a new variable as the temperature difference between the junction and the case $\theta_{jr}(t)$.
In the new variable ,

$$P = C_{th}\frac{d\theta_{jr}}{dt} + \frac{1}{R_{th}}\theta_{jr} \; ; \quad C_{th} = \frac{ms}{J} \; ; \quad R_{th} = \frac{J}{K} \tag{1.4}$$

C_{th} = Thermal Capacity of the Junction in $J/°C$ or $J/°K$.
R_{th} = Thermal Resistance of the Junction in $°C/W$ or $°K/W$.
The above differential equation relates the thermal behaviour of the junction, and when solved will give the junction temperature rise as a function of time.

1.13.2 Steady state temperature rise

Under steady state, the above equation reduces to

$$P_{av} = \frac{1}{R_{th}}\theta_{jr} \; ; \quad \theta_{jr(av)} = P_{av}R_{th} \tag{1.5}$$

1.13.3 Transient temperature rise

Under transient conditions the differential equation of the thermal model has to be solved to obtain the temperature rise as a function of time. However, if we consider transients of very small duration (as happens in power switches during switching), P(t) may be considered constant. Then θ_{jr}, may be solved as

$$\theta_{jr}(t) = P\ R_{th}(1 - e^{t/\tau})\ ; \tau = R_{th}C_{th} \tag{1.6}$$

τ = Thermal time constant of the junction
The quantity $R_{th}(1-e^{t/\tau})$ is defined as the transient thermal impedance $Z_{th}(t)$ of the device and is usually provided by the device manufacturer. Then the temperature rise may be conveniently calculated.

$$\theta_{jr} = P_{av}Z_{th} \tag{1.7}$$

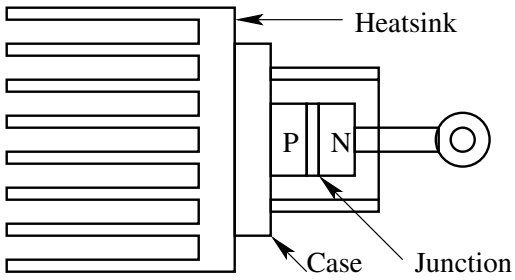

Figure 1.27: Power Switching Device Mounted on the Heatsink

1.13.4 Equivalent circuit of the thermal model

The thermal model is put into the equivalent circuit shown in Fig. 28 for convenience. In practice to validate our assumption that the case temperature is constant, the device is mounted on a massive heatsink as shown in Fig. 27. The thermal model may be extended as shown in Fig. 28, to take into account the heatsink also.

1.14 Intelligent Power Modules (IPM)

The introduction of MOS technology in the fabrication of power semiconductors has created great device and application advantages. Of particular interest is the current modern power device namely the insulated gate bipolar transistor (IGBT). Currently IGBTs are taking several applications away from MOSFET modules at the low power high frequency end and from bipolar

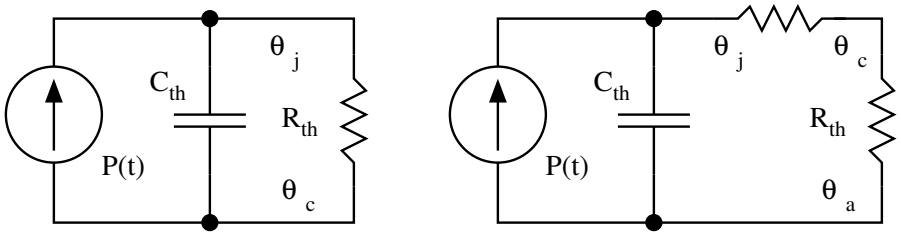

Figure 1.28: Eqivalent Circuit of the Thermal Model

Darlington modules at the high power medium frequency end of the application spectrum. With such technology, it has become possible to integrate the peripheral devices to be built into the power modules. Such devices are classified as Intelligent Power Modules (IPM). The different levels of integration achieved and achievable are shown in Fig. 29. The IPM family provides the

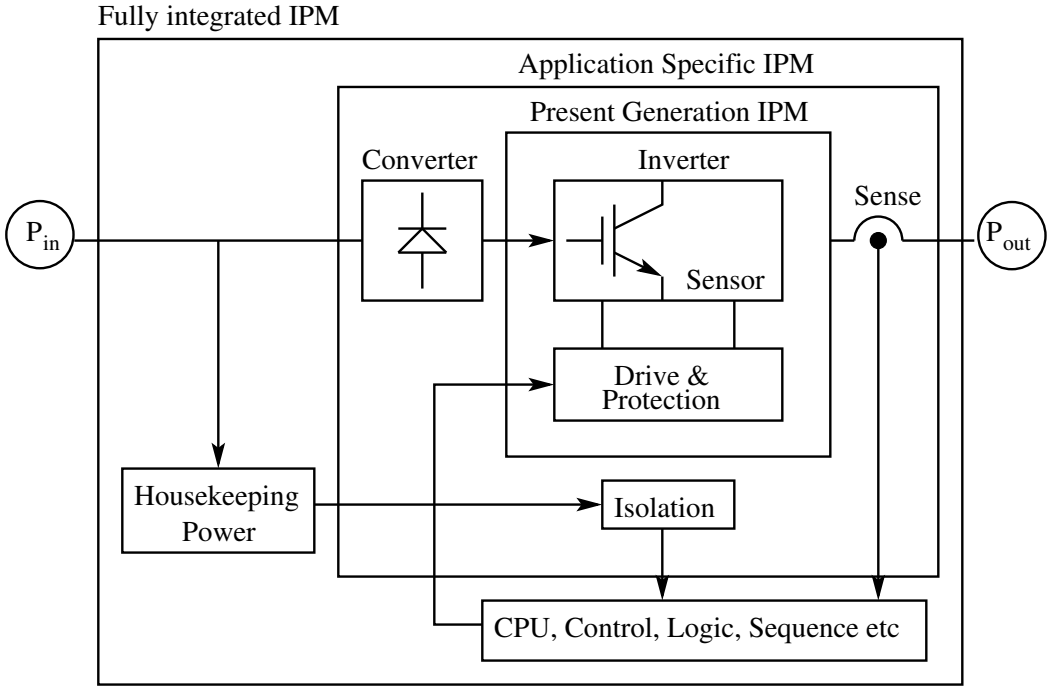

Figure 1.29: Different Levels of Integration in IPMs

user with the additional benefits of equipment miniaturization and reduced design cycle time. They include gate drive circuit and protection circuits for short circuit protection, over-current protection, over-temperature protection, and gate drive under-voltage lockout. IPM has sophisticated built-in protection circuits that prevent the power devices from being damaged in case of system malfunction or overload. Control supply under-voltage, over-temperature,

over-current, and short-circuit protection are all provided by the IPMs internal gate control circuits. A fault output signal is provided to alert the system controller if any of the protection circuits are activated. Fig. 30 is a block diagram of the IPM's internally integrated functions. This diagram also shows the isolated interface circuits and isolated control power supply that must be provided to the IPM. The IPM's internal control circuit operates from an iso-

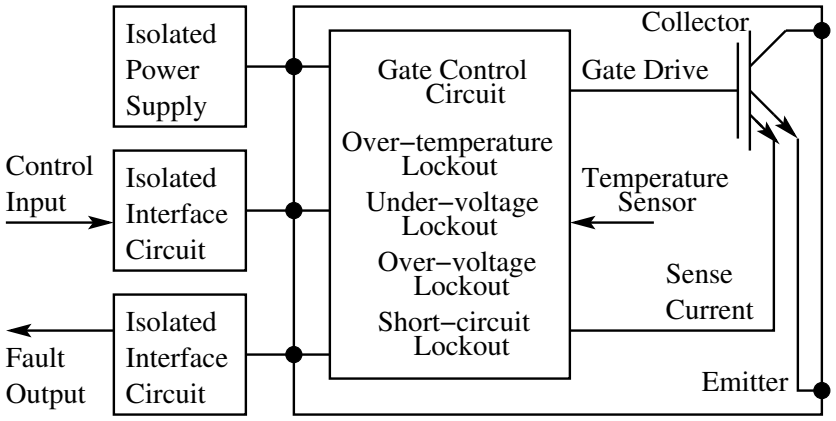

Figure 1.30: Functional Diagram of an IPM

lated 15V DC supply. If for any reason, this voltage falls below the specified under-voltage trip level, the power devices will be turned off and a fault signal generated. Small glitches less than the specified t_{dUV} in length will not affect the operation of the control circuit and will be ignored by the under-voltage protection circuit. In order for normal operation to resume, the control supply voltage must exceed the under-voltage reset level (UV_r). Operation of the under-voltage protection circuit will also occur during power up and power down situation. The system controller must take into account the fault output delay (t_{fo}).

Application of the main bus voltage at a rate greater than 20V/μs before the control power supply is on and stable may cause the power device to fail. Voltage ripple on the control power supply with dv/dt in excess of 5V/μs may cause a false trip of the under-voltage lockout. The IPM has a temperature sensor mounted on the isolating base plate near the IGBT chips. If the temperature of the base plate exceeds the over-temperature trip level (OT), the internal control circuit will protect the power devices by disabling the gate drive, and ignoring the control input signal till the normal-temperature condition is restored. The over-temperature reset level is (OT_r). The over-temperature function provides effective protection against overloads and cooling system failures. Tripping of the over-temperature protection is an indication of stressful operation. Repetitive tripping is an indication that the above symptoms exist. The IPM uses current sense IGBT chips. If the cur-

rent through the IPM exceeds the specified over-current trip level (OC), for a period longer than $t_{off(OC)}$, the IPM's internal control circuit will protect the power device by disabling the gate drive and generating an output signal. If a

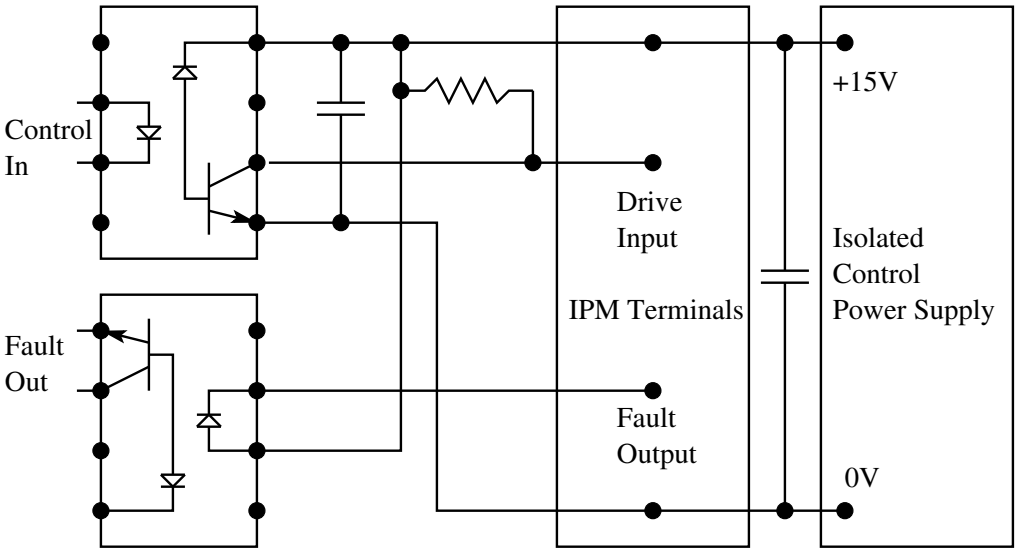

Figure 1.31: Typical Interface Circuit to an IPM

load short circuit occurs or the system controller malfunctions causing a shoot through, the IPM's built-in short circuit protection will prevent the IGBTs from being damaged. When the current, through the IGBT exceeds the short circuit trip level (SC), an immediate controlled shut down is initiated and a fault output is generated. The IPMs employ for short circuit protection actual current measurements to detect dangerous conditions. This type of protection is faster and more reliable than the conventional out-of-saturation protection schemes. It is necessary to reduce the time between short-circuit detection and short-circuit shut down. In certain IPMs this time may be as small as 100 ns. Tripping of the over-current and short-circuit protection indicates stressful operation of the IGBT. Repetitive tripping is to be avoided. High surge voltage occurs during emergency shut down, Low inductance bus bars and snubbers are essential. It is necessary to coordinate the peak current and the maximum junction temperature. Depending on the power circuit configuration of the IPM, one, two, or four isolated power supplies are required for the IPM's internal drive and protection circuits. In high power 3 phase inverters using single or dual type IPMs, it is a good practice to use six isolated power supplies. In these high current applications, each low side device must have its own isolated control power supply in order to avoid ground loop noise problems. The supplies should have an isolation voltage rating of at least twice the IPM's V_{CES} rating. Using bootstrap technique is not recommended for the control power supply. A typical interface circuit is shown in Fig. 31. The

link to the data sheet of a typical IPM PM75CVA120 is given in Appendix F. IPMs can be profitably employed in practically all of the power supply and drive applications listed below at appropriate power levels to achieve higher levels of integration.

1. Uninterruptible Power Supply
   (A) Low dc voltage ($< 400V$), Low Power ($< 10kW$), High Switching Frequency ($> 20kHz$)
   (B) Half Bridge IPMs
2. Welding Power Supply
   (A) AC input power, Low voltage, High Current DC Output Power, Low Power ($< 10kW$), High Switching Frequency ($> 20kHz$)
   (B) Half Bridge IPMs
3. Constant Voltage Constant Frequency Power Supply (CVCF) Auxiliary Power
   (A) Battery Input ($< 400V$), Medium Power ($< 200kW$), Medium Switching Frequency ($< 10kHz$)
   (B) Half Bridge IPMs
4. Switched Mode Power Supplies - Telecom
   (A) 3 Phase Input Power, Medium Voltage DC Link ($< 800V$), Medium Output Power ($< 100kW$)
   (B) Six Packs for Front End and Half Bridge for Rear End

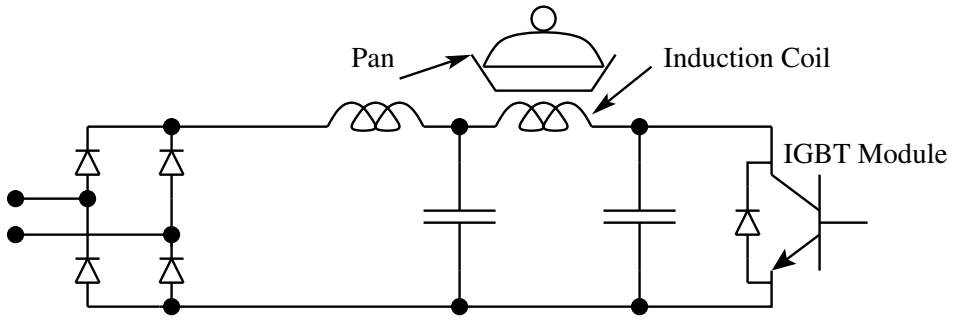

Figure 1.32: Induction Oven

5. Induction Oven/Heater - Fig. 32
   (A) Single Phase Input Power, Low output Power ($< 5kW$), High Switching Frequency ($> 100kHz$)

(B) Three Phase Input Power, Medium Output Power ($< 100kW$), High Switching Frequency ($> 100kHz$)

(C) Half Bridge IPMs or Single Switch IPMs

6. Medical Equipment, High Voltage Power Supplies, Drives

   (A) Single Phase Input Power, Low Voltage DC Link ($< 200V$), High Switching Frequency ($> 100kHz$), Low Output Power ($< 5kW$)

   (B) Half Bridge IPMs

7. Variable Voltage Variable Frequency Drives (VVVF)

   (A) Three phase Input Power, High Output Power (100s of kW), Medium to Low Switching Frequency (1 kHz to 10s of kHz)

   (B) Six Pack IPMs

8. Machine Tool Drives

   (A) Three phase Input Power, Medium Output Power (10s of kW), Medium to Low Switching Frequency (1 kHz to 10s of kHz)

   (B) Six Pack IPMs

9. HVAC Compressor Drives

   (A) Single phase Input Power, Low Output Power (fractional kW), High Switching Frequency ($> 20kHz$)

   (B) Application Specific IPMs

10. Elevator, Crane Drives

    (A) Three phase Input Power, High Output Power (100s of kW), Medium to Low Switching Frequency (1 kHz to 10s of kHz)

    (B) Half Bridge IPMs.

1.15 Illustrated Examples

1. Show practical realizations with electronic switches (diodes, BJTs, SCRs, MOSFETs, GTOs, IGBTs) to meet the operating points shown in Fig. 1.1

2. For the switching devices shown in Fig. 1.2 (a) and (b), show on the v-i plane, the possible steady state operating points.

3. The power converter in Fig. 3 has two power switching devices namely - T_1P and T_2P. The source voltage is 50V. The inductor current is steady 5A without any ripple. On the v-i plane mark the operating points of the switches T_1P and T_2P.
   T_1P may be realized by a controlled power-switching device (BJT, MOSFET or IGBT). T_2P may be realized by an uncontrolled diode.

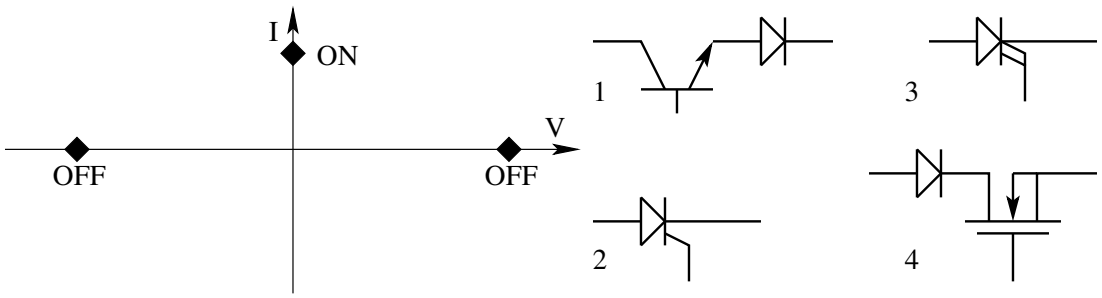

Fig. Ex 1.1: Composite Switches

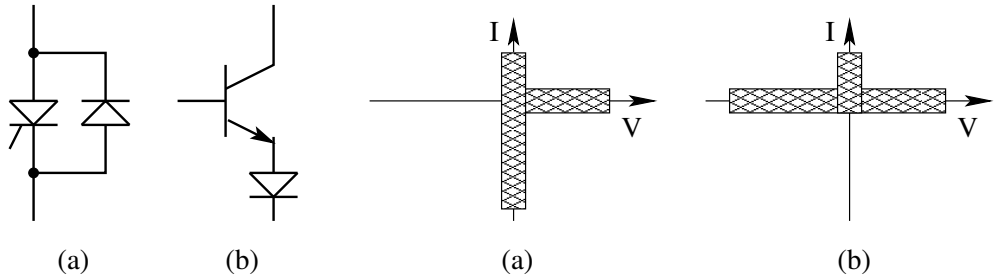

Fig. Ex 1.2: Operating Points of Composite Switches

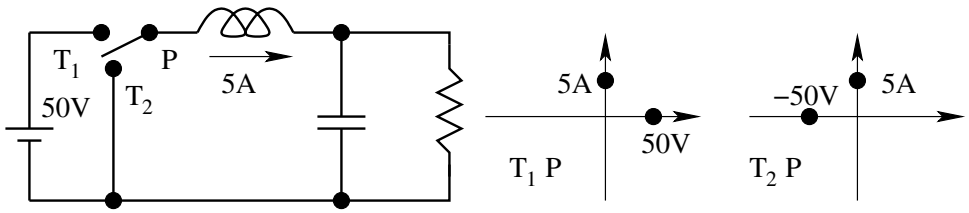

Fig. Ex 1.3: Realisation of T_1P and T_2P.

4. The current through and the voltage across a power device is shown in Fig. 4. Evaluate the average current and the rms current rating of the device. Evaluate the conduction loss in the device.
   $I_{av} = 2.5A$
   $I_{rms} = 4.1A$
   Conduction loss = 2.5W

5. In an inverter, the current through the active device is measured and found to be as shown in Fig. 5. Evaluate the average current rating of the switch. The switching frequency may be considered very high compared to the fundamental frequency of the output current. If the power device is a power transistor with a Vce drop of 1.2 V, evaluate the conduction

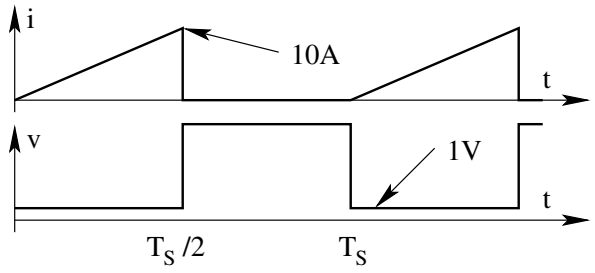

Fig. Ex 1.4: Average Current, RMS Current and Conduction Loss.

loss in the transistor.

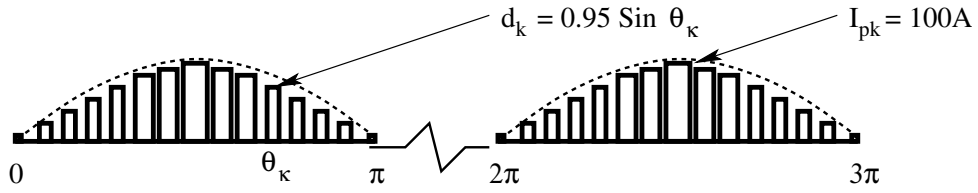

Fig. Ex 1.5: Average Current, RMS Current and Conduction Loss.

$I_{av}(k) = I_{pk}Sin(\theta_k)0.95Sin(\theta_k)$

$$I_{av} = \frac{1}{2\pi} \int_0^{\pi} i_{av}(k)d\theta(k)$$

$I_{av} = 23.75A$
$I_{rms} = 1.2A$
Conduction loss = 28.5W

6. The Thyristor SKAT28F is used in an application carrying half sinusoidal current of period 1 mS and a peak of 100 A as shown in Fig. 6. The Thyristor may be modeled during conduction to have a constant voltage drop of 1.1 V and a dynamic resistance of 8 mΩ. Evaluate the average conduction loss in the device for this application.

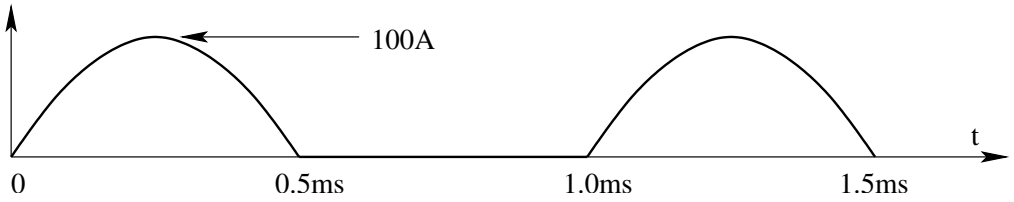

Fig. Ex 1.6: Loss Calculation.

$V_t = 1.1V$; $R_d = 0.008\Omega$; $I_{av} = 31.83A$; $I_{av} = 50A$
$P = (I_{av}V_t) + I_{rms}^2 R_d$; $P = 55W$

7. Figure 7 shows the periodic current through a power-switching device in a switching converter application.

   (A) Evaluate the average current through the device.

   (B) Evaluate the rms current through the device.

   (C) A BJT with a device drop of 1.2 V and a MOSFET with an of 150 $m\Omega$ are considered for this application. Evaluate the conduction loss in the device in either case.

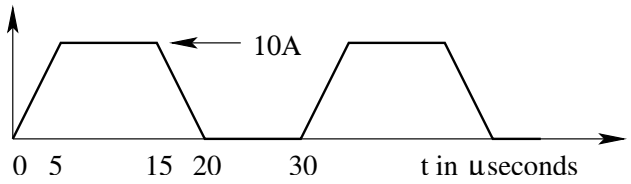

Fig. Ex 1.7: Loss Calculation.

$I_{av} = 5A$; $I_{rms}^2 = 44.44A$; $I_{rms} = 6.67A$
Losses with BJT = 6W
$V_{ce(sat)} = 1.2V$; $R_{ds(on)} = 0.15\Omega$
Losses with MOSFET = 6.67W

8. A disc type Thyristor is shown with its cooling arrangement in Fig. 8. The device is operating with a steady power dissipation of 200W.

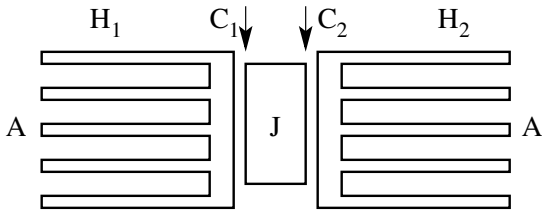

Fig. Ex 1.8: Thermal Design.

   (A) Evaluate the steady state temperature rise of the junction.

   (B) With the above steady power dissipation of 200W, find the excess power dissipation allowable for 10 ms, if the junction temperature rise is not to exceed 90C.

$R_{th}JC_1 = 0.3°C/W$; $R_{th}JC_2 = 0.3°C/W$; $R_{th}C_1H_1 = 0.05°C/W$;
$R_{th}C_2H_2 = 0.05°C/W$; $R_{th}H_1A = 0.5°C/W$; $R_{th}H_2A = 0.4°C/W$;

$Z_{th}(10ms) = 0.05°C/W$; $P = 200W$; $T_{max} = 90°C$;
$R_{theq} = 0.4\Omega$;
$T_{rise} = 79.69°C$;
$P_{pulse} = 206.25W$; Excess rise = $10.31°C$;

9. A power diode (ideal in blocking and switching) shown in Fig. 9, is capable of dissipating 75 W. For square wave operation, it is rated for peak current of 100 A and 135 A at duty ratios 0.5 and 0.33 respectively. Evaluate the ON state model of the diode.

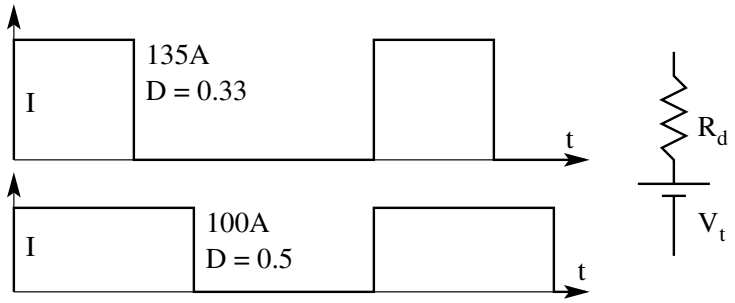

Fig. Ex 1.9: Thermal Design.

For D = 0.5: $I_{av} = 50A$; $I_{rms} = 70.7A$;
For D = 0.33: $I_{av} = 44.6A$; $I_{rms} = 77.6A$;
$50V_t + 4998.9R_d = 75$; $44.6V_t + 6021.8R_d = 75$;
$V_t = 0.98V; R_d = 0.005\Omega$
The above diode while dissipating 40W at an ambient temperature of $35°C$, is running with a case temperature of $75°C$ and $125°C$ respectively. Evaluate the thermal resistances of the device.
$T_c = 75°C; T_j = 125°C; T_a = 35°C; P = 40W$;
$R_{jc} = 1.25°C/W; R_{ca} = 1°C/W$

10. The BJT D62T–75 is used to switch resistive load as shown in Fig. 10. Sketch the switching waveforms I_b, V_{ce}, and I_c as a function of time for both ON/OFF and OFF/ON transitions. Assume ideal switching behaviour.
$V_{ce(sat)} = 1.25V$; $I_{ceo} = 3mA$; $t_f = 0.6\mu s$; $t_r = 1.2\mu s$

    (A) Evaluate the conduction loss in watts.

    (B) Evaluate the blocking loss in watts.
    Conduction Loss = 93.75 W;
    Blocking Loss = 0.75W

    (C) Evaluate the peak power dissipation during switch in transients.

    (D) Evaluate the energy dissipation during the transitions.
    Peak Power = 4687.5 W;

Energy ON/OFF = 0.0019J;
Energy OFF/ON = 0.0038J

(E) If the load resistance has an inductance of 2 mH, show the and waveforms during the ON/OFF transient.

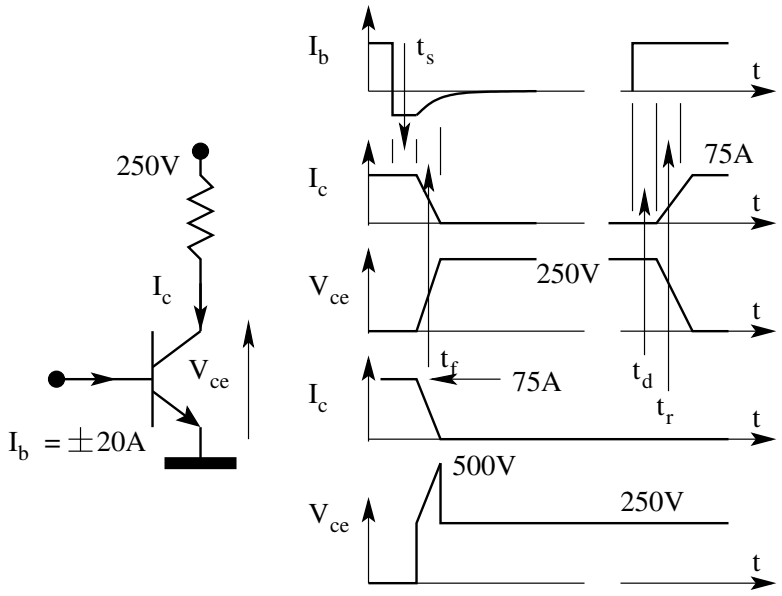

Fig. Ex 1.10: Switching Transients.

1.16 Problem Set

1. A power-switching device is rated for 600V and 30A. The device has an on state voltage drop of 1.5V to 2.4V for conduction current in the range of 15 to 30A. The device has a leakage current of 5 mA while blocking 600V. Evaluate

   (A) the maximum conduction loss,

   (B) maximum blocking loss, and

   (C) ratio of the conduction and blocking loss with maximum possible power that may be controlled by this switch and make your comment on the result.

2. A power-switching device is ideal in conduction and blocking (0 V during conduction and 0 A in blocking). It is used in a circuit with switching voltages and currents as shown. The switching waveforms under resistive loading and inductive loading are shown in Fig. 2. The switching times t_r and t_f are 100 ns and 200 ns respectively. Evaluate

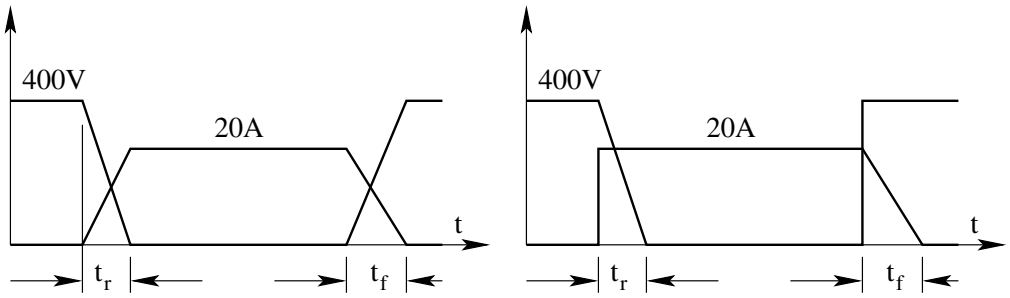

Fig. P 1.2: Switching Waveforms under Resistive and Inductive Switching

(A) the switch-on and switch-off energy loss (in Joule) for resistive loading,

(B) the switch-on and switch-off energy loss (in Joule) for inductive loading, and

(C) the resistive and inductive switching losses in W for a switching frequency of 100 kHz.

3. A power MOSFET has an $r_{ds(on)}$ of 50 $m\Omega$. The device carries a current as shown in Fig. 3. Consider the switching process to be ideal and evaluate the conduction loss in the device. (It is necessary to evaluate the rms current through the device. Explore if you can simplify the evaluation of rms value by applying superposition).

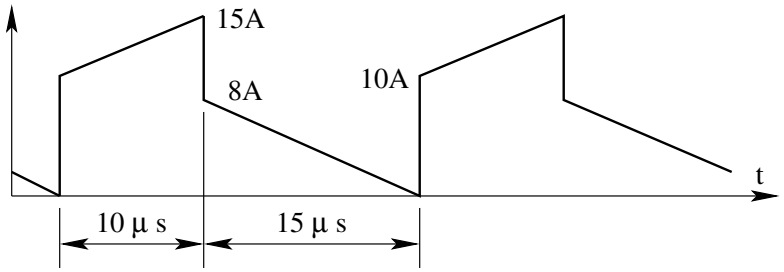

Fig. P 1.3: Current through the MOSFET

4. The diode 20ETS08 is a 20 A, 800 V rectifier diode. It has a voltage drop of 0.8 V at 2 A and 1.2 V at 30A. Fit a piece-wise linear model for this diode consisting of a cut-in voltage and dynamic resistance. With this piece-wise model evaluate its conduction loss for a 30A peak half sine wave of current.

5. For the IGBT device HGTG30N120D2 (1200V, 30A, Harris make), find out the conduction loss at rated current and blocking loss at rated voltage

and comment on the same. It is observed from the data sheet that the device withstands short circuit for $6\mu s$ at V_{ge} of 15 V and for $15\mu s$ at V_{ge} of 10 V. Comment on this observation.

The thermal process is predominantly a first-order process and is similar in most applications. The thermal model is related to the physical process of evacuation of heat to the ambient. This problem set is to apply the simple steady state and transient thermal models to evaluate temperature rise, thermal resistance, temperature ripple, etc.

6. The temperature of an oil-cooled transformer when disconnected fell from $75°C$ to $25°C$ in 2 hr. Evaluate the cooling time constant of the transformer.

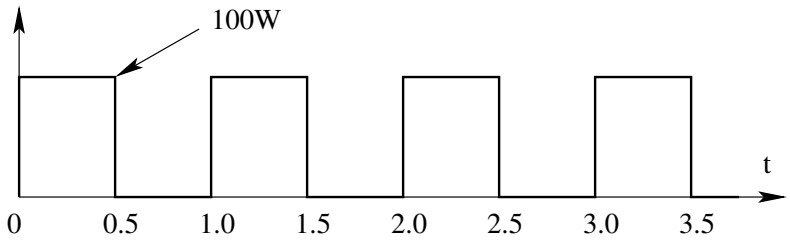

Fig. P 1.8: Periodic Power Dissipation in the Switch

7. A power-switching device dissipates an average power of 100 W and is mounted on a heatsink. The temperature rise of the heatsink is $40°C$ in an ambient of $40°C$. The junction is at a temperature of $100°C$. Evaluate the case-to-ambient and junction-to-heatsink thermal resistances.

8. Figure 8 shows the periodic power dissipation in a power device. The junction-to-case and case-to-ambient thermal resistances are respectively $0.4°C/W$ and $0.6°C/W$. The thermal time constant is 0.4 s. The ambient temperature is $50°C$. Evaluate of the steady-state maximum and minimum temperature of the junction and the case.

9. A heatsink has a radiation surface area of $100cm^2$ and convection surface area of $500cm^2$. The radiation dissipation constant is $0.015W/°C/cm^2$. The convection dissipation constant is $0.075W/°C/cm^2$. The heatsink has a mass of 0.2 kg and a specific heat of 0.2 kCal/kg/$°C$. Evaluate the thermal resistance of the heatsink. Evaluate the thermal time constant of the heatsink.

10. In the above problem, when the convection process is blocked, evaluate the thermal resistance and the thermal time constant of the heatsink.

11. A power device is operating under certain conditions with a certain power dissipation of 100 W and a temperature rise of $80°C$ between the junction

and the ambient. The thermal time constant of the device together with the heatsink is 1 s. Under this condition, evaluate the excess pulsed power of duration 0.3 s if the peak temperature rise is not to exceed $100°C$

12. The MOSFET IRF540 is operating in a circuit with a power dissipation of 20 W. Evaluate the temperature rise of the junction without external heatsink and with an external heatsink of thermal resistance $2°C/W$.

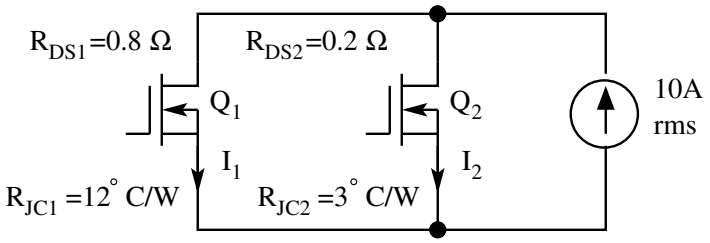

Fig. P 1.13: MOSFETs in Parallel

13. A composite switch (Q_1 and Q_2 in parallel) carrying a load current of 10A is shown in Fig. 13. The switches may be considered ideal in switching. The on-state resistances of the devices Q_1 and Q_2 are respectively 0.8Ω and 0.2Ω. The devices are mounted on a common heatsink held at a temperature of 80°C. Evaluate

    (A) $I_1(rms)$ and $I_2(rms)$

    (B) the average power dissipation (P_1 and P_2) in Q_1 and Q_2.

    (C) the junction temperatures of Q_1 and Q_2.

14. Figure 14 shows the voltage across and the current through a switch during off/on transition. The switch-on transition consists of two sub-intervals (rise time of 0.5 μs and a tail time of 2 μs).

    (A) Evaluate power in the device at t = 0.

    (B) Evaluate the power in the device at t = 0.5 μs.

    (C) Evaluate the power in the device at t = 2.5 μs.

    (D) Evaluate the power in the device as a function of time furing the rise time (P(t) for $0 \leq t \leq 0.5\mu s$).

    (E) Evaluate the peak power in the device during the rise time $0 \leq t \leq 0.5\mu s$.

    (F) Sketch P(t) for $0 \leq t \leq 0.5\mu s$

15. A composite switch used in a power converter is shown in Fig. 15. The periodic current through the switch is also shown. Evaluate

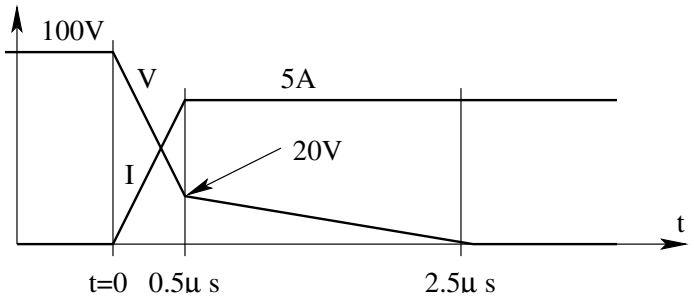

Fig. P 1.14: Switching Waveforms of the Device

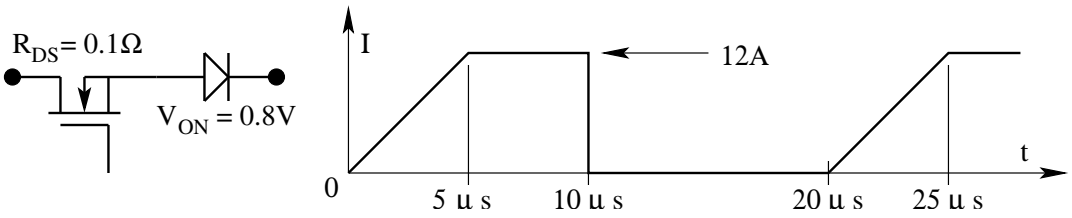

Fig. P 1.15: Current Through the Device

(A) the average current and rms current through the composite switch.

(B) the power loss in the MOSFET and the diode of the composite switch.

16. Visit a manufacturer's website, identify a controlled power switching device (BJT, or Darlington, or MOSFET, or IGBT) of rating $> 10A$ and $> 600V$. Download the datasheet and fill in the following.

(A) Manufacturer.

(B) Device and Type No.

(C) On-state voltage (V).

(D) Off-state current (A).

(E) Transient switching times (s).

(F) Maximum junction temperature (K).

(G) Recommended drive conditions (?).

(H) Conduction loss at rated current (W).

(I) Blocking loss at rated voltage (W).

(J) Switching energy loss (J).

Chapter 2

Reactive Elements in Power Electronic Systems

2.1 Introduction

The conditioning of power flow in PES is done through the use of electromagnetic and reactive elements (inductors, capacitors and transformers). In this section the basics of electromagnetics is reviewed. The type of capacitors popular in power electronic applications are also given. They are formulated in such a way as to be useful for the design of inductors and transformers.

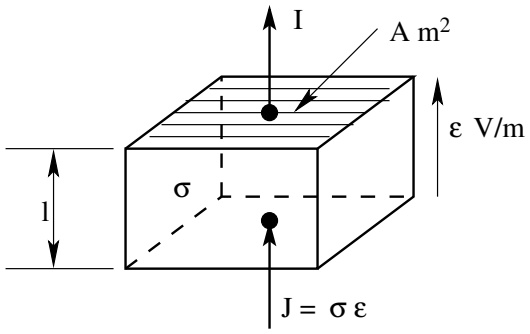

Figure 2.1: Conduction Process

2.2 Electromagnetics

The voltage across and current through a conducting element is related through Ohm's law. This law may be stated as follows. When an electric field (of intensity ϵ V/m) is set up across a conducting material (of conductivity σ $1/\Omega$ m), there is an average flow of electrical charge across the conducting material

(of current density J A/m^2). This is shown in Fig. 1.

$$J = \sigma\epsilon \tag{2.1}$$

When expressed in terms of element voltage and current, this reduces to the familiar statement of Ohm's law.

$$I = \frac{V}{R} \tag{2.2}$$

$$R = \frac{l}{\sigma A} \tag{2.3}$$

In comparison with conducting materials, the property of magnetic materials may be stated as follows. When a magnetic field (of intensity H A/m) is set up across a magnetic material, of magnetic permeability (μ H/m), a magnetic flux of density (B Tesla) is set up in the magnetic material as shown in Fig. 2.

$$B = \mu H \tag{2.4}$$

The above equation, in terms of the magnetomotive force (mmf) F and the

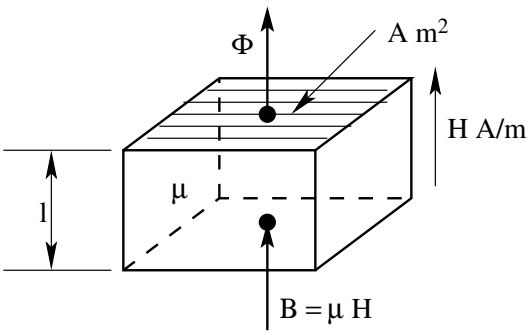

Figure 2.2: Magnetisation Process

flux Φ in the magnetic circuit, reduces to

$$\Phi = \frac{F}{R} \tag{2.5}$$

where, R = reluctance of the magnetic circuit = $l/A\mu$.
The above relationship is analogous to Ohm's law for magnetic circuits. The magnetic permeability μ of any magnetic material is usually expressed relative to the permeability of free space ($\mu_o = 4\pi 10^{-7}$ H/m). The reluctance of the magnetic circuit is given by

$$R = \frac{l}{A\mu_o\mu_r} \tag{2.6}$$

Electromagnetic circuit elements consist of an electric circuit and a magnetic circuit coupled to each other. The electric current in the electric circuit sets up

the magnetic field in the magnetic circuit with resultant magnetic flux. Seen as an electrical circuit element, the electromagnetic element possesses the property of energy storage without dissipation. Ampere's law and Faradays law

Figure 2.3: Magnetomotive Force

relate the electric and magnetic circuits of the electromagnetic element. Ampere's law states that the mmf in a magnetic circuit is equal to the electric current enclosed by the magnetic circuit. For example for the electromagnetic circuits shown in Fig. 3, the magnetic circuit mmfs are I and NI respectively. With further assumption that the magnetic material is isotropic and homogenous, and that the magnetic flux distribution is uniform, we may relate the magnetic flux in the magnetic circuit as

$$\Phi = \frac{\Sigma I}{R} = \frac{NI}{R} \tag{2.7}$$

The above equation may conveniently be put in the equivalent circuit shown

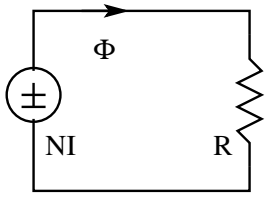

Figure 2.4: Magnetic Equivalent Circuit

in Fig. 4. Faraday's law relates the voltage induced in an electric circuit that is coupled to a magnetic circuit.

$$v = N\frac{d\Phi}{dt} = \frac{N^2}{R}\frac{di}{dt} \tag{2.8}$$

The quantity N^2/R is defined as the inductance of the electric circuit. Thus an electromagnetic circuit provides us an electric circuit element (inductor). The voltage across an inductor is directly proportional to the rate of rise of current through it. The energy stored in the magnetic circuit is

$$E = \frac{1}{2}LI^2 = \frac{1}{2}\frac{F^2}{R} = \frac{1}{2}\Phi^2 R = \frac{1}{2}\Phi F \tag{2.9}$$

The equivalent circuit of an inductor showing both its electric and magnetic

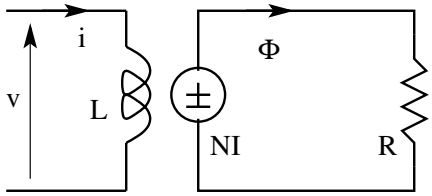

Figure 2.5: Electromagnetic Circuit

parts may be conveniently represented as shown in Fig. 5. However in practice, the inductor will have certain parasitic resistance (of the wire in the electric circuit) and magnetic leakage (in the magnetic circuit). These non-idealities may conveniently be incorporated in the equivalent circuit as shown in Fig. 6. The design of an inductor involves the design of the electrical (Number of turns and wire size) and the magnetic (geometry of the magnetic core and its required magnetic property) circuit.

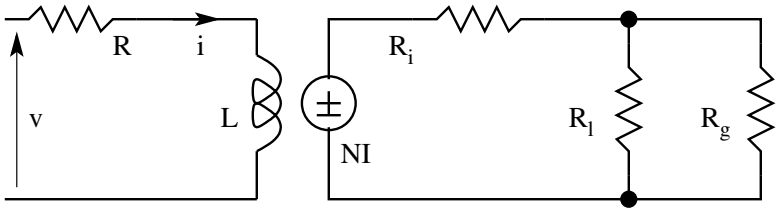

Figure 2.6: Electromagnetic Circuit with Parasitics

2.3 Design of Inductor

The inductor consists of a magnetic circuit and an electrical circuit. The design requires,

- The size of wire to be used for the electric circuit, to carry the rated current safely.
- The size and shape of magnetic core to be used such that
  - The peak flux is carried safely by the core without saturation.
  - The required size of the conductors are safely accommodated in the core.
- The number of turns of the electric circuit to obtain the desired inductance.

2.3.1 Material constraints

Any given wire (conducting material) can only carry a certain maximum current per unit cross section of the wire size. When this limit is exceeded, the wire will overheat from the heat generated (I^2R) and melt or deteriorate. The safe current density for the conducting material is denoted by J A/m^2. Any magnetic material can only carry a certain maximum flux density. When this limit is exceeded, the material saturates and the relative permeability drops substantially. This maximum allowable flux density for the magnetic material is denoted by B_m T.

2.3.2 Design Relationships

In order to design an inductor of L Henry, capable of carrying an rms current of I_{rms} and peak current of I_p [4],

- Let the wire size be a_w m^2.

$$a_w = \frac{I_{rms}}{J} \tag{2.10}$$

- Let the peak flux density in the core of area (A_C) be B_m on account of the peak current I_p in the inductor.

$$LI_p = N\Phi_p = NA_CB_m \tag{2.11}$$

- The winding of the inductor is accommodated in the window of the core. Let the window area (A_W) be filled by conductors to a fraction of k_w.

$$k_wA_W = Na_w = N\frac{I_{rms}}{J} \tag{2.12}$$

  Cross-multiplying Eq. (11) and Eq. (12), we get

$$LI_pN\frac{I_{rms}}{J} = NA_CB_mk_wa_w \tag{2.13}$$

$$LI_pI_{rms} = k_wJB_mA_CA_W \tag{2.14}$$

The above equation may be interpreted as a relationship between the energy handling capacity ($0.5LI^2$) of the inductor to the size of the core (A_CA_W), the material properties (B_m, J), and our manufacturing skill (k_w).

- k_w depends on how well the winding can be accommodated in the window of the core. k_w is usually 0.3 to 0.5.
- B_m is the maximum unsaturated flux is about 1 T for iron and 0.2 T for ferrites.
- J is the maximum allowable current density for the conductor. For copper conductors J is between 2.0 10^6 A/m^2 to 5.0 10^6 A/m^2.

2.3.3 Design steps

Input L I_p, I_{rms}, Core Tables, Wire Tables, J, B_m, k_w

1. Compute
$$A_C A_W = \frac{L\ I_p\ I_{rms}}{k_w\ B_m\ J} \tag{2.15}$$
2. Select a core from core tables with the required $A_C A_W$.
3. For the selected core, find A_C, and A_W.
4. Compute
$$N = \frac{L\ I_p}{B_m\ A_C} \tag{2.16}$$
Select nearest whole number of N^*.
5. Compute
$$a_w = \frac{I_{rms}}{J} \tag{2.17}$$
Select nearest whole number of wire guage and a_w^* from wire table.
6. Compute the required air gap in the core
$$l_g = \frac{\mu_o\ N^*\ I_p}{B_m} \tag{2.18}$$
7. Check the assumptions:
   - Core reluctance << Air gap reluctance;
   $$R_c << R_g\ ; \frac{l}{\mu_r}\ << \ l_g \tag{2.19}$$
   - No fringing:
   $$l_g\ << \ \sqrt{A_C} \tag{2.20}$$
8. Recalculate
$$J^* = \frac{I_{rms}}{a_w^*} \tag{2.21}$$
9. Recalculate
$$k_w^* = \frac{N^*\ a_w^*}{A_W} \tag{2.22}$$
10. Compute from the geometry of the core, mean length per turn and the length of the winding. From wire tables, find the resistance of winding.

Table 2.1: Wire Table

Nominal Diameter	Wire Size SWG	Outer Diameter	Resistance Ohm/km	Area mm^2
0.025	50	0.036	34026	0.000506
0.030	49	0.041	23629	0.000729
0.041	48	0.051	13291	0.001297
0.051	47	0.064	8507	0.002027
0.061	46	0.074	5907	0.002919
0.071	45	0.086	4340	0.003973
0.081	44	0.097	3323	0.005189
0.091	43	0.109	2626	0.006567
0.102	42	0.119	2127	0.008107
0.112	41	0.132	1758	0.009810
0.122	40	0.142	1477	0.011675
0.132	39	0.152	1258	0.013701
0.152	38	0.175	945.2	0.018242
0.173	37	0.198	735.9	0.02343
0.193	36	0.218	589.1	0.02927
0.213	35	0.241	482.2	0.03575
0.234	34	0.264	402.0	0.04289
0.254	33	0.287	340.3	0.05067
0.274	32	0.307	291.7	0.05910
0.295	31	0.330	252.9	0.06818
0.315	30	0.351	221.3	0.07791
0.345	29	0.384	183.97	0.09372
0.376	28	0.417	155.34	0.1110
0.417	27	0.462	126.51	0.1363
0.457	26	0.505	105.02	0.1642
0.508	25	0.561	85.07	0.2027
0.559	24	0.612	70.30	0.2452
0.610	23	0.665	59.07	0.2919
0.711	22	0.770	43.40	0.3973
0.813	21	0.874	33.23	0.5189
0.914	20	0.978	26.26	0.6567
1.016	19	1.082	21.27	0.8107
1.219	18	1.293	17.768	1.167
1.422	17	1.501	10.850	1.589
1.626	16	1.709	8.307	2.075
1.829	15	1.920	6.564	2.627
2.032	14	2.129	5.317	3.243
2.337	13	2.441	4.020	4.289
2.642	12	2.756	3.146	5.480
2.946	11	3.068	2.529	6.818
3.251	10	3.383	2.077	8.302
3.658	9	3.800	1.640	10.51
4.064	8	4.219	1.329	12.97

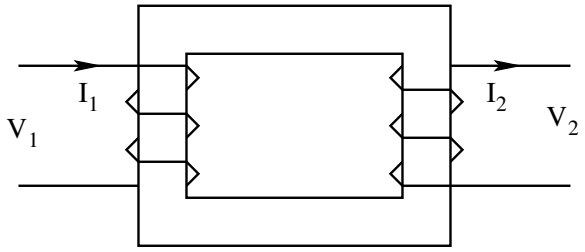

Figure 2.7: Electromagnetic Circuit of a Transformer

2.4 Design of Transformer

Unlike the inductor, the transformer does not store energy. The transformer consists of more than one winding. Also, in order to keep the magnetization current low, the transformer does not have air gap in its magnetizing circuit. Consider a transformer with a single primary and single secondary as shown in Fig. 7. Let the specifications be
Primary: V_1 volt; I_1 ampere;
Secondary: V_2 volt; I_2 ampere;
VA Rating: $V_1\ I_1 = V_2\ I_2$;
Frequency: f Hz

For square wave of operation, the voltage of the transformer is

$$V_1 = 4\ f\ B_m\ A_C\ N_1\ ;\ V_2 = 4\ f\ B_m\ A_C\ N_2 \tag{2.23}$$

The window for the transformer accommodates both the primary and the secondary. With the same notation as for inductors,

$$k_w\ A_W = N_1\ I_1 + N_2\ I_2 \tag{2.24}$$

From the above equations,

$$V_1\ I_1 + V_2\ I_2 = 4\ k_w\ J\ B_m\ A_C\ A_W \tag{2.25}$$

$$VA = 2\ f\ B_m\ J\ A_C\ A_W \tag{2.26}$$

$$A_C A_W = \frac{VA}{2\ f\ B_m\ J\ k_w} \tag{2.27}$$

The above equation relates the area product ($A_C A_W$) required for a transformer to handle a given VA rating.

2.4.1 Design Steps

For a given specification of VA, V_1, V_2, J, B_m, k_w, and f, it is desired to design a suitable transformer [5] [6]. The design requires

- Size of wire and number of turns to be used for primary and secondary windings.
- Core to be used.
- Resistance of the winding.
- Magnetizing inductance of the transformer.

1. Compute the Area product ($A_C A_W$) of the desired core.

$$A_C A_W = \frac{VA}{2fk_w JB_m} \tag{2.28}$$

2. Select the smallest core from the core tables having an area product higher than obtained in step (1).
3. Find the core area (A_C) and window area (A_W) of the selected core.
4. Compute the number of turns

$$N_1 = \frac{V_1}{4fB_m A_C} \; ; \; N_2 = \frac{V_2}{4fB_m A_C} \tag{2.29}$$

5. Select the nearest higher whole number to that obtained in step (4), for the primary and secondary turns.
6. Compute the wire size for secondary and primary.

$$a_{w1} = \frac{I_1}{J} \; ; \; a_{w2} = \frac{I_2}{J} \tag{2.30}$$

7. Select from the wire tables the desired wire size.
8. Compute the length of secondary and primary turns, from the mean length per turn of the core tables.
9. Find from the wire tables, the primary and secondary resistance.
10. Compute from the core details, the reluctance of the core.

$$R = \frac{l_c}{A_C \mu_o \mu_r} \tag{2.31}$$

11. Compute the magnetizing inductance.

$$L_m = \frac{N^2}{R} \tag{2.32}$$

Table 2.2: Design of Transformers and Inductors

Laminations: GKW — Core Section: Square
Flux Density: 1T for Inductor — 1.2T for Transformer
Current Density: J = 2.5 A/mm^2 — Window Space Factor: 0.3
Transformer Design: $N = 3754V_{rms}/A_C$ — a_w in $mm^2 = I_{rms}/J$
Inductor Design: $N = 10^6 LI_{peak}/A_C$ — $l_g = 4\pi 10^4 NI_{peak}$ mm

Core Type No.	A_C mm^2	A_W mm^2	A_P mm^4	VA@ As a Xformer	Energy# As an Inductor
L202	12.3	27.7	33.7	0.03	0.13
L164	23	53.3	1,227.6	0.12	0.46
L109	41	81.3	3329	0.33	1.25
12AX	90.3	210.9	19,033	1.9	7.1
T17	161.3	122.2	19,716	1.97	7.4
INT41	169	168	28,392	2.8	10.6
17A	204.5	1519	31,070	3.1	11.7
12A	252.8	188	47,533	4.7	17.8
10A	252.8	443.2	1,12,052	11.2	42
T 1	278.9	656.7	1,83,138	18.3	68.7
T 74	306.3	227.9	69,806	7	26.2
T 23	364.8	271.7	99,118	9.9	37.2
T 2	364.8	1,092.5	39,862	39.8	149.5
T 30	400	300	1,20,000	12	45
T 45	492.8	369.6	1,82,168	18.2	68.3
T 31	492.8	369.6	1,82,168	18.2	117
T 15	645.2	483.9	3,12,173	31.2	159
T 14	645.2	656.7	4,23,657	42.3	173
T.33	784	588	4,60,992	46.1	287
T.3	1011.2	756.8	7,65,346	76.5	595
T.16	1451.6	1,092.5	15,85,913	158.4	691
T 5	1451.6	1,269.8	18,43,312	184.1	1,054
T 6	1451.6	1,935.5	28,09,562	280.7	720
INT 120	1,600	1,200	19,20,000	191.8	1,873
T 43	2,580.6	1,935.5	49,94,777	499	4,824
T 8	2,580.6	4,984.9	1,28,64,258	1,285	3,645
INT 180	3,600	2700	97,20,000	971	15,452
8 A	5,806.4	7,096.8	4,12,06,911	4,117	10,854
8 B	5,806.4	4,984.9	2,89,44,581	2,892	21,699
8 C	5,806.4	9,965.7	5,78,65,181	5,781	44,953
T 100	10,322.6	11,612.9	11,98,74,000	1,1975	555
4 AX	566.4	2,612.2	14,79,626	147.8	4,28,500
35 A	1,451.6	7,871.8	1,14,26,755	1,142	
43 TP	645.2	2,903.2	18,73,041	281	
8 TP	1,451.6	7,871.8	1,14,26,755	1,583	
100 TP	2,580.6	15,483.8	3,99,58,217	5,988	
@ Transformer Primary $V_{rms}I_{rms}$; Frequency (for Transformer) f=50 Hz					
# Energy Capacity of the Inductor = $LI_{peak}I_{rms}/2$					

2.4.2 Transformer and Choke Design Table

Table 2 gives a typical transformer and choke design table. A data book on cores and accessories is available at Magnetic Cores and Accessories.

2.5 Capacitors for Power Electronic Application

Power electronic systems employ capacitors as power conditioning elements. Unlike in signal conditioning applications, the capacitors in PES are required to handle large power. As a result they must be capable of carrying large current without overheating. To satisfy the demands in PES, the capacitors must be very close to their ideal characteristics namely low equivalent series resistance (ESR) and low equivalent series inductance (ESL). Low ESR will ensure low losses in the capacitor. Low ESL will ensure that the capacitor can be used in a large range of operating frequency. Figure 8 shows the impedance of a capacitor as a function of frequency. It is seen that a real capacitor is

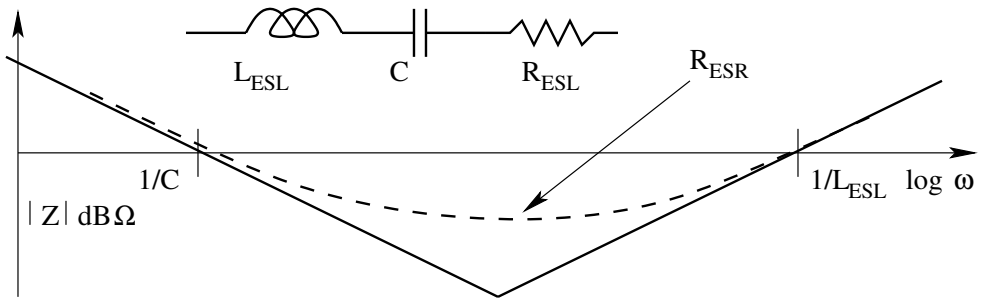

Figure 2.8: Impedance of a Capacitor as a Function of Frequency

close to the ideal at lower frequencies. At higher frequencies, the ESR and the ESL of the real capacitor make it deviate from the ideal characteristics. For PES applications, it is necessary that the ESR and ESL of the capacitor are low.

2.6 Types of Capacitors

There are several different types of capacitors employed for power electronic applications.

2.6.1 Coupling Capacitors

Coupling capacitors are used to transfer ac voltages between two circuits at different average potentials. Such capacitors are employed mostly in control

circuits to couple ac signals from one circuit to another with differing dc potentials. The current carried by such a capacitor is comparatively low. The important feature of such capacitors is

- High insulation resistance

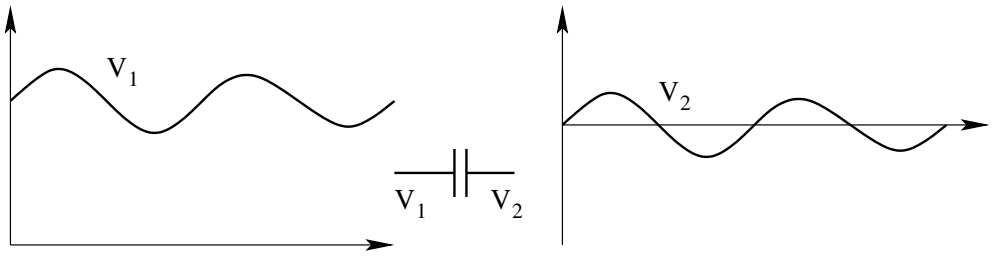

Figure 2.9: Coupling Capacitor

2.6.2 Power capacitors (low frequency)

These are used in PES mainly to improve power factor. They are generally used at low frequencies (predominantly 50/60 Hz). They compensate the reactive power demanded by the load so that the power handling portion of the PES are not called upon to supply the reactive power. Further, they also bypass harmonics generated in the PES. In such applications the voltage is predominantly sinusoidal; the current may be rich in harmonics. The important features of these capacitors are

- Capability to handle high reactive power.
- Capability to handle high harmonic current.

A typical application is shown in Fig. 10

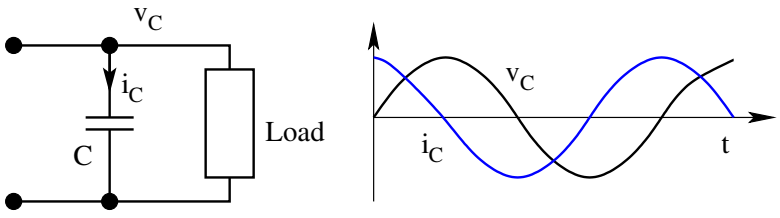

Figure 2.10: Power Frequency Power Capacitors

2.6.3 Power capacitors (high frequency)

These are used for the same applications as the low frequency power capacitors but at higher frequencies (up to 20 kHz). Further they are also capable

of carrying surge current resulting from switching. Such applications arise when capacitor banks are switched on and off to cater to conditions of varying load (typical in induction heating applications). The main features of these capacitors are

- Capability to handle large reactive power.
- Capability to operate at higher frequency.
- Capability to handle switching surge currents.

2.6.4 Filter capacitors

These capacitors are forward filtering capacitors to smooth out the variable source voltage applied to the load or reverse filtering capacitor to smooth out the variable load current from reaching the source. They are called upon to handle large periodic currents. The important features of these capacitors are

- High capacitors value.
- High rms current rating.

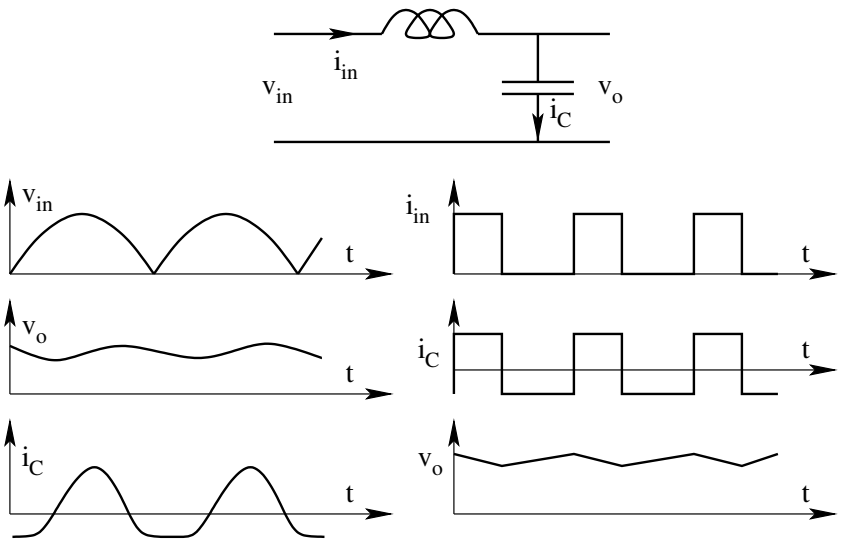

Figure 2.11: Waveforms in a Filtering Application

These capacitors are electrolytic capacitors on account of the unipolar voltage they are subjected to. Typical applications are shown in Fig. 11.

2.6.5 Pulse capacitors

Pulse capacitors are used to provide very high surge currents to loads. They will be charged over a relatively long period and discharged in a very short

period. Typical applications are precision welding, electronic photoflash, electronic ignition etc. The required features for these applications are

- Large energy storage capacity.
- Large peak current handling capacity.
- Low ESL.

A typical application is shown in Fig. 12.

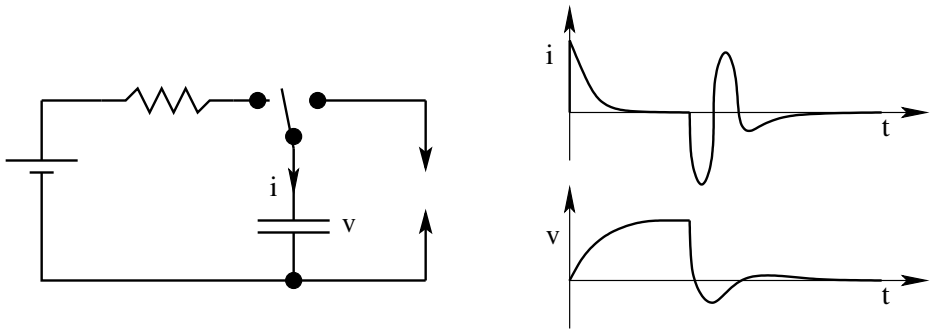

Figure 2.12: Pulse Capacitor Application

2.6.6 Damping capacitors

Damping or snubber capacitors are used in parallel with power switching devices to suppress undesired voltage stresses on the device. The rms current in the capacitor will be high. The desired features are

- High rms current capacity.
- Low ESL.

A typical application is shown in Fig. 13.

2.6.7 Commutation capacitors

These capacitors are employed in the commutation circuits of SCRs for forced turn-off of the device. They are subjected to very high reactive power and peak currents. The commutation process is quite short and so these capacitors must have purely capacitive reactance even at high operating frequency. The desired features are

- High peak current capacity.
- Low ESL.

A typical application is shown in Fig. 14.

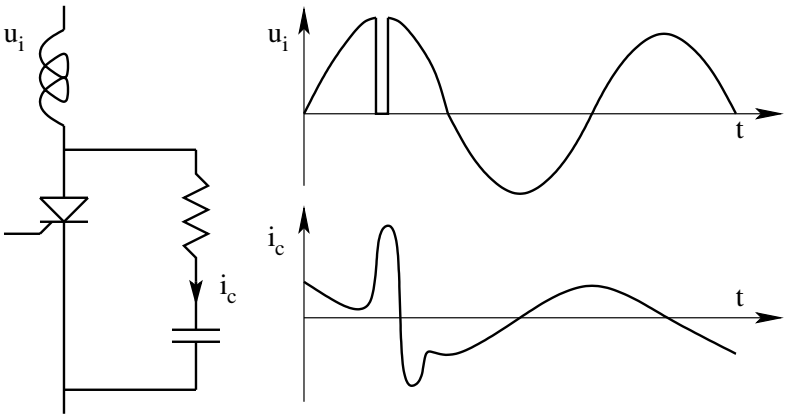

Figure 2.13: Damping Application

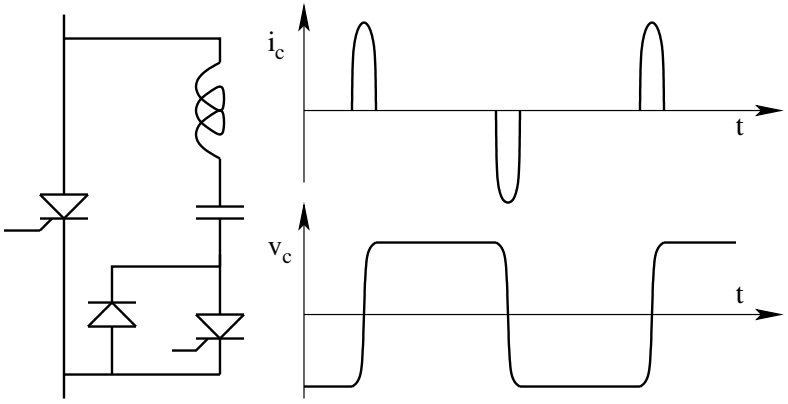

Figure 2.14: Commutation Applications

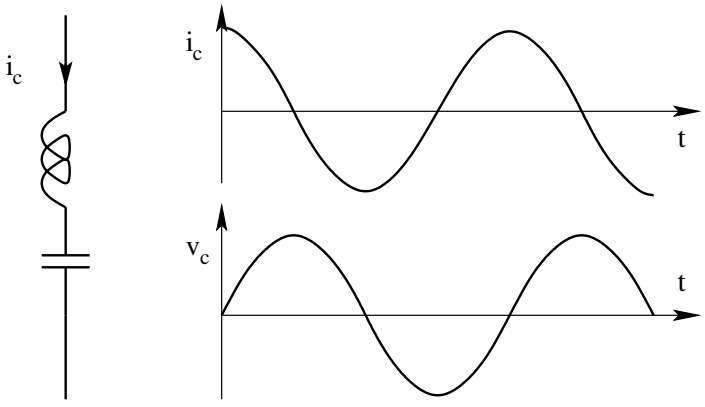

Figure 2.15: Resonant Capacitor Application

2.6.8 Resonant capacitors

Resonant capacitors are used in circuits in combination with inductors and are subjected to sinusoidal voltages and current. The operating frequency is high. The stability of the capacitor is important. The desirable features are

- Stability of capacitance.
- Low ESR.

A typical application is shown in Fig. 15. The following links give data sheets of different types of capacitors.

Electrolytic Single Ended Capacitors

Electrolytic Double Ended Capacitors

AC Capacitors

2.7 Illustrated Examples

1. Figure 1 shows the voltage across a capacitor used for a power electronic application. The capacitance value is $2.5\mu F$. The capacitor has an equivalent resistance (ESR) of 10 mΩ. The dielectric of the capacitor has a thermal resistance of $0.2°C/W$ to the ambient.
   (A) Sketch the current waveform through the capacitor for one cycle.
   (B) Evaluate the losses in the capacitor.
   (C) Evaluate the temperature rise in the dielectric of the capacitor.

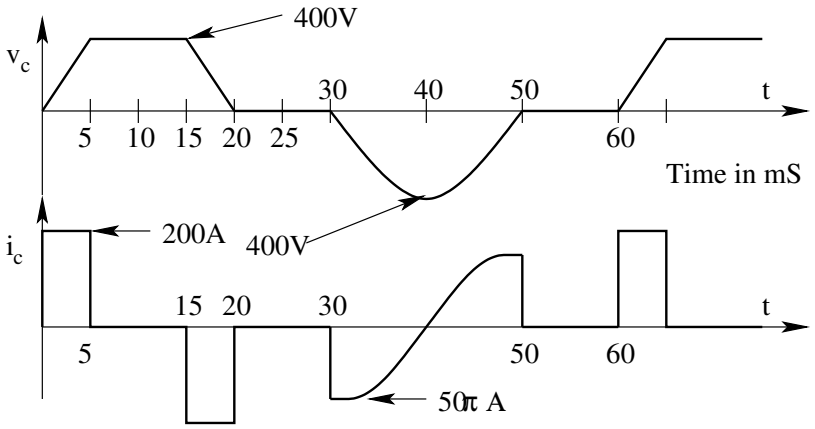

Fig. Ex 2.1: Loss Calculation.

I_{rms}^2	10779	ESR	0.01Ω
I_{rms}	103.8A	R_{th}	$0.2°C/W$
Loss	107.8W	Temperature Rise	$21.6°C$

2. A power electronic capacitor is specified to have the following values.
   Capacitance = $10\mu F$;
   ESR = 30 mΩ;
   ESL = 75 nH;
   Sketch the impedance of the capacitor as a function of frequency in the dBΩ vs log ω. Determine the range of frequency for which the capacitor may be idealized to be a pure capacitance of 10 μF

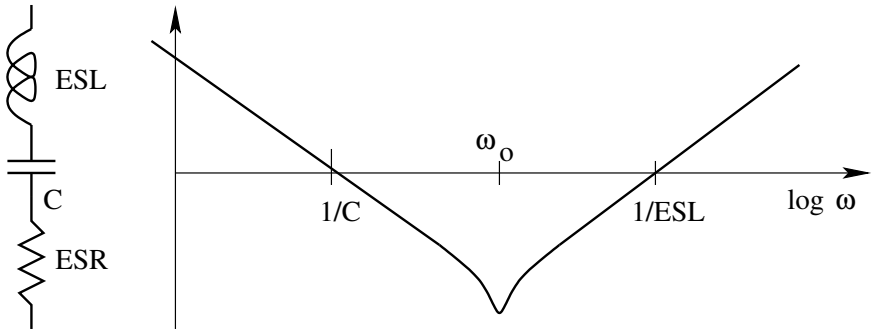

Fig. Ex 2.2: Capacitor's Non-idealities

$$Z = \frac{1 + scR + s^2LC}{sC} \tag{2.33}$$

C is ideal upto a frequency of 18.4 kHz

L	75nH
C	$10\mu F$
R	30 mΩ
Natural Frequency	183.8 kHz

3. The following design refers to a 2 mH inductor suitable for dc application with a maximum current of 0.5 A.
   Core: 26x19; $A_W = 40mm^2$; $A_C = 90mm^2$; N = 37 turns; $a_w = 0.29mm^4$ (23 SWG);
   Evaluate the above design (i.e. peak flux density, peak current density, window space factor, and inductance value) for airgap values of 0.08mm and 1mm.

A_W	$40mm^2$	$40mm^2$
A_C	$90mm^2$	$90mm^2$
N	37T	37T
a_w	$0.29mm^2$	$0.29mm^2$
l_g	0.08mm	1mm
I	0.5A	0.5A
Peak Flux Density	0.29T	0.29T
Window Space Factor	0.27	0.27
Inductance	1.94 mH	0.15 mH

4. Figure 4 shows the magnetic circuit of a coupled inductor. The magnetic material of the core may be assumed to be ideal. Evaluate the inductances L_1, L_2, L_{12}, L_{21}.
$N_1 = 100T; N_2 = 200T; A_{g1} = A_{g2} = 40mm^2; A_g = 80mm^2;$
$l_{g1} = 1mm; l_{g2} = 2mm; l_g = 1.5mm$

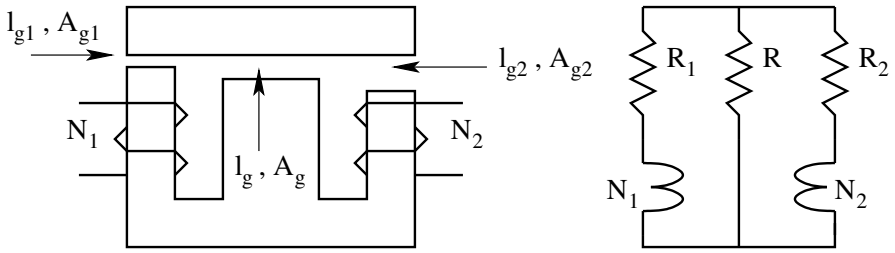

Fig. Ex 2.4: Evaluation of Mutual Inductances

$$L_1 = \frac{N_1^2}{R_1 + \dfrac{RR_2}{R + R_2}} \tag{2.34}$$

$$L_2 = \frac{N_2^2}{R_2 + \dfrac{RR_1}{R + R_1}} \tag{2.35}$$

$$L_{12} = \frac{N_1 N_2 R}{\left(R_2 + \dfrac{RR_1}{R + R_1}\right)(R + R_1)} \tag{2.36}$$

$$L_{21} = \frac{N_1 N_2 R}{\left(R_1 + \dfrac{RR_2}{R + R_2}\right)(R + R_2)} \tag{2.37}$$

l_{g1}	1 mm	l_{g2}	2 mm
l_g	1.5 mm	A_{g1}	$40mm^2$
A_{g2}	$40mm^2$	A_g	$80mm^2$
N_1	100 T	N_2	200 T
R_1	19894368	L_1	325.25 μH
R_2	39788736	L_2	827.9 μH
R	14920776	L_{12}	177.41 μH
$R\|\|R_1$	8526158	L_{21}	177.41 μH
$R\|\|R_2$	10851473		

5. The approximate wave shape of a capacitor current in a commutation circuit is shown in Fig. 5. The capacitor has an ESR of 20 mΩ. Evaluate the power dissipation in the capacitor.

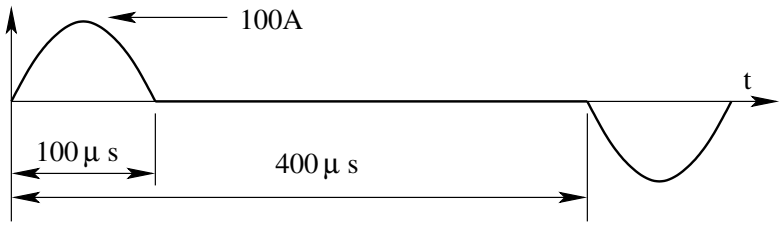

Fig. Ex 2.5: Capacitor's Loss Calculation

$I_{rms} = 35.36A$; ESR = 0.2Ω; P = 250W.

6. Figure 6 shows a lifting magnet used for handling metal billets in a steel mill. The dc current I to the coil (of N turns) is supplied from a current source. The area of cross section of the magnetic path is A_e m^2. The yoke of the magnet and the metal billet may be assumed to be infinitely permeable. The fringing effect of the field in the path of the magnet may be neglected.

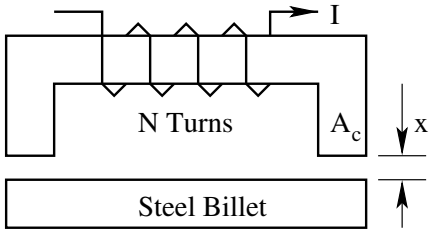

Fig. Ex 2.6: Lifting Magnet

(A) Find an expression for the energy stored in the system as a function of the air gap (x meter).

(B) Find the force exerted by the magnet as a function of the gap length.

$$R = \frac{l_g}{A_e \mu_o \mu_r} = \frac{2x}{A_e \mu_o} \tag{2.38}$$

$$L = \frac{N^2}{R} = \frac{N^2 A_e \mu_o}{2x} \tag{2.39}$$

$$E = \frac{1}{2} L I^2 = \frac{N^2 A_e \mu_o I^2}{4x} \tag{2.40}$$

$$F = -\frac{dE}{dx} = \frac{N^2 A_e \mu_o I^2}{4x^2} \tag{2.41}$$

The above relationship is valid for intermediate values of x. For x close to zero, infinite permeability assumption is not valid. For large values of x, negligible fringing assumption ($x << A_e$) is not valid.

7. Figures 7 (a, b, and c) show three magnetic circuits with an exciting winding on each having 100 turns. The core in (c) is obtained by assembling together one each of cores shown in (a) and (b). The magnetic material for the core may be considered to have very large permeability with saturation flux density of 0.2 T.

   (A) Evaluate the expression for flux linkages (NΦ) for cores (a) and (b) as a function of the exciting current i_a and i_b.

   (B) Plot the characteristics NΦ vs i for the cores (a) and (b).

   (C) From the above plot NΦ vs i for the composite core (c).

   (D) Comment on the inductance of the circuit (c).

N_a	100	N_b	100	
l_{ga}	0.001	l_{gb}	0.005	
B_{max}		L_a	0.00314	$N\Phi = L_a i_a$
		L_b	0.000628	$N\Phi = L_b i_b$
Sauturation Current for Core A			1.59A	
Sauturation Current for Core B			7.96A	

8. Figure shows the magnetic circuit of a coupled inductor. Make suitable assumptions and evaluate the inductances L_a, L_b, and L_c.

$$L_a = \left(\frac{N_a \Phi_a}{i_a}\right)_{i_b=0} = \frac{N_a^2 (R_b + R_c)}{R_a R_b + R_b R_c + R_c R_a} \tag{2.42}$$

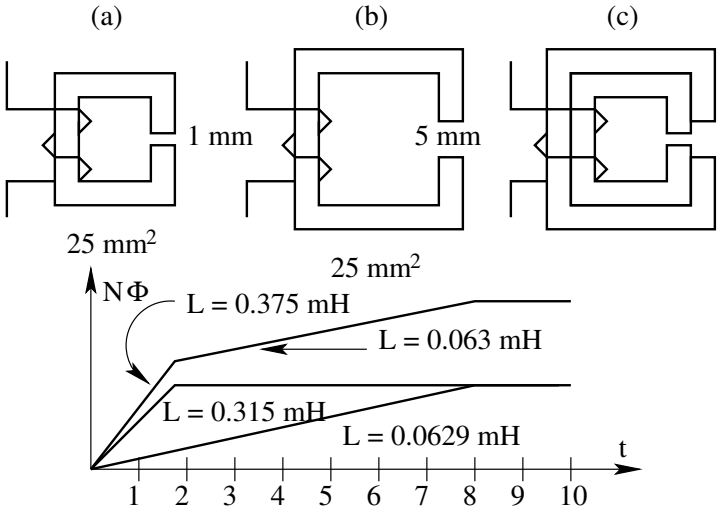

Fig. Ex 2.7: Composite Inductor

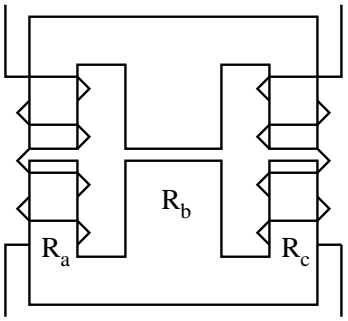

Fig. Ex 2.8: Mutual Inductance

$$L_b = \left(\frac{N_a\Phi_a}{i_b}\right)_{i_a=0} = \frac{N_b^2(R_a + R_c)}{R_aR_b + R_bR_c + R_cR_a} \tag{2.43}$$

$$L_{ab} = \left(\frac{N_b\Phi_b}{i_a}\right)_{i_b=0} = \frac{N_aN_bR_c}{R_aR_b + R_bR_c + R_cR_a} \tag{2.44}$$

$$L_{ba} = \left(\frac{N_a\Phi_a}{i_b}\right)_{i_a=0} = \frac{N_aN_bR_c}{R_aR_b + R_bR_c + R_cR_a} \tag{2.45}$$

9. Figure 9 shows a coupled magnetic circuit. The two windings are excited by identical square waves. The core has a cross-sectional area of S unit. The reluctance of the central limb is Rc unit. The reluctance of the outer limbs are dominated by the gap reluctances.

   (A) Draw the equivalent reluctance circuit model of the magnetic circuit.

   (B) Find the self-inductances L_{11} and L_{22}.

(C) Find the mutual-inductances L_{12} and L_{21}.

(D) Verify that $L_{12} = L_{21}$.

(E) Write the dynamic equations relating v_t, $i_1(t)$, and $i_2(t)$.

(F) Solve for di_1/dt.

(G) Find the condition (among x, y, N_1/N_2) under which $di_1/dt = 0$, may be a solution to the above set of equations. Interpret the result.

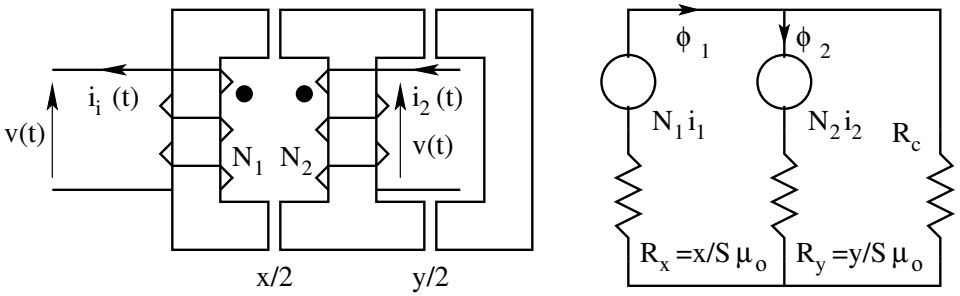

Fig. Ex 2.9: Ripple free Current

$$L_{11} = \frac{N_1^2(R_c + R_y)}{R_xR_y + R_xR_c + R_cR_y} \tag{2.46}$$

$$L_{22} = \frac{N_2^2(R_x + R_y)}{R_xR_y + R_xR_c + R_cR_y} \tag{2.47}$$

$$L_{12} = \frac{N_1N_2R_y}{R_xR_y + R_xR_c + R_cR_y} \tag{2.48}$$

$$L_{21} = \frac{N_1N_2R_y}{R_xR_y + R_xR_c + R_cR_y} \tag{2.49}$$

$$v = L_{11}\frac{di_1}{dt} + L_{12}\frac{di_2}{dt} = L_{21}\frac{di_1}{dt} + L_{22}\frac{di_2}{dt} \tag{2.50}$$

$$\frac{di_1}{dt} = \frac{L_{22} - L_{12}}{L_{11}L_{22} - L_{21}L_{12}} \tag{2.51}$$

For $di_1/dt = 0$, $L_{22} = L_{12}$; $y = \dfrac{x}{N_1/N_2 - 1}$.

Under the above condition for coil 1, the induced voltage equals source voltage and so rate of change of input current is zero or ripple free.

Chapter 3

Control, Drive and Protection of Power Switching Devices

3.1 Introduction

In this section we see the issues related to the control, drive and protection of power switching devices. The ideal requirements are set down and some of the practical circuits useful in achieving these requirements are given.

3.2 Base Drive Circuits for BJT

In power electronic applications, the BJTs used will be capable of blocking high voltages (up to about 600V) when OFF, and passing high currents (up to 50 to 100A) when ON. Such high power transistors are quire sensitive to voltage and current stresses. The high voltage devices are very sensitive to reverse biased second breakdown. The high current devices usually have low current gain. On account of these factors, the design of suitable drive circuits for BJTs is a demanding task.

3.2.1 Requirements of Base Drive

A good base drive circuit must satisfy the following general requirements

1. A fast rising ($< 1\mu S$) current to turn on the device fast.
2. A hard drive of adequate magnitude (I_{B+}) to reduce turn on loss.
3. A steady base current of adequate magnitude (I_B) to keep the device in saturation during the on period of the switch.
4. A fast falling ($< 1\mu S$) current of adequate magnitude (I_{B-}) during the storage time (typically 5 to 10 μS) of the turn-off period of the switch.

5. A base voltage of adequate negative magnitude (typically 5V) during the off period of the device. This base voltage that is applied during the off period must be through a low impedance to ensure good dV/dt immunity during the off period.
6. The drive circuit must be such that the switching performance is insensitive to the operating point of the switch.
7. Electrical isolation between the control input and the switch may be desired. This will be necessary very often when the system has several switches located at different electrical potentials.
8. The drive circuit must have overriding protection to switch off the device under fault.

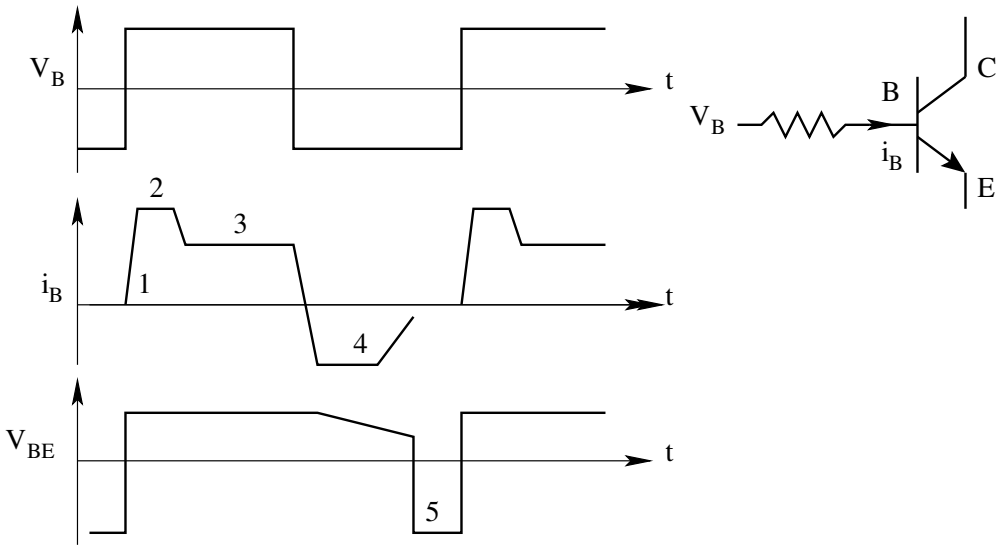

Figure 3.1: Typical Requirements of a BJT Drive Circuit

The preferred base drive is illustrated in Fig. 1. The desired features of a good drive circuit are

- Fast rising current for fast turn on.
- Hard turn on drive to reduce turn on loss.
- Adequate drive for low conduction test.
- Negative base drive to reduce storage time.
- Negative base bias for good dv/dt immunity. Base drive current is zero under this condition.

There are several drive circuits, which satisfy these requirements. Some of these circuits are described here.

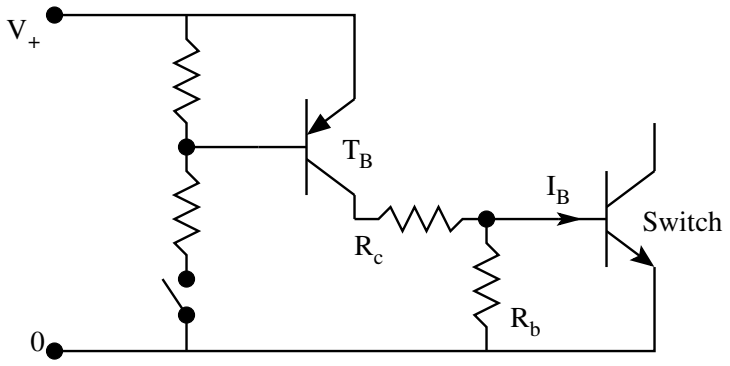

Figure 3.2: Drive Circuit 1

3.2.2 Drive Circuit 1

The circuit shown in Fig. 2 is a bare minimum drive circuit. The turn on time of the base drive is the same as the rise time of the control transistor TB. The turn on base drive is approximately V_+/R_c. This is a very rudimentary circuit. The drive requirement 1 and 3 are satisfied by this circuit and is not a practical circuit.

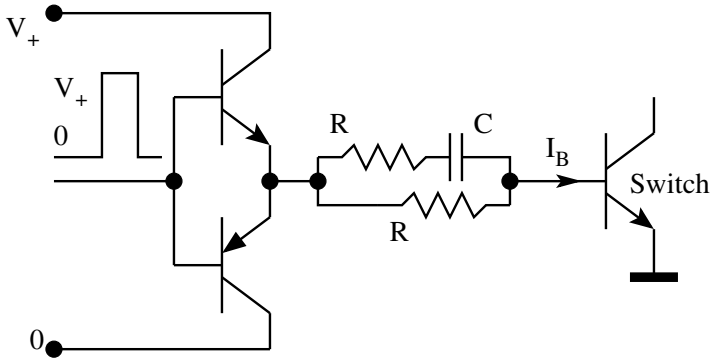

Figure 3.3: Drive Circuit 2

3.2.3 Drive Circuit 2

A slightly better circuit is shown in Fig. 3. This drive circuit satisfies the requirements 1, 2, 3, and 4. This does not provide negative bias during the off period. There is no electrical isolation or other protections. This circuit may be used in single switch chopper circuits.

$$I_{B+} = \frac{2V_+}{R} \tag{3.1}$$

$$I_B = \frac{V_+}{R} \tag{3.2}$$

$$I_{B-} = \frac{2V_+}{R} \tag{3.3}$$

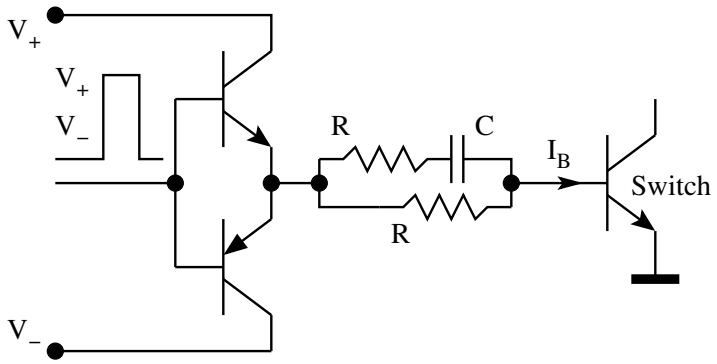

Figure 3.4: Drive Circuit 3

3.2.4 Drive Circuit 3

The circuit in Fig. 3 may be modified with a bipolar control power supply as shown in Fig. 4, so that the drive requirement 5 also may be satisfied.

$$I_{B+} = \frac{2V_+}{R} \tag{3.4}$$

$$I_B = \frac{V_+}{R} \tag{3.5}$$

$$I_{B-} = \frac{V_+}{R} \tag{3.6}$$

3.2.5 Drive Circuit 4

One feature of circuits 1, 2 and 3 is that the drive current is nearly constant during the on time. This would result in the switch being overdriven when the switch current is low. For applications where the load current is varying over a wide range, this may result in the storage delay time being a function of the load. This delay time variation could cause difficulties especially at high switching frequencies (the delay time may become appreciable compared to the on and off time of the switch). In such applications the excess base drive current may be diverted by a simple add-on circuit known as the Baker clamp. This is shown in Fig. 5. If the load current is low and the device enters deep

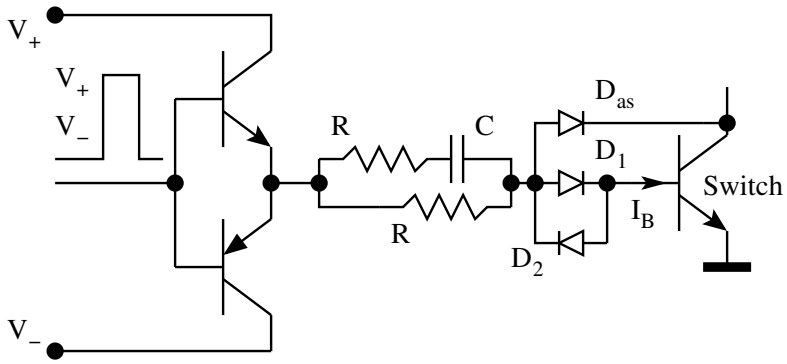

Figure 3.5: Drive Circuit 4

saturation, the V_{ce} drop of the switch becomes low and forward biases D_{as}. Thus the excess drive is diverted from the base into the collector. Such a drive will keep the switch on the border of saturation, thereby making the storage delay time independent of the switch current. However this positive feature is obtained at the cost of higher conduction loss (Note that the V_{ce} drop now cannot go below about 0.7V). The base drive shown in Fig. 5 satisfies the drive requirements 1 to 6.

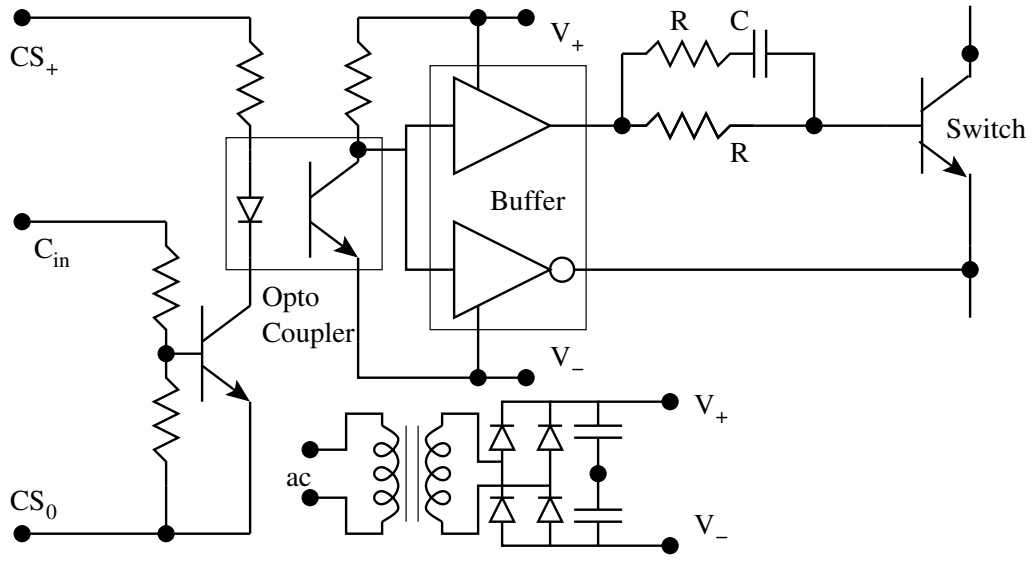

Figure 3.6: Drive Circuit 5

3.2.6 Drive Circuit 5

In most applications of PES where more than one switch is used, it will be necessary to provide isolation between the control input and the switch. In the circuit shown in Fig. 6, the isolation is provided by an opto coupler. Notice that there is a separate power supply V_+ and V_- isolated from the control circuit power supply CS_+ and $CS0$. Such isolated drive circuits employing opto-couplers may be used upto a frequency of about 5 KHz.

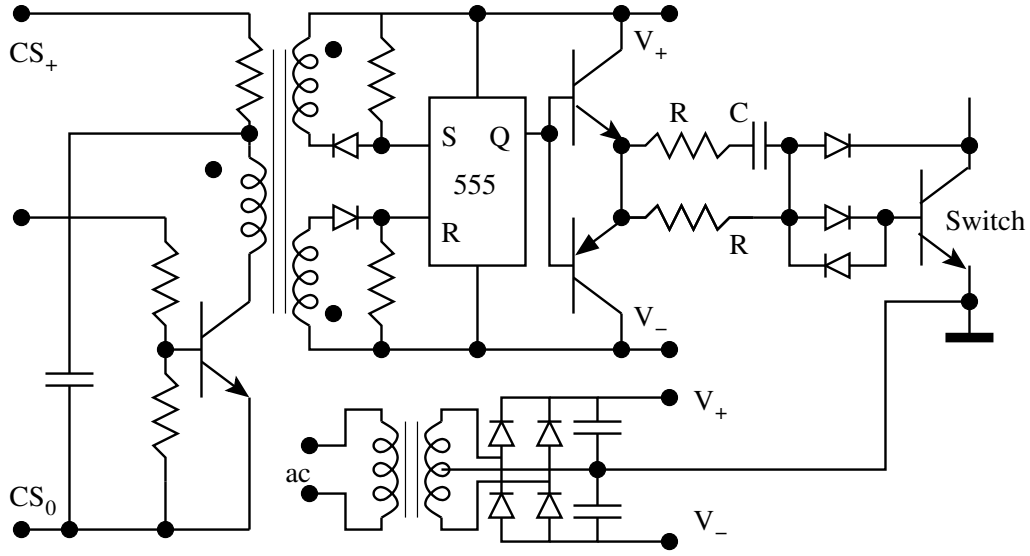

Figure 3.7: Drive Circuit 6

3.2.7 Drive Circuit 6

More modern switching applications need drive circuits capable of operating in a higher frequency range. In such applications optocoupler circuits will be too slow. Electromagnetic isolation is used then. A circuit with electromagnetic isolation capable of operating upto about 20 KHz is shown in Fig. 7. The operating frequency range may be extended further if the SR flip flop is faster. Notice again the need for a separate isolated power supply.

3.2.8 Drive Circuit 7

The requirement of separate power supply is a definite disadvantage in isolated drive circuits. An elegant solution to this problem at high switching frequencies is the proportional drive circuit. The required power to drive the switch is drawn from the load circuit itself through a current transformer (CT). A typical proportional base drive circuit is shown in Fig. 8. It is useful in the

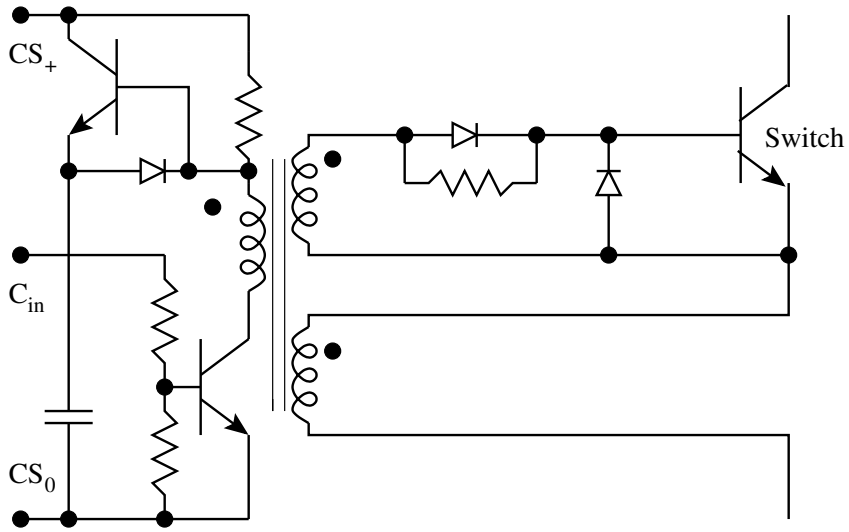

Figure 3.8: Drive Circuit 7

range of 20 to 50 KHz. Notice the absence of the Baker clamp. The antisaturation circuit is not required, since the base drive is proportional to the switch current. This circuit is especially useful for switches, which turn on at zero current (many resonant converters). The control circuit is required to provide energy to only initiate the turn on and turn off process

3.2.9 Drive Circuit 8

Unlike the high power devices such as diodes and SCRs, a BJT cannot be protected from over currents with a series fuse. The control circuit must be capable of cutting off the base drive when over current through the device is sensed. This may be done directly with a Hall effect current sensor in series with the transistor or indirectly by sensing the collector-emitter voltage drop of the device during conduction. When the device is overloaded the current gain of the transistor will drop and as a result the device will come out of saturation. This will result in an increase in the collector-emitter voltage. A drive circuit, which senses the over current indirectly and cuts off the drive current to the transistor, is shown in Fig. 9.

3.3 Snubber Circuits for Power Switching Devices

Real power switching devices take a finite time to switch on or off. During the switch-on time the device voltage is defined. During switch-off the device current is defined. The second quantity during switching (device current during turn-on and device voltage during turn-off) is decided by the external circuit to the switch. In many applications, the load will be inductive (motor drives,

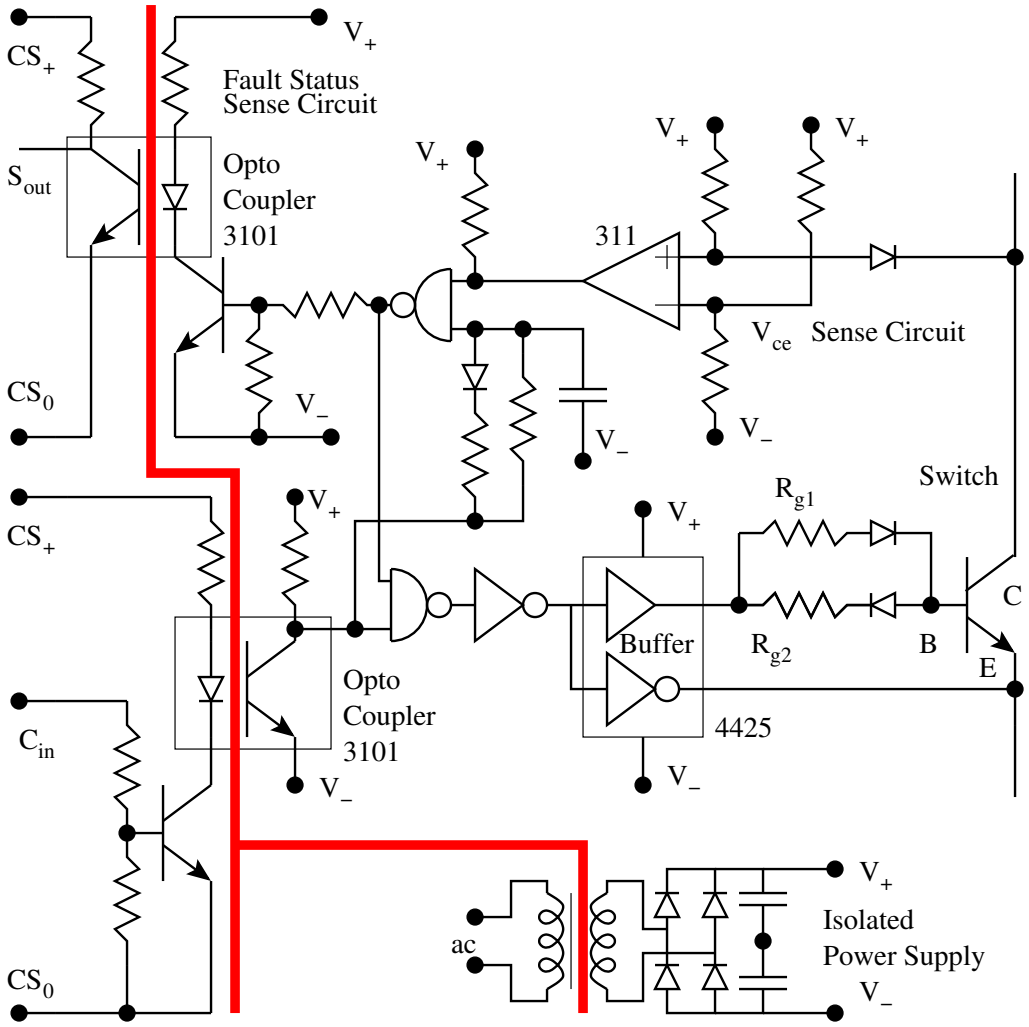

Figure 3.9: Drive Circuit 8

inductive filters). The power circuit will have parasitic inductance associated with the conducting paths. Further there will be several other non-idealities of the switches present. On account of all these factors, the switching process in the device will be far from ideal. Figure 10 shows a simple chopper circuit consisting of all ideal components except the power switching device (in this case a BJT). The load being inductive, may be considered to be a constant current branch for the purpose of analysis. The switch voltage, current, switching energy loss and the v-i trajectory of the switch current and voltage on the vi plane in course of switching are shown in Fig. 11. The peak power dissipation in the device is seen to be quite large ($V_G I_L$). The switching loss will be proportional to the switching frequency and is equal to

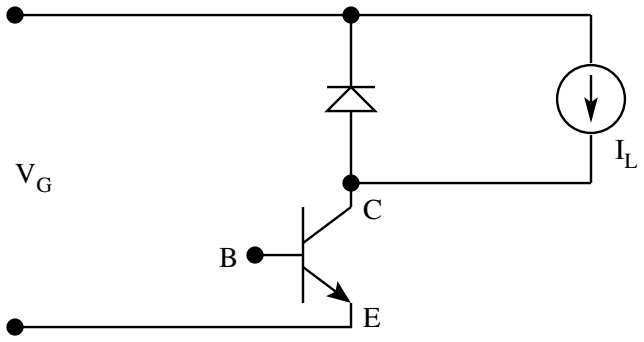

Figure 3.10: Ideal Chopper

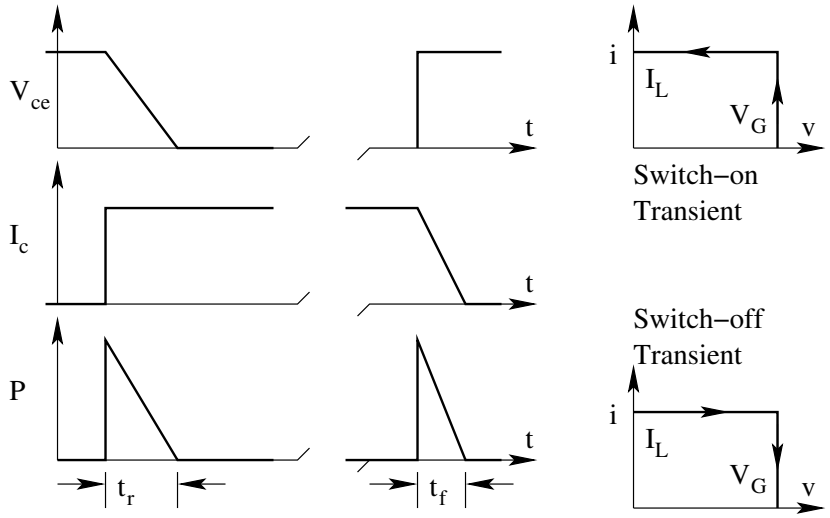

Figure 3.11: Switching Trajectories in the Chopper

$$P_{SW} = f\frac{V_G I_L t_r + V_G I_L t_f}{2} \tag{3.7}$$

The practical circuits will have several nonidealities as listed above. The switching loci with some of these nonidealities are shown in Fig. 12. The current overshoot (1) is on account of the reverse recovery current of the diode. The voltage overshoot (2) is on account of the stray inductances and capacitances in the circuit. The important point to notice is that the peak voltage and current stresses on the switching device are far more than the circuit voltage and the load current. The switching loci traverse far from the axes of the v-i plane, thus indicating large transient losses. When these loci cross the safe operating area of the v-i plane, device failure is certain. The purpose of the snubber circuits for power switching devices is to reduce the switching losses by constraining the switching trajectories to move close to the

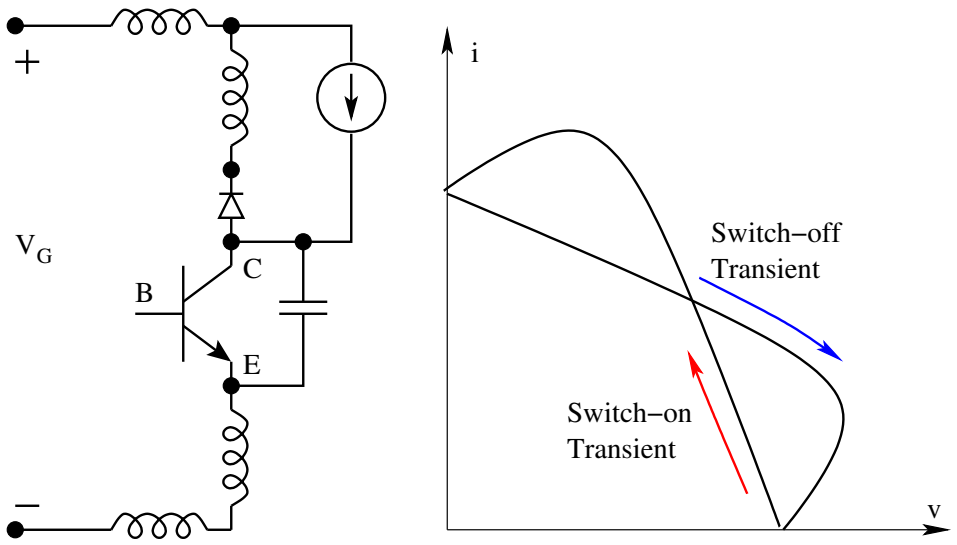

Figure 3.12: Switching Trajectories with Non-idealities in the Chopper

vi axes during the switching transient. From the non-ideal switching loci, it may be seen that over currents occur during turn-on and over voltage during turn-off. The snubber ensures that during turn-on rate of rise of current is limited (with a series inductor), and during turn-off the rate of rise of voltage is limited (with a shunt capacitor). The other elements in the snubber are to reduce the effects of turn-on snubber on the turn-off process and turn-off snubber on the turn-on process. The snubber circuit caters to three functions.

- Turn-off aid
- Turn-on aid
- Over-voltage suppression

3.3.1 Turn-off Snubber

The circuit show in Fig. 13 is a simple realization of a turn off snubber. It may be seen qualitatively that on turn-off the device current is diverted into the capacitor through D_f so that the device voltage on turn-off is constrained to rise slowly. At the end of turn-off the capacitor is charged to the circuit voltage. During the next turn-on the capacitor discharges its energy into the resistor R_f and is ready for the next turn-off. The snubber reduces the device turn-off loss by forcing the device voltage to rise slowly. But the energy trapped in the capacitor at the end of the turn-off process has to be lost in R_f during the next turn-on. From Fig. 13, we may evaluate the following

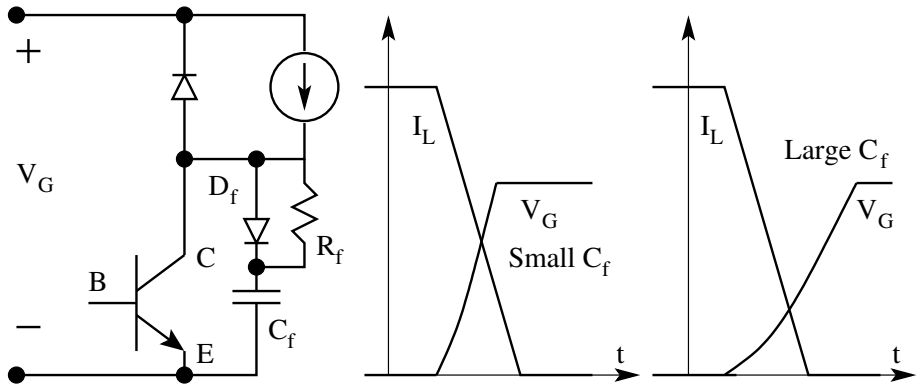

Figure 3.13: Turn-off Snubber

Turn off loss without snubber:

$$E_{off} = \frac{V_G I_L t_f}{2} \tag{3.8}$$

Turn off loss with snubber:

$$E_{off} = \int_0^{t_f} v_{ce} i_c dt \tag{3.9}$$

Trapped energy in the capacitor:

$$E_C = \frac{C_f V_G^2}{2} \tag{3.10}$$

There are two possible ways of designing the snubber capacitor as seen from

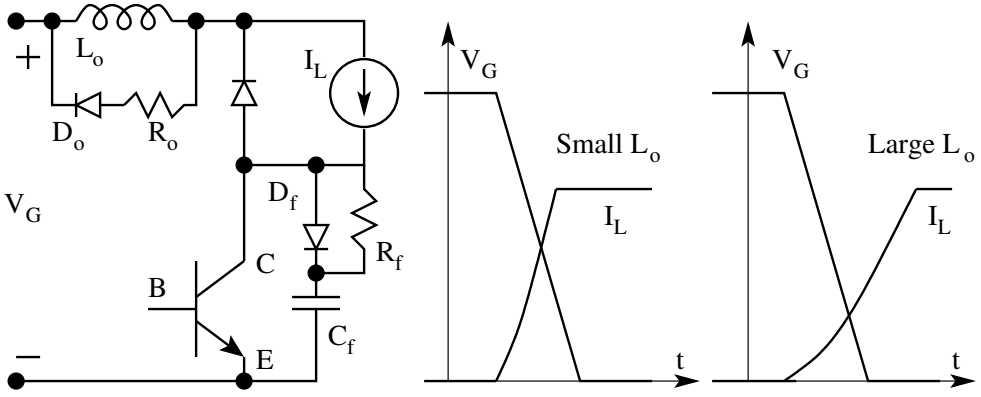

Figure 3.14: Turn-on Snubber

Fig. 13 (small C_f and large C_f). With the simple switching model of a transistor (fall time t_f), it may be seen that the capacitor voltage during

transient is

$$V_C = \frac{I_L t^2}{2C_f t_f} = V_G \frac{C_b}{C_f} \frac{t}{t_f}^2 \tag{3.11}$$

$$C_b = \frac{I_L t_f}{2V_G} \tag{3.12}$$

Notice that $C_f = C_b$ will make the turn off transient in v_c equal to t_f. Then at the border of the two design possibilities,

$$V_c = V_G \frac{t}{t_f}^2 \tag{3.13}$$

$$E_{off} = \frac{V_G I_L t_f}{12} \tag{3.14}$$

$$E_{R_f} = \frac{C_f V_G^2}{2} = \frac{V_G I_L t_f}{4} \tag{3.15}$$

$$E_{off}(total) = \frac{V_G I_L t_f}{3} \tag{3.16}$$

The device switching off loss has reduced by a factor of 1/6 and the total turn-off loss by a factor of 2/3. With C_f in the range of $0.5C_b$ to C_b, the overall loss is low. The snubber capacitor C_f may be designed based on this criteria. After selecting C_f, R_f is chosen such that the $R_f C_f$ time constant is much less than the minimum on time in the given application. This will ensure that the snubber capacitor is reset during the on time and is ready for the next turn-off.

3.3.2 Turn-on Snubber

The circuit shown in Fig. 14 is a simple realization of a turn-on snubber. It may be seen qualitatively that on turn-on, the excess voltage is dropped across the inductor (L_o) so that the device current on turn-on is constrained to rise slowly. At the end of turn-on the inductor carries the load current and stores the associated energy. During the next turn-off the inductor discharges its energy into the parallel resistor R_o and is ready for the next turn-on. The snubber reduces the device turn-on loss by forcing the device current to rise slowly. But the energy trapped in the inductor at the end of the turn on process has to be lost in R_o during the next turn-off. From Fig. 14, we may evaluate the following.
Turn off loss without snubber:

$$E_{off} = \frac{V_G I_L t_r}{2} \tag{3.17}$$

Turn off loss with snubber:

$$E_{off} = \int_0^{t_f} v_{ce} i_c dt \tag{3.18}$$

Trapped energy in the inductor:

$$E_L = \frac{L_o I_L^2}{2} \tag{3.19}$$

There are two possible ways of designing the snubber inductor as seen from Fig. 14 (small L_o and large L_o). With the simple switching model of a transistor given in the earlier chapter (rise time t_r), it may be seen that the inductor current during transient is

$$I_C = \frac{I_L t^2}{2 L_o t_r} = V_G \frac{L_b}{L_o} \frac{t}{t_r}^2 \tag{3.20}$$

$$L_b = \frac{V_G t_r}{2 I_L} \tag{3.21}$$

Notice that $L_o = L_b$ will make the turn off transient in I_c equal to t_r. Then at the border of the two design possibilities,

$$I_c = I_L \frac{t}{t_r}^2 \tag{3.22}$$

$$E_{on} = \frac{V_G I_L t_r}{12} \tag{3.23}$$

$$E_{R_o} = \frac{L_o I_L^2}{2} = \frac{V_G I_L t_r}{4} \tag{3.24}$$

$$E_{off}(total) = \frac{V_G I_L t_r}{3} \tag{3.25}$$

The device turn-on loss has reduced by a factor of 1/6 and the total turn-

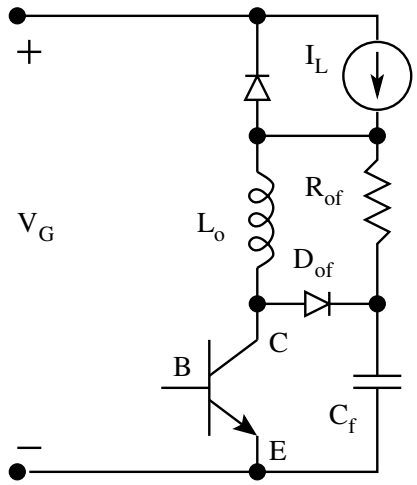

Figure 3.15: Turn-on and Turn-off Snubber

on loss by a factor of 2/3. With L_o in the range of $0.5L_b$ to L_b, the overall loss is low. The snubber inductor L_o may be designed based on this criteria. After selecting L_o, R_o is chosen such that the L_o/R_o time constant is much less than the minimum off time in the given application. This will ensure that the snubber inductor is reset during the off time and is ready for the next turn-on. Figure 15 shows a snubber circuit, which provides both turn-on and turn-off aid. Note that R_{of} serves as R_f and R_o. D_{of} serves as D_o and D_f. For many low power applications these snubbers are satisfactory. For higher power applications, it may be difficult to eliminate stray inductance in the power circuit. In such cases it will be necessary to provide over voltage protection. Over voltages are on account of current interruptions through the stray inductance in the circuit. Two snubber circuits which protect the device from switching over voltage with switch-on and switch-off snubbers are shown in Figs. 16 and 17.

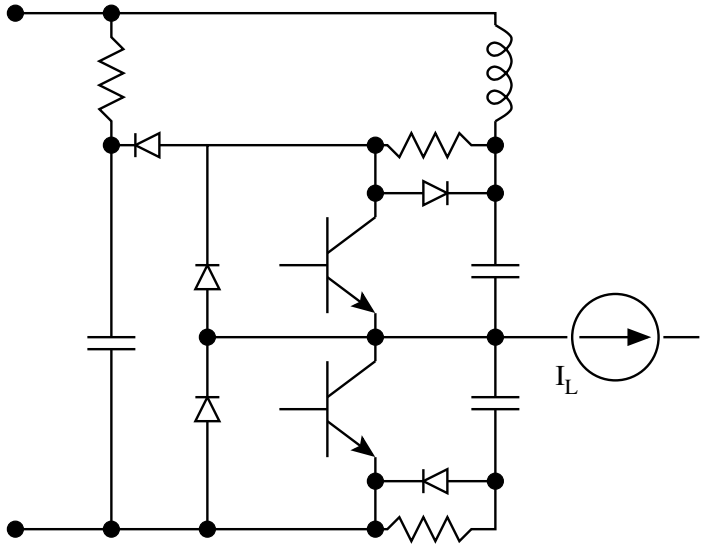

Figure 3.16: Snubber for a Pair of Complementary Switches

3.4 Gate Drive Circuits for MOSFET

MOSFETs can switch much faster than BJTs. They are becoming popular now for low power applications. The drive power requirement for a MOSFET is much less than that of a BJT.

3.4.1 Requirements of Gate Drive

The desirable features of a good drive circuit for a MOSFET are as follows

- A fast rising ($< 0.1\mu S$) current to turn on the device fast.

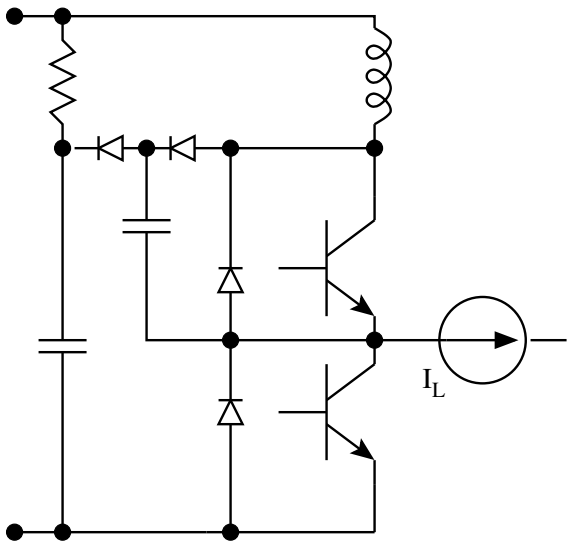

Figure 3.17: Snubber for a Pair of Complementary Switches

- A hard drive of adequate magnitude to quickly ($< 0.5\mu S$) charge the gate source voltage above the threshold voltage $V_{gs}(th)$. This will ensure low turn-on loss.
- A steady gate voltage of greater than $V_{GS(th)}$ to keep the device on with a low on-state resistance $r_{ds(on)}$. Since the gate is isolated from the source, the current required to maintain the gate source voltage constant is zero.
- A fast falling ($< 0.1\mu S$) current drive to initiate turn-off. The magnitude of the negative current must be adequate so that the gate source capacitance is quickly ($< 0.5\mu S$) discharged to zero or a negative voltage.
- A gate voltage of adequate negative magnitude during the off period of the device. This gate voltage that is applied during the off period must be through a low impedance to ensure good noise margin.
- The drive circuit must be such that the switching performance is insensitive to the operating point of the switch.
- Electrical isolation between the control input and the switch may be desired. This will be necessary very often when the system has several switches at different electrical potentials.
- The drive circuit must have overriding protection to switch off the device under fault.

The preferred gate drive is illustrated in Fig. 18. The features are

1. Fast rising gate current for fast turn on.

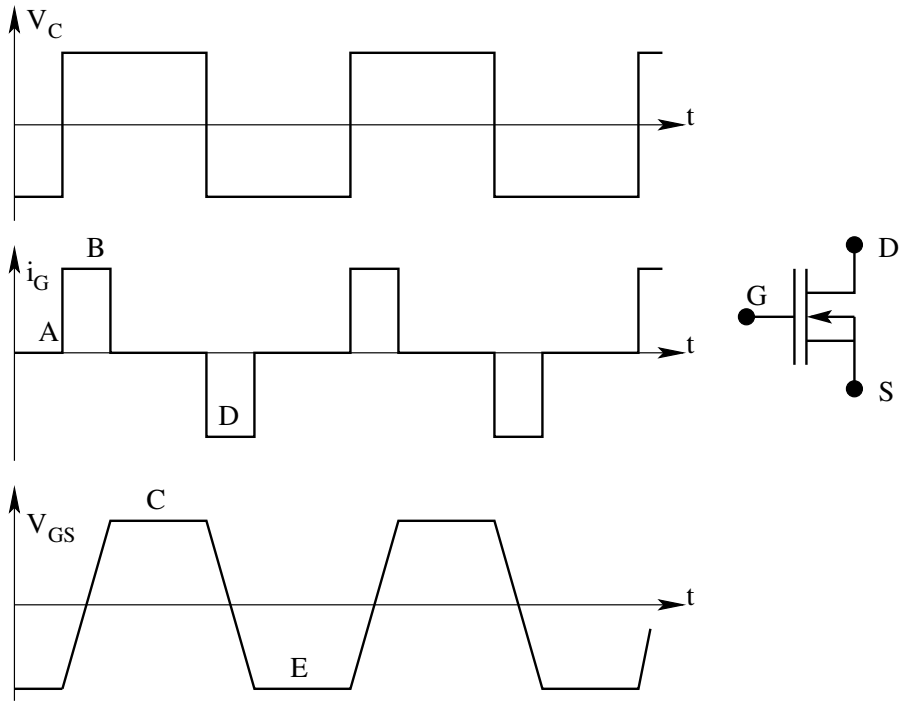

Figure 3.18: Drive Waveforms of a MOSFET

2. Hard turn on drive to reduce turn on loss.
3. Adequate gate voltage for low conduction loss.
4. Negative gate drive for fast turn off.
5. Negative base bias for good noise immunity.

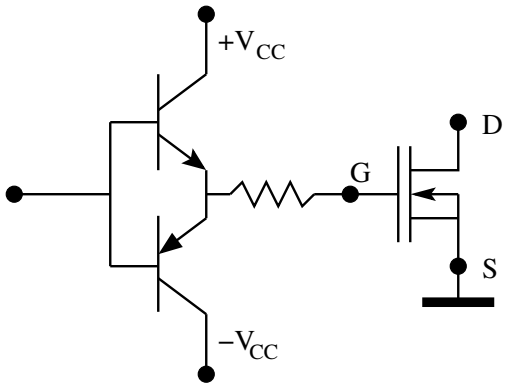

Figure 3.19: MOSFET Drive Circuit

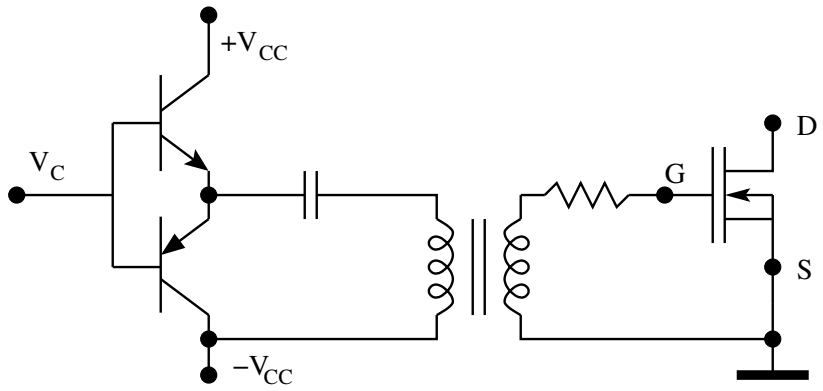

Figure 3.20: MOSFET Drive Circuit

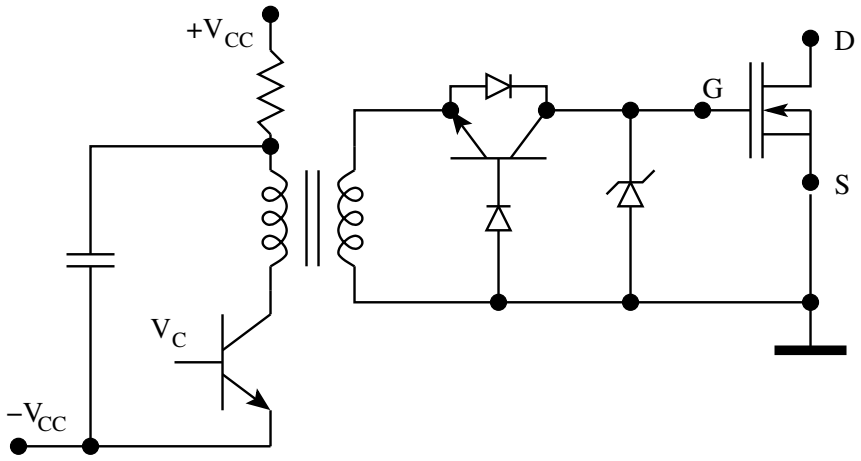

Figure 3.21: MOSFET Drive Circuit

There are several drive circuits, which satisfy these requirements. Some of these circuits are shown in Figs. 19 to 21. Several commercially available drive circuits are given in the following links.

Opto-isolated MOSFET/IGBT driver

Hybrid driver

Single MOSFET/IGBT driver

Semikron dual IGBT driver

Hybrid IGBT driver

Hybrid BJT driver

Non-isolated dual driver

3.5 Illustrated Examples

1. The circuit shown below is a chopper operating at 10 kHz. Evaluate the switching losses in the snubber of the circuit.

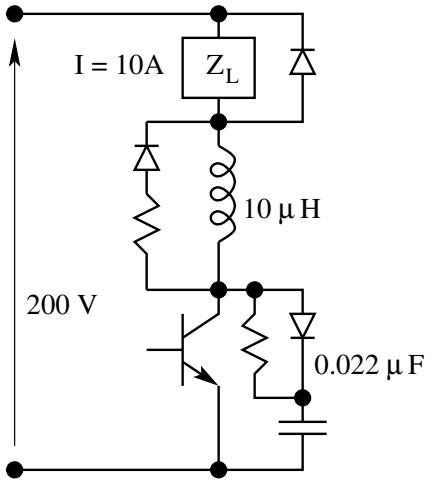

Fig. Ex 3.1: Snubber Losses

$$P_{off-snubber} = 0.5C\ V^2\ f = 0.5\ 0.022\ 10^{-6}\ 200^2\ 10000 = 4.4\ W \quad (3.26)$$

$$P_{on-snubber} = 0.5L\ I^2\ f = 0.5\ 10\ 10^{-6}\ 10^2\ 10000 = 5\ W \quad (3.27)$$

$$P_{snubber} = 4.4\ W + 5.0\ W = 9.4\ W \quad (3.28)$$

2. The circuit shown below is a chopper operating at 10 kHz. Evaluate the switching losses in the snubber of the circuit.

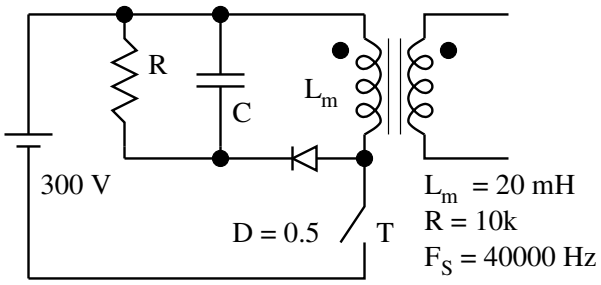

Fig. Ex 3.2: Snubber Losses

$$I_m = \frac{V}{L_m} DT_S = \frac{300}{20\ 10^{-3}} 0.5\ 25\ 10^{-6} = 0.1875A \tag{3.29}$$

$$E_m = 0.5\ L_m\ I_m^2 = 0.5\ 20\ 10^{-3}\ (0.1875)^2 = 351.6\mu J \tag{3.30}$$

$$P_{loss} = E_m F_S = 14.1W \tag{3.31}$$

$$V_C = \sqrt{P_{loss}\ R} = 375\ V \tag{3.32}$$

3. The drive circuit shown is used to control the transistor switch S. The device S requires appropriate continuous positive base current during ON time and transient negative base current of atleast 1.5 A for atleast $2\mu S$ during OFF time. Evaluate the values of R1, R2, and C.

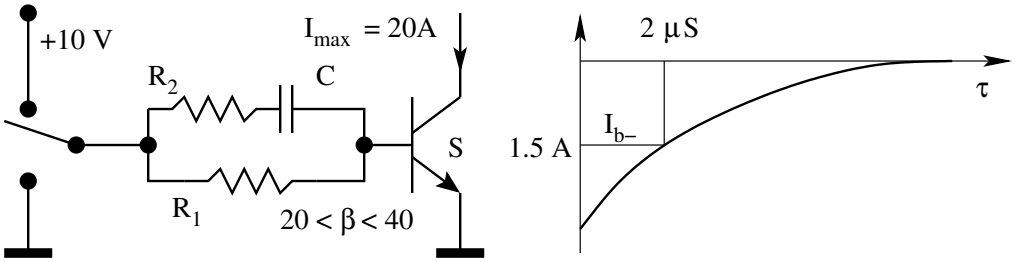

Fig. Ex 3.3: Snubber Losses

$$I_{b+} \ = \ 1\ A = \frac{V_C}{R_1} \ \Rightarrow \ R_1 \ = \ 10\ \Omega \tag{3.33}$$

$$I_{b-} \ = \ 1.5\ A = V_C\ e^{-(2.5\mu S/R_2 C)} \tag{3.34}$$

Select $R_2 = 2.5\ \Omega$

$$\frac{10}{2.5}\ e^{-2.0\mu S/(2.5\ C)} = \ 1.5\ A \Rightarrow \ C \ = \ 0.815\ \mu F \tag{3.35}$$

4. A drive IC is capable of sinking and sourcing 1 A is used to drive a MOSFET switch (C_{GS} = 1000 pF; C_{DS} = 200 pF; V_{th} = 4 V) as shown in Fig. 4. Find the value of R_g such that V_{GS} on turn-on reaches 10 V within 500 nS.
With the above value of R_g, evaluate the off time dV_{DS}/dt noise margin provided by the circuit. At 500 nS, the gate voltage reaches 10 V.

$$10 \ = \ V_{GS} \ = \ 15 \left(1 - e^{-500\ 10^{-9}/\tau}\right) \tag{3.36}$$

$$\tau \ = \ \frac{500nS}{ln(15/5)} \ = \ 455\ nS \tag{3.37}$$

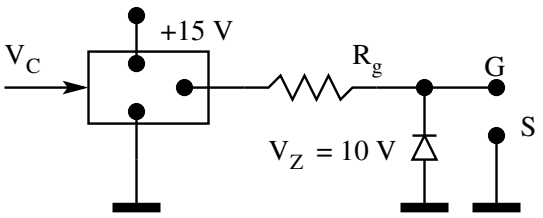

Fig. Ex 3.4: Snubber Losses

$$R_g \;=\; \frac{\tau}{C_{GS}} \;\Rightarrow\; R_g \;=\; 455\ \Omega \tag{3.38}$$

Off-time noise immunity:

$$V_{th} \;=\; R_g\, C_{DS}\, \frac{dV_{DS}}{dt} \;\Rightarrow\; \frac{dV_{DS}}{dt} \;=\; 109.1\ V/\mu S \tag{3.39}$$

5. The following circuit is a simple non-isolated drive used with a BJT. The base emitter drop of the power transistor and the drive transistors (V_{be}) are 0.8 V, and 0.7 V respectively. The different parameters relating to the circuit are: $I_C = 15\ mA$; $R_1 = 3\ \Omega$; $R_2 = 3\ \Omega$; $C = 0.2\ \mu F$; $\beta \geq 10$; $t_s = 3\ \mu S$; $T_{on} = 20\mu S$; $T_S = 50\ \mu S$. The control input is as shown.

   (A) Sketch the base current waveform.

   (B) Evaluate the source/sink current of the control input.

   (C) Evaluate the peak current rating of the drive sources.

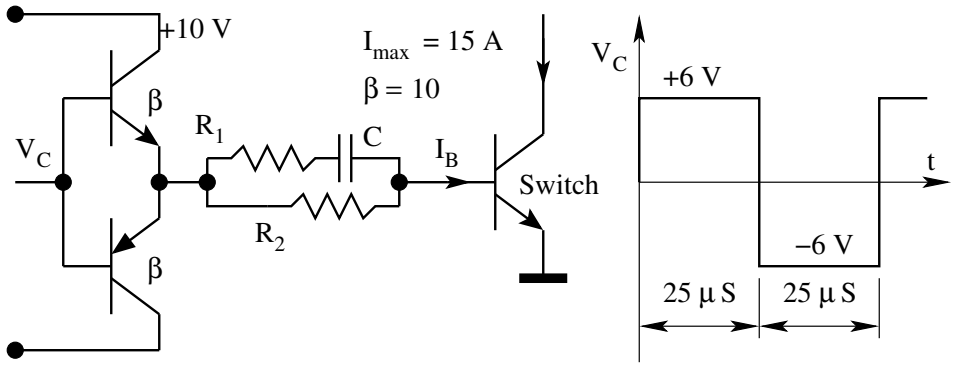

Fig. Ex 3.5: Drive Circuit

Source current from V_C = 300 mA.
Sink current from V_C = 560 mA.
Source current from +10 V = 300 mA.
Sink current to ground = 560 mA.

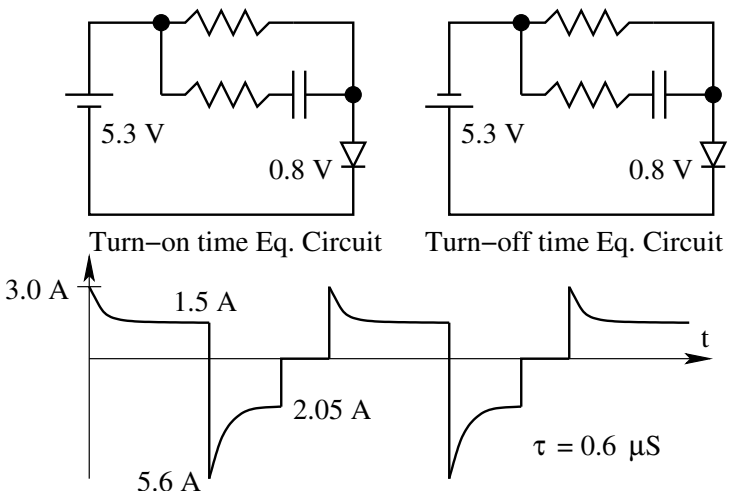

Fig. Ex 3.5: Equivalent Circuits and Drive Currents

6. The current through and the voltage across a switching device is given in Fig. 6. Evaluate the approximate switch-off and switch-on energy loss in the device.

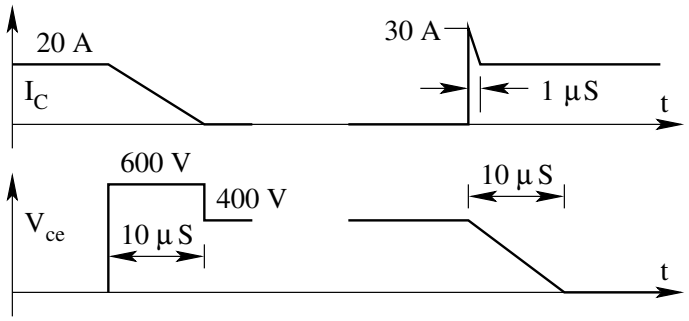

Fig. Ex 3.6: Switching Loss

$$E_{off} \;=\; 0.5\; V_{off}\; I_{on}\; t_r \;=\; 0.5\; 600\; 20\; 10\; \mu s \;=\; 60\; mJ \qquad (3.40)$$

$$E_{on} \;=\; 0.5\; V_{off}\; I_{on}\; t_f \;=\; 0.5\; 400\; 30\; 10\; \mu s \;=\; 60\; mJ \qquad (3.41)$$

Problem Set

1. The following problem is based on the analysis of snubber circuits for transistor switches. The circuits in Fig. 1.1(a) and 1.1(b) show a typical switch in a chopper application with and without a snubber network. The load L, C and R form the inductive load on the chopper. The elements

L_f, D_f and R_f form the turn-on snubber. The elements L_o, D_o and R_o form the turn-off snubber. The following assumptions in the analysis of switching transients are valid.

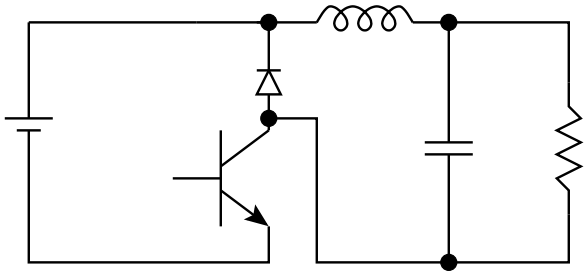

Fig. P 3.1: (a) A Chopper without Snubber

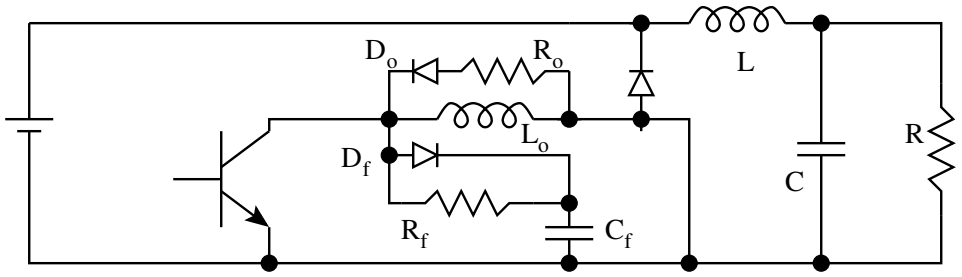

Fig. P 3.1: (b) A Chopper with Turn-on and Turn-off Snubber

- The load current is continuous and constant during the switching transient.
- During the rise time of the turn-on switching transient, the collector-emitter voltage V_{ce} falls linearly to zero.
- During the fall time of the turn-off switching transient, the collector current I_C falls linearly to zero.

It is necessary to analyse the turn-on and turn-off transient during the switching process. The drive waveforms during the switch-off process are shown in Fig. 1.1(d). The circuit equivalents in the different intervals (Pre-transient, turn-off storage delay time t_s, fall time t_f, turn-on completion time T_1, T_2 and T_3, and post-transient time). These intervals are marked sequentially as intervals 1,2,3,4,5,6 and 7. Interval 1 is the pre-transient time. Interval 2 is the turn-off storage delay time. The effective turn-on transient starts in interval 3. In this interval, it may be taken that the voltage across the switch is given by

$$I(t) \;=\; I\left(1 - \frac{t}{t_f}\right) \tag{3.42}$$

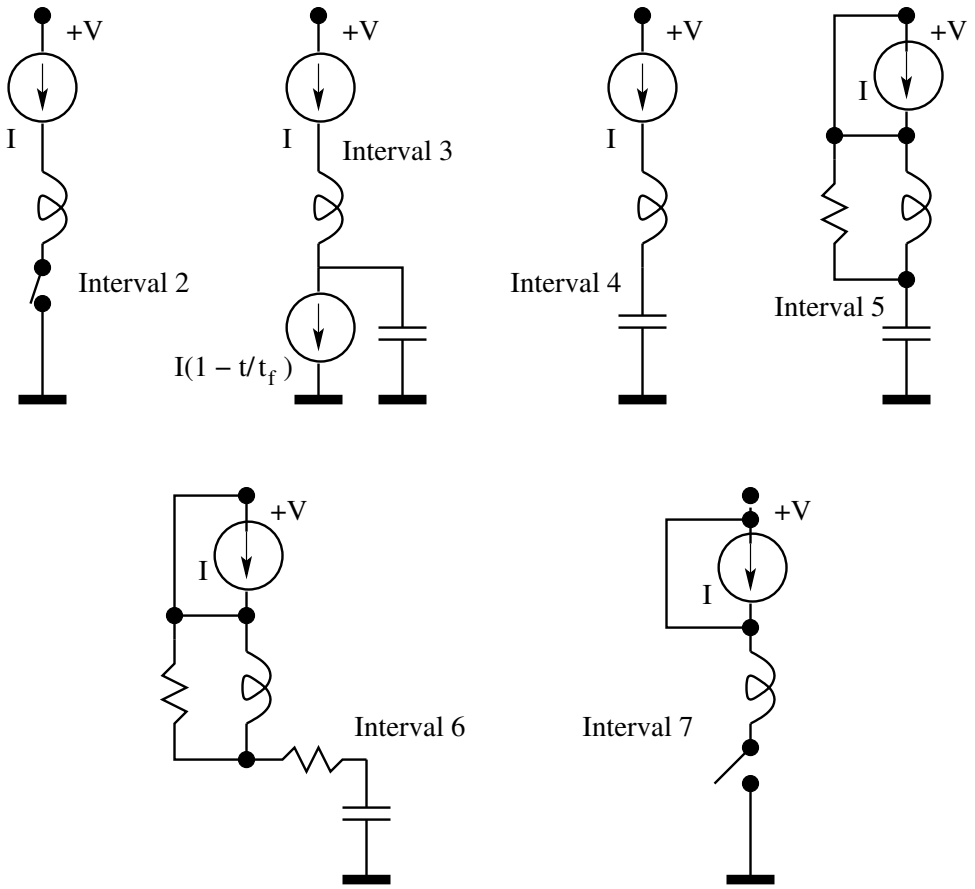

Fig. P 3.1: (c) The Equivalent Circuits in Different Intervals

The initial condition on the capacitor voltage is that $V_c = 0$. The initial condition on the inductor (Lo) current is that $I_{Lo}(o) = 0$.

(A) During the interval 3, find the expressions for the following quantities as a function of time.

- $V_{ce}(t)$
- $I_{ce}(t)$

(B) During the interval 3, evaluate the energy dissipation in the transistor.

At the end of interval 3, the transistor is completely off. However, the transient process not complete. The transient process will be over when the capacitor gets charged to V_{cc} and the inductor current reaches 0. The equivalent circuit for the interval 4 is shown in Fig. 1.1(c). In interval 4, the capacitor gets charged at constant current, till it reaches V_{cc}.

(C) Find the condition on C_f such that the voltage across C_f has not

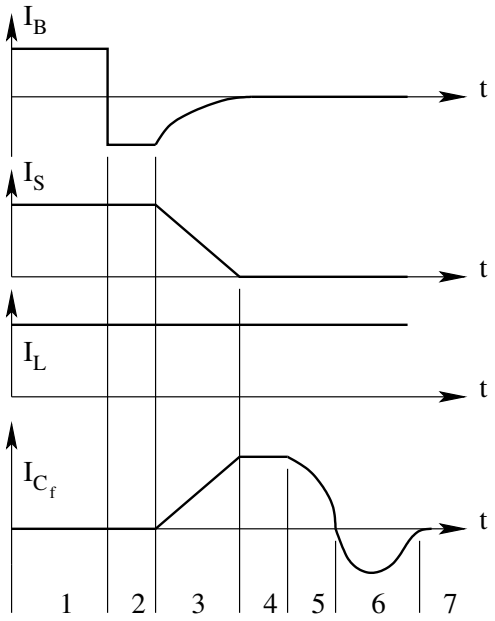

Fig. P 3.1: (d) Circuit Transient Waveforms

reached V_{cc} by the end of interval 3.

(D) Evaluate the time taken (T_1 interval 4) for the voltage across to reach V_{cc}.

The circuit equivalent in interval 5 (after reaches) is given in Fig. 1.1(c).

(E) In this interval evaluate the expression for the capacitor voltage $V_c(t)$. Assume over damped response of the resultant second order system.

(F) Evaluate the over voltage on the capacitor at the end of interval T_2.

During the interval 6, the capacitor loses its excess charge.

(G) Estimate the duration of interval 6 (T_3).

(H) Plot the waveforms of capacitor voltage during the entire turn-off process.

2. The following waveform shows the current through the device when it is being switched off. The circuit voltage is 600 V. The load current is constant at 60 A. The freewheeling diode ensures that the load current has an alternate path when the switch is off. The RC circuit provides smooth recovery of the device voltage during switch-off. The value of C is 0.5 μF. Assume the diodes to be ideal.

(A) Sketch the capacitor current during and following turn-off.

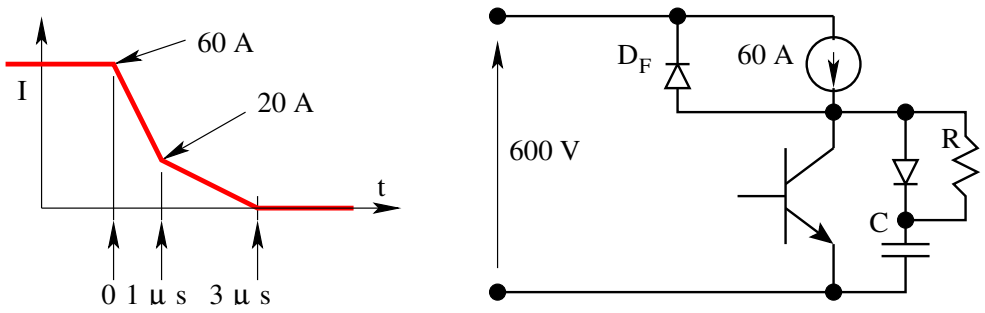

Fig. P 3.2: Turn-off Current Waveform

(B) Evaluate the voltage across the device during switch-off (0 to 3 μs).

(C) Sketch the device voltage following switch-off (0 to 3 μs).

(D) Evaluate the switching loss in the device during turn-off (0 to 3 μs).

(E) Following switch-off, evaluate the time taken for the capacitor C to get fully charged to 600 V so that the freewheeling diode D_F will conduct.

Chapter 4

DC-TO-DC Converter

4.1 Introduction

DC-to-DC converters convert electrical power provided from a source at a certain voltage to electrical power at a different dc voltage. Electrical energy, though available extensively from storage sources such as batteries, or from primary converters such as solar cells, distributed ac mains, is hardly ever used as such at the utilization end. The electrical energy is converted at the utilization end to forms of energy as required (thermal, chemical, light, mechanical and so on). Electrical power converter interfaces between the available source of electrical power and the utilization equipment (heaters, storage battery chargers, lamps, motors and so on) with its characteristics demands of electrical power. The need for this interface arises on account of the fact that in most situations the source of available power and the conditions under which the load demands power are incompatible with each other. An example of such a situation is where a 24V lead acid battery is available as the source of power and the load to be catered consists of digital circuits demanding power at +5V.

DC-to-DC power converters form a subset of electrical power converters. Both the output and input power specifications of dc-to-dc converters are in dc. Most dc loads require a well-stabilized dc voltage capable of supplying a range of required current, or a variable dc current or pulsating dc current rich in harmonics. The dc-to-dc converter has to provide a stable dc voltage with low output impedance over a wide frequency range. These features of the dc-to-dc converter are known through the output regulation and the output impedance of the converter. Most dc sources are either batteries or derived by rectifying the ac mains. The source voltage may vary as much as 40% in the case of batteries. It may contain substantial superimposed voltage ripple in the case of rectified supplies. Most dc sources also exhibit a finite source impedance (against the ideal of zero source impedance). The dc-to-dc converter must maintain integrity of the output power in the presence of these non-ideal source characteristics. This capability of the dc-to-dc converters is known

through the line regulation, ripple susceptibility, and the input impedance of the converter. This chapter on dc-to-dc converter deals with the switched mode dc to dc converter, their basic topologies, and principle of operation, operating modes, and their steady state performance characteristics [22, 32].

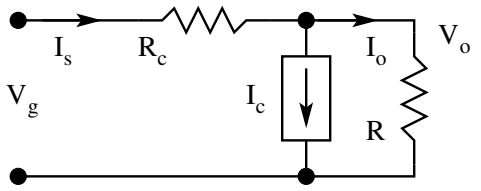

Figure 4.1: Generalised DC to DC Converter

4.2 Simple DC to DC Converter

The simplest and the traditional dc-to-dc converter is shown in Fig. 1.1. Power is available from a voltage source of V_g. The load connected to the output of the converter is resistive (R) demanding power at a voltage level of V_o (V_o ¡ V_g). In this converter the excess voltage between the source (V_g) and the load (V_o) is dropped in the resistor (R) inside the converter. The converter also has an internal current sink (I_c) connected at the output of the converter. The output voltage of the converter may be readily found as a function of R_c, I_c, V_g and R.

$$V_o = \frac{(V_g - I_c R_c)R}{R + R_c} \tag{4.1}$$

V_o may be controlled to the desired level by controlling either R_c (with $I_c = 0$), or by controlling I_c (with a fixed value of R_c). The former is called a series-controlled regulator, and the latter is called a shunt-controlled regulator. The two types of regulators are shown in Fig. 1.2. Notice that in both regulators the series element is present. The distinguishing feature is the presence of control capability either in series element or in the shunt element.

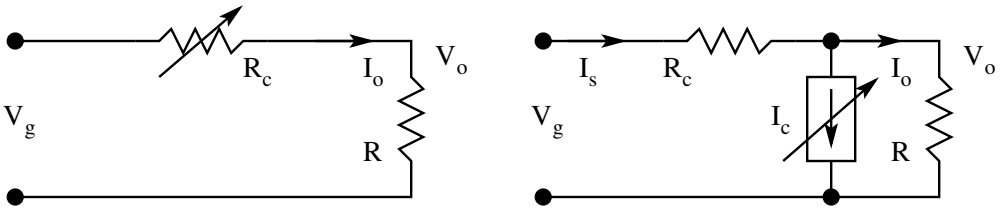

Figure 4.2: Series and Shunt Controlled DC to DC Converter

4.2.1 Series Controlled Regulator

The defining equation of the series controlled regulator is

$$V_o = \frac{V_g R}{R + R_c} \tag{4.2}$$

In order to obtain the required output voltage V_o, against input (V_g) variations, or load (R) variations, the controlled resistor R_c must be varied as per the following relationship.

$$R_c = R\left(\frac{V_g}{V_o} - 1\right) \tag{4.3}$$

The output voltage, power loss, and the efficiency of power conversion may be readily found.

$$V_o = \frac{V_g R}{R + R_c} \tag{4.4}$$

$$P_l = \frac{V_g^2 R_c}{(R + R_c)^2} \tag{4.5}$$

$$\eta = \frac{V_o}{V_g} \tag{4.6}$$

From the above the following features of the series controlled converter may be observed.

1. The converter may be used as a step-down ($V_o \leq V_g$) converter only.
2. The power loss in the converter is dependent on the value of R_c. It is zero for both the extreme values of $R_c = 0$ (input is directly connected to the output), and $R_c = \infty$ (input is totally isolated from the output). This feature in fact is the seed idea of switched mode dc-to-dc converters.
3. The power conversion efficiency is dependent on the ratio V_o/V_g (called the gain of the converter). The lower the required gain of the converter, the lower is its efficiency.

4.2.2 Shunt Controlled Converter

The defining equation of the output voltage of the shunt-controlled regulator is

$$V_o = \frac{V_g R}{R + R_c} - \frac{I_c R R_c}{R + R_c} \tag{4.7}$$

In order to obtain the required output voltage (V_g), against input voltage (V_g) variation, or load (R) variation, the controlled current I_c must be varied according to the following relationship.

$$I_c = \frac{V_g}{R_c} - \frac{V_o(R + R_c)}{R R_c} \tag{4.8}$$

The output voltage, power loss, and the efficiency of power conversion may be found as follows.

$$V_o = \frac{V_g R}{R + R_c} - \frac{I_c R R_c}{R + R_c} \tag{4.9}$$

$$P_l = V_o I_c + (I_c + I_o)^2 R_c \tag{4.10}$$

$$\eta = \frac{V_o}{V_g} \frac{I_o}{I_o + I_c} \tag{4.11}$$

The following features of the converter may be observed from the above set of relationships.

1. The converter may be used as a step-down converter ($V_o \leq V_g$) only, on account of the series pass element R_c. For a given R_c there will be a further limit on V_o, depending on the current to be supplied.

2. The power loss in the converter never reaches zero for any positive value of the control quantity. Remember that in a series controlled regulator, the power loss in the converter was zero at either end of the control quantity ($R_c = 0$, and $R_c = \infty$).

3. The efficiency of power conversion is worse than the series controlled converter. The efficiency is degraded on two counts; the efficiency on account of the series element (V_o/V_g) and the efficiency on account of the shunt branch [$I_o/(I_o + I_g)$].

4.2.3 Practical Regulators

In practice, the series controlled regulator is realized with a series pass transistor used as a controlled resistor. The shunt-controlled regulator is realized with a shunt constant voltage diode (zener) used as a controlled current sink. The circuits are shown in Fig.1.3

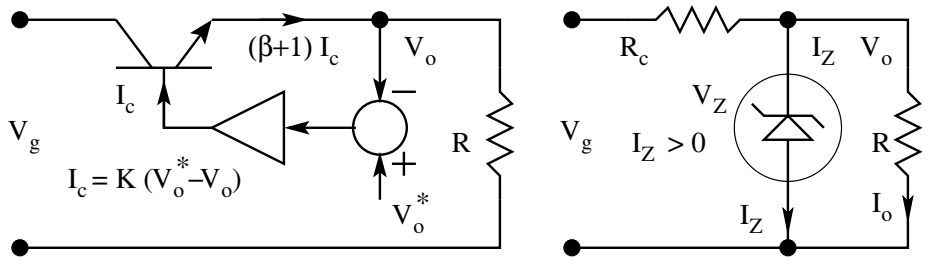

Figure 4.3: Practical Series and Shunt Regulators

Series Controlled Regulator

$$V_o = \frac{(\beta+1)KRV_o^*}{1+(\beta+1)KR} \simeq V_o^* \tag{4.12}$$

K = Transconductance of the feedback amplifier;
β = Common Emitter gain of the pass transistor;

Shunt Controlled Regulator

$$V_o = V_Z \tag{4.13}$$

$$\frac{V_o}{R} \leq \frac{V_g - V_o}{R_c} \tag{4.14}$$

The series controlled and the shunt-controlled regulators are commonly known as linear regulators. They are simple to analyze and design. The major drawback of linear regulators is their poor efficiency. The losses in such converters appear as heat in the series and shunt elements. The design of such converters must also take into account effective handling of the losses, so that the temperature rise of the components is within the safe limits. The linear regulators are therefore used only for low power levels, a few watts in the case of shunt regulators and a few tens of watts in the case of series regulators. For catering to loads in excess of these limits and/or for applications where efficiency is very important (space applications), linear regulators are not suitable. In such applications, switched mode power converters are standard. In the next section we see the basic principles of switched mode dc-to-dc converters.

4.3 Switched Mode Power Converters

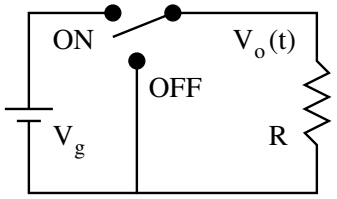

Figure 4.4: Series Controlled Switching Regulator

It was mentioned that the seed idea of switched mode power conversion came from the fact that the power dissipation in a series controlled regulator is zero at either end values of the control quantity Rc, namely $Rc = 0$ and $Rc = \infty$. The core of switched mode dc-to-dc converter is obtained by replacing the series pass element (Rc) of the series controlled regulator by a switch. The circuit is shown in Fig. 4. The switch may occupy either of the position ON and OFF. The ON position connects the source (Vg) to the output (V_o). This

is identical to the condition that $Rc = 0$ in the series controlled regulator. In the OFF position the output is totally isolated from the input. This is identical to the condition that $R_c = \infty$ in the series controlled regulator. In order to obtain a finite effective value of R_c, the switch is operated at high frequency alternating between these (ON and OFF) two states. The switch is operated at a switching period of T_s. For a fraction (dT_s) of the switching period, the switch is kept ON. For the rest of the switching period $[(1-d)T_s]$, the switch is kept OFF. The fraction 'd' is defined as the duty ratio of the switch. The output voltage under such an operation is shown in Fig. 5. The average output voltage under such a control is

$$V_o = \frac{1}{T_s} \int_0^{T_s} V_o(t)\, dt \;=\; d\, V_g \tag{4.15}$$

The duty ratio may be varied in the range of 0 to 1.The average value of the

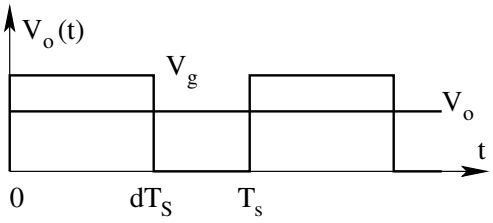

Figure 4.5: Output Voltage of the Switching Converter

output voltage is therefore variable between 0 and V_g. There are no losses in the converter. The power dissipation in the switch is zero during both the ON and OFF states. Therefore the converter has ideally no losses. However the output voltage is not pure dc. The output apart from the desired average voltage (dV_g), also has superimposed alternating voltage at switching frequency. Real dc-to-dc converters are required to provide nearly constant dc output voltage. A real dc-to-dc converter therefore consists of a low pass filter also apart from the switches. The function of the low pass filter is to pass the dc power to the load and to block the ac components at the switching frequency from reaching the output of the converter. In order to achieve efficient operation, the low pass filter is realized by means of non-dissipative passive elements such as inductors and capacitors.

4.3.1 Primitive dc-to-dc Converter

A primitive dc-to-dc converter is shown in Fig. 6. Many operating features of Switched Mode Power Converters (SMPC), and their analysis methods may be learnt by a study of this primitive converter. The operation of the circuit is as follows.

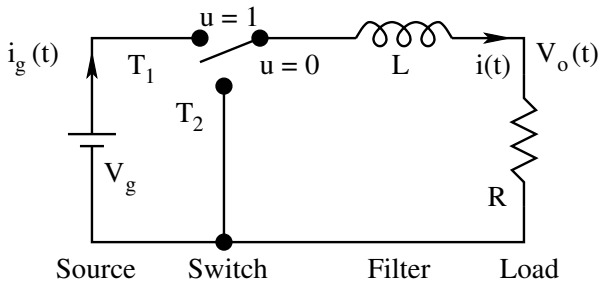

Figure 4.6: A Primitive dc to dc Converter

1. The switch is operated at a constant switching frequency of f_s. The switching period is T_s $(1/f_s)$.

2. For a fraction of the switching period (u = 1), the pole P of the switch is connected to V_g through the throw T_1. The ON time per cycle is dT_s.

3. For the rest of the switching period (u = 0), the pole P of the switch is connected to zero volts through the throw T_2. The OFF time per cycle is $(1-d)T_s$.

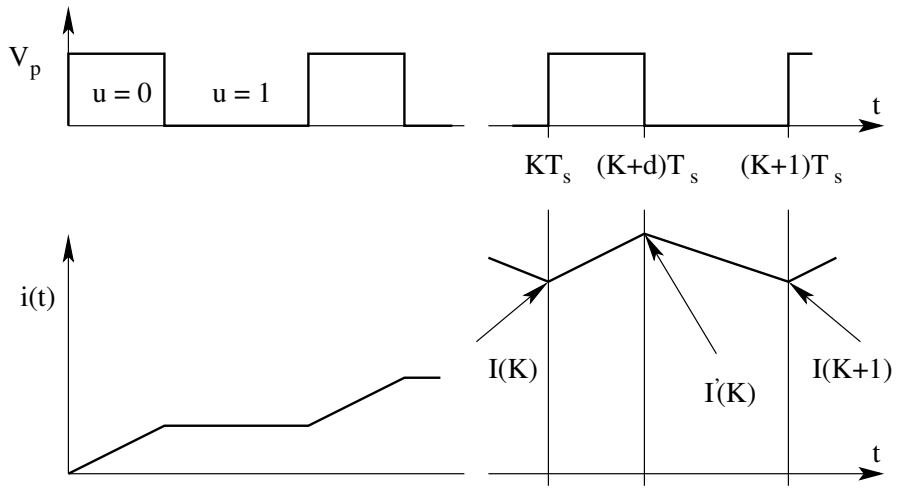

Figure 4.7: Voltage and Current Waveforms in the Primitive Converter

The voltage obtained at the pole of the switch is a function of time and is shown in Fig. 7.

Analysis of the Primitive Converter

In every cycle from kT_S to $(k+d)T_S$ (k = 1, 2, 3...), the pole of the switch is connected to V_g. During ON time,

$$V_g = L\frac{di}{dt} \; + \; R\; i \tag{4.16}$$

$$i(kT_S) = I(k) \tag{4.17}$$

When we redefine from the start of the k^{th} cycle,

$$i(t) = I(k)e^{\frac{-Rt}{L}} + \left\{\frac{V_g}{R}\left[1 - e^{\frac{-Rt}{L}}\right]\right\} \tag{4.18}$$

The current at the end of ON time is found for $t = dT_S$.

$$I^{'}(k) = I(k)e^{\frac{-RdT_S}{L}} + \left\{\frac{V_g}{R}\left(1 - e^{\frac{-RdT_S}{L}}\right)\right\} \tag{4.19}$$

In every cycle from time $(K+d)T_S$ to $(K+1)T_S$ (K=1, 2, 3...), the pole P of the switch is connected to the ground.

During OFF time

,

$$0 = L\frac{di}{dt} \; + \; R\; i \tag{4.20}$$

$$i[(k+d)T_S] = I^{'}(k) \tag{4.21}$$

When we redefine time from the start of the OFF time of the k^{th} cycle,

$$i(t) = I^{'}(k)e^{\frac{-Rt}{L}} \tag{4.22}$$

The current at the end of OFF time is found for $t = (1-d)T_S$

$$I(k+1) = I^{'}(k)e^{\frac{-R(1-d)T_S}{L}} \tag{4.23}$$

If the initial condition $i(0)$ is known, the inductor current $i(t)$ may be found out from the above equations cycle by cycle. We may also solve for the steady state by forcing $I(k) = I(k+1)$ in the above set of equations.

Under steady state,

$$I(k) = I(k+1) = I \tag{4.24}$$

$$I^{'}(k) = I^{'}(k+1) = I^{'} \tag{4.25}$$

$$I^{'} = Ie^{\frac{-RdT_S}{L}} + \left\{\frac{V_g}{R}\left(1 - e^{\frac{-RdT_S}{L}}\right)\right\} \tag{4.26}$$

$$I = I^{'}e^{\frac{-R(1-d)T_S}{L}} \tag{4.27}$$

Combining equations (1.26) & (1.27), we get

$$I^{'} = \frac{V_g}{R}\frac{\left\{1 - e^{-\frac{RdT_S}{L}}\right\}}{\left\{1 - e^{-\frac{RT_S}{L}}\right\}} \tag{4.28}$$

$$I = \frac{V_g}{R}\frac{\left\{e^{-\frac{R(1-d)T_S}{L}} - e^{-\frac{RT_S}{L}}\right\}}{\left\{1 - e^{-\frac{RT_S}{L}}\right\}} \tag{4.29}$$

If we choose the converter element L and the operating switching period such that $L/R << T_S$ then the exponential terms may be approximated by the first two or three terms of the series to obtain the following approximate results. If the result given in Eq. (1.28) confirms our assumption that the ripple factor is indeed low and that I is approximately equal to $I^{'}$ when $L/R << T_S$.
Average Current:

$$\frac{I + I^{'}}{2} \simeq \frac{dV_g}{R} \tag{4.30}$$

Ripple Current:

$$\delta I \simeq \frac{V_g d(1-d)T_S}{L} \tag{4.31}$$

Ripple Factor:

$$\frac{\delta I}{I} = \delta_i \simeq \frac{(1-d)RT_S}{L} \tag{4.32}$$

4.3.2 A Simplified Analysis Of The Primitive Converter

In the earlier section we did an exact solution of the circuit differential equations for steady state and then applied the simplifying assumption that the current ripple is low. We may perform the analysis by assuming that the current and voltage ripple is low to start with and then carry out the analysis. Such a method is more common in the analysis of SMPC. After steady state is reached, $v_o(t)$, $v_L(t)$, $i(t)$ become periodic with period T_S.

$$i(t) = i(t + kT_S) \tag{4.33}$$

Current buildup in the inductor over a period is zero under steady state.

$$\int_0^{T_S} di \;=\; \frac{1}{L} \int_0^{T_S} v_L dt \;=\; 0 \tag{4.34}$$

We may express this in words, as "the inductor volt-sec integral over a cycle is zero under steady state". We may use this criterion along with the assumption that the current ripple is low and the consequent voltage ripple across the load is nearly zero. Such an approach considerably simplifies the analysis. Consider the two sub-circuits of the primitive converter under steady state shown in Fig. 8. The following are the key points of the analysis.

1. DC-to-DC converters will have negligible ripple voltage at the output; $v_o(t) \;\simeq\; V_o$.

2. Volt -sec integral across an inductor over a cycle is zero under steady state. The dual of this property (Amp-sec integral through a capacitor under steady state is zero over a cycle) is also useful in some other converters.

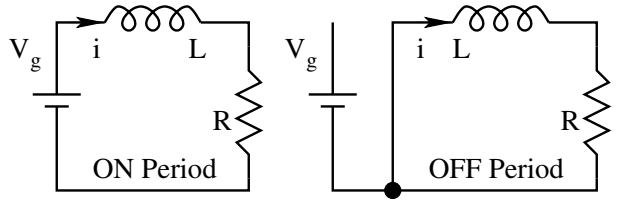

Figure 4.8: Equivalent Circuits of the Primitive Converter

Steady State Output:
Apply volt-sec balance on the inductor

$$(V_g - V_o)dT_S \;-\; V_o(1-d)T_S \;=\; 0 \tag{4.35}$$

$$V_o \;=\; dV_g; I \;=\; \frac{dV_g}{R} \tag{4.36}$$

Current Ripple:
During the ON time of the switch the current in the inductor rises linearly with $di/dt = (V_g - V_o)/L$; (since $v_o(t) \simeq V_o$.)

$$\delta I = \int_0^{T_S} di = \frac{1}{L}\int_0^{T_S}(V_g - V_o)dt = \frac{(V_g - V_o)dT_S}{L} \tag{4.37}$$

$$\frac{\delta I}{I} = \delta_i = \frac{(1-d)RT_S}{L} \tag{4.38}$$

Voltage ripple:

$$\delta V_o = R\delta I = \frac{(V_g - V_o)RT_S}{L} \tag{4.39}$$

$$\frac{\delta V_o}{V_o} = \delta_v = \frac{(1-d)RT_S}{L} \tag{4.40}$$

In order that our analysis results are valid, δ_v must be small. We may ensure

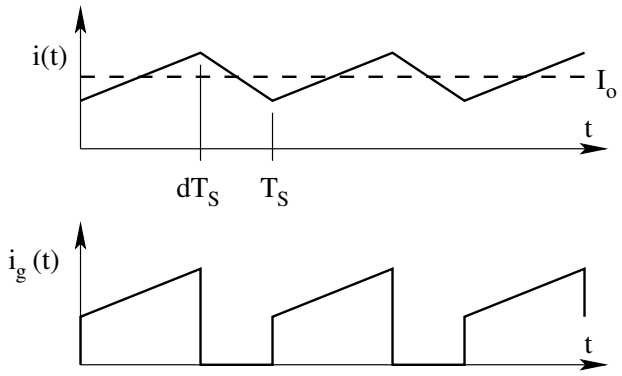

Figure 4.9: Input and Output Currents in the Primitive dc to dc Converter

this by imposing the condition from Eq. (39) that ($T_S << L/R$) the switching period is very much smaller than the natural period (L/R) of the circuit. In the primitive converter that we considered the switch is ideal and so also the inductor. There are no losses in the converter and so the efficiency is unity. The input current and the output current of such a converter is shown in Fig. 9. It may be assumed that the output voltage ripple and the inductor current ripple are small as per the foregoing analysis.

$$I_g = \frac{1}{T_S}\int_0^{T_S} i_g(t)\, dt = \frac{1}{T_S}\int_0^{dT_S} I_o\, dt = dI_o \tag{4.41}$$

For the primitive converter,

$$\frac{V_o}{V_g} = d = \frac{I_g}{I_o} \tag{4.42}$$

This result is in general true for all loss-less converters. The forward voltage transfer ratio will be the same as the reverse current transfer ratio. It is easy to see that the product of the voltage transfer ratio and current transfer ratio is the efficiency of the converter. The efficiency is obviously unity in the case of loss-less converters.

4.3.3 Nonidealities in the Primitive Converters:

In practice a real converter will have several nonidealities associated with the different components in the converter. These are the source resistance (R_g), the parasitic resistance of the inductor (R_l), and the switch voltage drops (V_{sn}: ON period throw conduction drop; V_{sf}: OFF period throw conduction drop). Fig. 10 shows the primitive converter with these nonidealities indicated. We may apply volt-sec balance on the inductor. Considering the nonideality of the inductor and the source

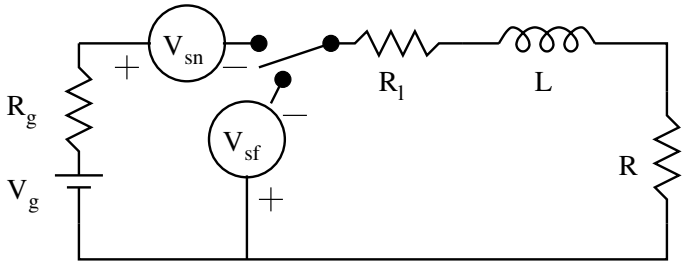

Figure 4.10: Primitive Converter with Different Non-idealities

$$\Big[V_g - I_o R_g - I_o R_l - V_o\Big] dT_S + \Big[-I_o R_l - V_o\Big](1-d)T_S \;=\; 0 \tag{4.43}$$

$$V_o \;=\; dV_g \frac{R}{R + R_l + dR_g} \tag{4.44}$$

$$= \text{Ideal gain * Correction Factor.}$$

The current transfer ratio is unaffected by these (series) nonidealities.

$$\frac{I_o}{I_g} \;=\; \frac{1}{d} \tag{4.45}$$

The overall efficiency of the converter is,

$$\eta = \frac{V_o I_o}{V_g I_g} = \frac{R}{R + R_l + dR_g} \tag{4.46}$$

In a similar way the nonideality of the switches may also be taken into account. Applying volt-sec balance

$$\Big[V_g - I_o R_g - V_{sn} - I_o R_l - V_o\Big] dT_S = \Big[V_{sf} + I_o R_l + V_o\Big](1-d)T_S \tag{4.47}$$

$$dV_g\left[1-\frac{V_{sn}}{V_g}-\frac{V_{sf}(1-d)}{dV_g}\right] \;=\; V_o\left[\frac{R+R_l+dR_g}{R}\right] \tag{4.48}$$

$$V_o \;=\; dV_g\left[1-\frac{V_{sn}}{V_g}-\frac{V_{sf}(1-d)}{dV_g}\right]\left[\frac{R}{R+R_l+dR_g}\right] \tag{4.49}$$

The correction factor consists of two terms; one corresponding to the parasitic resistances in the circuit and the other corresponding to the switch nonidealities. Since the current transfer ratio is unaffected, the voltage gain correction factor directly gives the efficiency of power conversion also.

4.4 More Versatile Power Converters

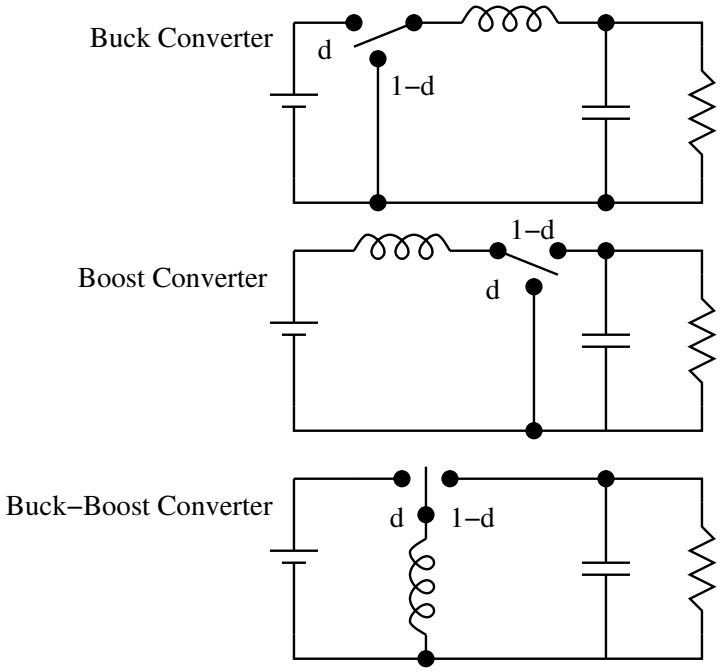

Figure 4.11: Basic Converters

The extension of the primitive dc-to-dc converters to the next level of complexity yields the three basic real converter topologies as shown in Fig. 11. These converters consist of one single pole double throw switch (SPDT), one inductor, and one capacitor each. These three converters are named the buck, the boost, and the buck-boost converters respectively [14, 15]. The steady state analysis of these converters may be done following the same methods developed for primitive converter.

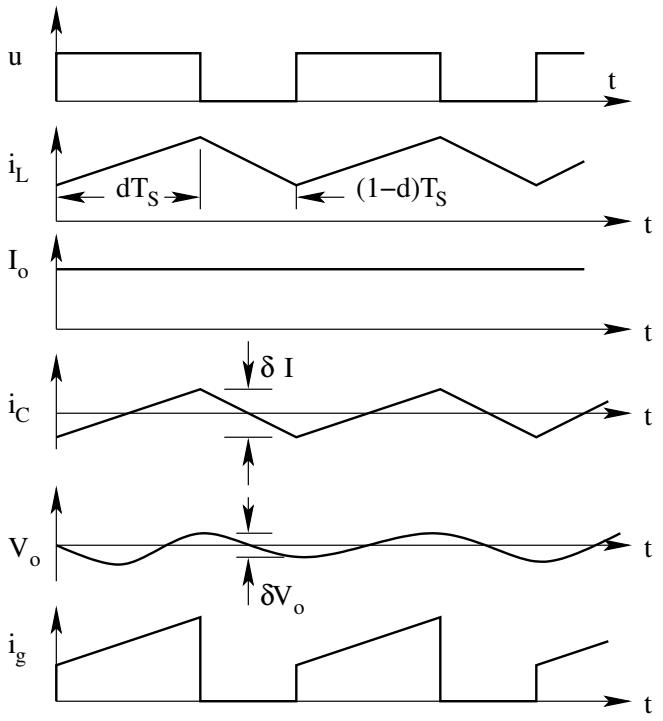

Figure 4.12: Steady State Waveforms of the Buck Converter

4.4.1 Buck Converter

The buck converter steady state waveforms are shown in Fig. 12 We may apply the assumption that the output voltage ripple is low ($\delta_v = \delta V_o/V_o << 1$).

Voltage gain

Apply volt-sec balance on inductor:

$$V_o = dV_g \tag{4.50}$$

Current ripple

In each sub period [dT_S and $(1-d)T_S$], the rate of change of current is constant.

$$\delta I_o = \frac{V_g d(1-d)T_S}{L} = \frac{V_o(1-d)T_S}{L} \tag{4.51}$$

$$\frac{\delta I_o}{I_o} = \delta_i = \frac{(1-d)RT_S}{L} \tag{4.52}$$

Voltage ripple

The charging and discharging current of the capacitor (hatched region in Fig. 12) decides the voltage ripple. We consider that the ac part of the inductor current flows into the capacitor.

$$\delta V_o = \frac{\delta Q}{C} = \frac{1}{C}\frac{1}{2}\frac{\delta I_o}{2}\frac{T_S}{2} \tag{4.53}$$

$$\delta V_o = \frac{V_o(1-d)T_S^2}{8LC} \tag{4.54}$$

$$\frac{\delta V_o}{V_o} = \delta_v = \frac{(1-d)T_S^2}{8LC} \tag{4.55}$$

Input Current

The average of the source current is found as for the primitive converter.

$$I_g = dI_o \tag{4.56}$$

Validity of Results

The results are valid when

$$\frac{\delta V_o}{V_o} = \delta_v = \frac{5(1-d)T_S^2}{T_o^2} << 1 \tag{4.57}$$

In other words, the switching period (T_S) must be very much less than the natural period ($T_o = 2\pi\sqrt{LC}$) of the converter. The important features of the buck converter are

1. The gain is less than unity (hence buck converter)
2. The gain is independent of the switching frequency so long as $T_S << T_o$.
3. The output voltage ripple percentage is independent of the load on the converter.
4. The output ripple has a second order roll-off with the switching frequency.
5. The ideal efficiency is unity. When the nonidealities are considered the efficiency degrades.

$$\eta = \left[1 - \frac{V_{sn}}{V_g} - \frac{V_{sf}(1-d)}{dV_g}\right]\left[\frac{R}{R + R_l + dR_g}\right] \tag{4.58}$$

The efficiency of power conversion is good when $R_l,\ R_g << R, V_{sn} << V_g$, and $V_{sf} << V_o$. Notice that when very low output voltages are required ($V_{sf} \simeq V_o$), or when the source voltage is low and comparable to the switch drop ($V_{sn} \simeq V_g$), the efficiency will be particularly poor.

6. The input current is discontinuous and pulsating. It will therefore be necessary to have an input filter with buck converter, if the source is not capable of supplying such pulsating current.

4.4.2 Boost Converter

The boost converter steady state waveforms are shown in Fig. 13. The analysis is based on similar lines as done for the buck converter.

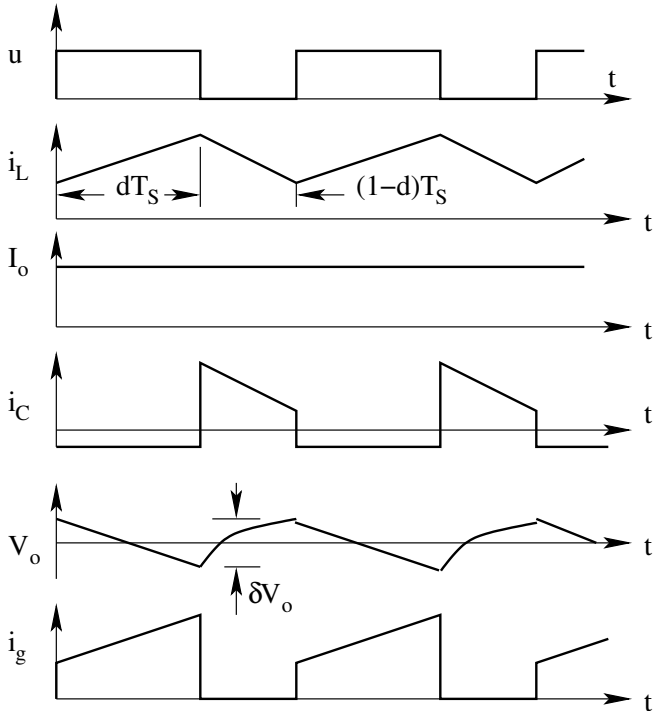

Figure 4.13: Steady State Waveforms of the Boost Converter

Voltage gain

Apply volt-sec balance on inductor.

$$V_o = \frac{V_g}{1-d} \tag{4.59}$$

When the parasitic resistance of the inductor (R_l) and the source resistance (R_g) are taken into account, the voltage gain gets degraded.

$$V_o = \frac{V_g}{1-d}\left\{\frac{1}{1+\frac{\alpha}{(1-d)^2}}\right\} \; ; \; \alpha = \frac{R_l + R_g}{R} \tag{4.60}$$

Current Ripple

In each sub-period [dT_S and $(1-d)T_S$] the rate of change of current is constant.

$$\delta I_L = \frac{V_g d T_S}{L} \tag{4.61}$$

$$\frac{\delta I_L}{I_L} = \delta_i = \frac{d(1-d)^2 R T_S}{L} \tag{4.62}$$

Voltage Ripple

The charging and discharging current of the capacitor (hatched region in Fig. 13) decides voltage ripple. We consider that the entire ac part of the inductor current flows into the capacitor.

$$\delta V_o = \frac{\delta Q}{C} = \frac{I_o d T_S}{C} \tag{4.63}$$

$$\frac{\delta V_o}{V_o} = \delta_v = \frac{d T_S}{RC} \tag{4.64}$$

Input Current

The average of the inductor current is the same as the average source current.

$$I_g = \frac{I_o}{1-d} \tag{4.65}$$

Validity of Results

The results are valid when

$$\frac{\delta V_o}{V_o} \;=\; \delta_v \;=\; \frac{d T_S}{RC} \;<<\; 1 \tag{4.66}$$

In other words, the switching period (T_S) must be very less than the natural period (RC) of the converter. The important features of the boost converter are

1. The gain is more than unity (hence boost converter).
2. The gain is independent of the switching frequency so long as $T_S << RC$. However this design inequality is a function of load.
3. The output voltage ripple percentage is dependent on the load on the converter. The output ripple has a first order roll-off with the switching frequency.

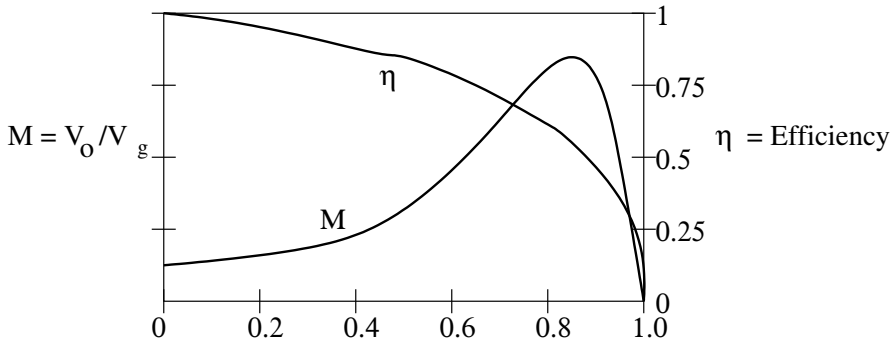

Figure 4.14: Gain and Efficiency of Boost Converter with Non-idealities

4. The parasitic resistance in the converter degrades the gain of the converter. The gain though ideally is a monotonically increasing function, in reality on account of the parasitic resistances, falls sharply as the duty ratio approaches unity. It reaches a peak of $(1/2\sqrt{\alpha}$ $[\alpha = (R_l + R_g)/R]$, and falls rapidly to zero at $d = 1$. The duty ratio at which this peak occurs is at $d = 1 - \sqrt{\alpha}$. The efficiency at this duty ratio will be 0.5, which is quite low. Therefore there is an indirect limit on operating duty ratio. In practice boost converters are not operated beyond a duty ratio of 1/2 to 2/3. The gain and the efficiency of a boost converter (with $\alpha = 0.02$) are shown as a function of duty ratio in Fig. 14.

5. The ideal efficiency is unity. When the nonidealities are considered the efficiency degrades. The efficiency of power conversion is good when $R_l, R_g << R$; $V_{sn} << V_g$; $V_{sf} << V_o$ and at low duty ratios.

$$\eta = \left[1 - \frac{dV_{sn}}{V_g} - \frac{V_{sf}(1-d)}{V_g}\right]\left[\frac{1}{1 + \dfrac{\alpha}{(1-d)^2}}\right] \tag{4.67}$$

6. The input current is continuous. Therefore the boost converter is less sensitive to the dynamic impedance of the source compared to the buck converter.

4.4.3 Buck-Boost Converter

The steady state waveforms of a buck boost converter are shown in Fig. 15. The analysis follows similar lines.

Voltage Gain

Apply volt-sec balance on inductor.

$$V_o = -\frac{dV_g}{1-d} \tag{4.68}$$

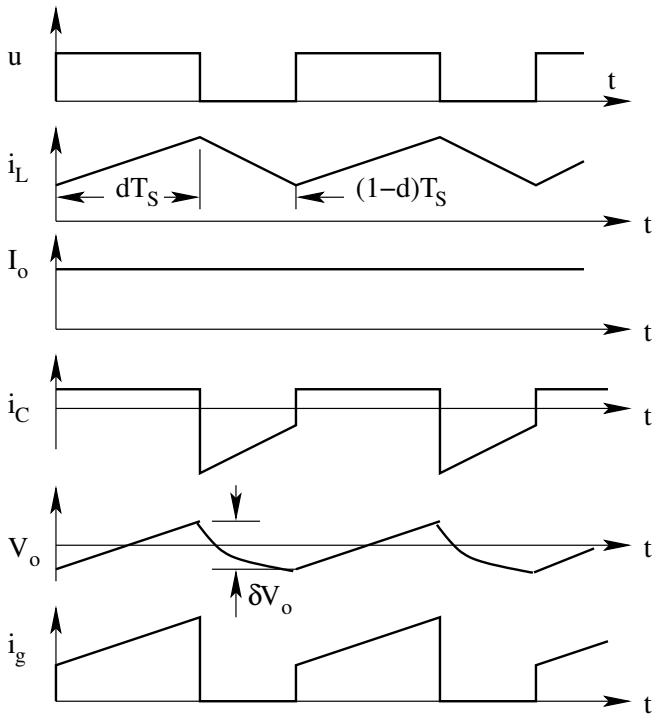

Figure 4.15: Steady State Waveforms of the Boost Converter

When the parasitic resistance of the inductor R_l and the source resistance R_g are taken into account, the voltage gain gets degraded.

$$V_o = \frac{V_g}{1-d}\left\{\frac{1}{1+\dfrac{\alpha+\beta d}{(1-d)^2}}\right\}\ ;\ \alpha = \frac{R_l}{R}; \beta = \frac{R_g}{R} \tag{4.69}$$

Current Ripple

In each sub period [dT_S and $(1-d)T_S$] the rate of change of current is constant.

$$\delta I_L = \frac{V_g d T_S}{L} \tag{4.70}$$

$$\frac{\delta I_L}{I_L} = \delta_i = \frac{(1-d)^2 R T_S}{L} \tag{4.71}$$

Voltage Ripple

The charging and discharging current of the capacitor (hatched region in Fig. 15) decides the voltage ripple. We consider that the entire ac part of the

inductor current flows into the capacitor.

$$\delta V_o = \frac{\delta Q}{C} = \frac{I_o d T_S}{C} \tag{4.72}$$

$$\frac{\delta V_o}{V_o} = \delta_v = \frac{dT_S}{RC} \tag{4.73}$$

Input Current

The average source current may be obtained from the average inductor current.

$$I_g = \frac{dI_o}{1-d} \tag{4.74}$$

Validity of Results

The results are valid when

$$\frac{\delta V_o}{V_o} \;=\; \delta_v \;=\; \frac{dT_S}{RC} \;<<\; 1 \tag{4.75}$$

In other words, the switching period (T_S) must be very much less than the natural period ($T_o = RC$) of the converter. The important features of the buck-boost converter are

1. The gain may be set below or above unity (hence buck-boost converter). The output polarity is opposite to that of the input polarity.

2. The gain is independent of the switching frequency so long as ($T_S << RC$). However this design inequality is a function of the load.

3. The output voltage ripple percentage is dependent on the load on the converter. The output ripple has a first order roll-off with the switching frequency.

4. The parasitic resistances in the converter degrade the gain of the converter. The gain though ideally is a monotonically increasing function, in reality on account of the parasitic resistances, falls sharply as the duty ratio approaches unity. It reaches a peak of

   $$V_o(max) = \sqrt{\alpha+\beta}/[2\alpha + 2\beta - \beta\sqrt{\alpha+\beta}] \tag{4.76}$$

   and falls rapidly to zero at $d = 1$. The duty ratio at which this peak occurs is at $d = 1 - \sqrt{\alpha+\beta}$. The efficiency at this duty ratio will be about 0.5, which is quite low. Therefore there is an indirect limit on the operating duty ratio. In practice buck-boost converters are not operated beyond a duty ratio of about 1/2 to 2/3.

5. The ideal efficiency is unity. When the nonidealities are considered the efficiency degrades.

$$\eta = \left[1 - \frac{V_{sn}}{V_g} - \frac{V_{sf}(1-d)}{dV_g}\right]\left[\frac{1}{1 + \dfrac{\alpha + \beta d}{(1-d)^2}}\right] \tag{4.77}$$

   The efficiency of power conversion is good when and $R_l, R_g << R$; $V_{sn} << V_g$; $V_{sf} << V_o$ at low duty ratios.

6. The input current is discontinuous and pulsating. It will therefore be necessary to have an input filter also with buck-boost converter, if the source is not capable of supplying such pulsating current.

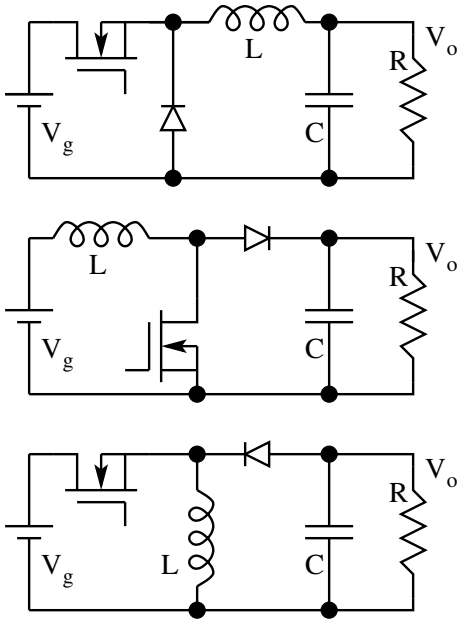

Figure 4.16: Practical Configuration of Three Basic dc to dc Converters

Table 1 gives the summary of the steady state results for the three basic converters. The practical realization of the three converters with controlled (transistor) and uncontrolled (diode) switches for unidirectional power conversion is shown in Fig. 16.

4.5 Discontinuous Mode of Operation in dc to dc Converters

In the analysis of the dc-to-dc converters in the previous section we forced a condition that the output ripple voltage is small. This is absolutely essential

Table 4.1: Steady State Performance of Basic Converters in CCM

	Buck	Boost	Buck-Boost
Ideal Gain	d	$\frac{1}{1-d}$	$-\frac{d}{1-d}$
Current Ripple	$\frac{(1-d)RT_S}{L}$	$\frac{d(1-d)^2RT_S}{L}$	$\frac{(1-d)^2RT_S}{L}$
Voltage Ripple	$\frac{(1-d)T_S^2}{8LC}$	$\frac{dT_S}{RC}$	$\frac{dT_S}{RC}$
Duty Ratio	$\frac{2}{3} \leq d \leq 1$	$0 \leq d \leq \frac{2}{3}$	$0 \leq d \leq \frac{2}{3}$
Efficiency degradation on account of different non-idealities Note: $\alpha = \frac{R_l}{R}$; $\beta = \frac{R_g}{R}$;			
R_l and R_g	$\frac{1}{1+\alpha+\beta d}$	$\frac{1}{1+\frac{\alpha+\beta}{(1-d)^2}}$	$\frac{1}{1+\frac{\alpha+\beta d}{(1-d)^2}}$
V_{sn} and V_{sf}	$1-\frac{V_{sf}}{V_g}-\frac{V_{sf}}{dV_g}$	$1-\frac{V_{sn}}{V_g}-\frac{(1-d)V_{sf}}{V_g}$	$1-\frac{V_{sn}}{V_g}-\frac{(1-d)V_{sf}}{dV_g}$

in order that the load connected to the dc-to-dc converter sees an ideal dc voltage source at the output of the converter. However, the inductor current in the dc-to-dc converter is an internal quantity of the converter and it is not necessary that the inductor current ripple is small. We have seen that the current ripple in all the basic converters is a function of $[T_S/(L/R)]$. It is possible to operate the converter at low switching frequency or with a low value of inductance where the current ripple is high. We have also seen that

the ripple voltage in all the basic converters is inversely proportional to the filter capacitance. Hence it is possible to independently control the voltage ripple to be small (with high ripple current). A typical buck converter realized

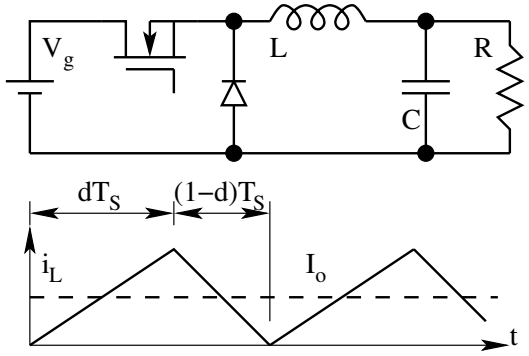

Figure 4.17: Practical Configuration of Three Basic dc to dc Converters

with electronic switches and the inductor current waveform is shown in Fig. 17. The transistor conducts during dT_s and the diode conducts during d_2T_s. Consider the case when T_s is further increased keeping "d" to be the same. The current waveform is shown in Fig. 18. Notice that now the currents through the switching elements tend to be bi-directional. The power circuit shown in Fig. 17 cannot support this mode of operation since the switches can carry only unidirectional current. In such a case the converter enters a mode of operation called the discontinuous inductor current mode (DCM) of operation. In such an operation the inductor current starts in every cycle from zero current and before the end of the cycle falls back to zero. The discontinuous mode (DCM) of operation results in steady state performance that is different from the continuous inductor current mode of operation (CCM) that we have seen earlier.

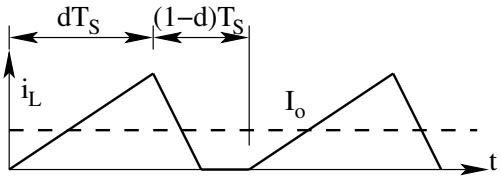

Figure 4.18: Practical Configuration of Three Basic dc to dc Converters

4.5.1 Buck converter in DCM Operation

The equivalent circuits of the buck converter in the various sub periods and the steady state inductor current and voltage are shown in Fig. 19. Again

the output voltage is assumed to have negligible ripple. The current in the inductor periodically goes to zero. There are three sub-periods in a cycle.

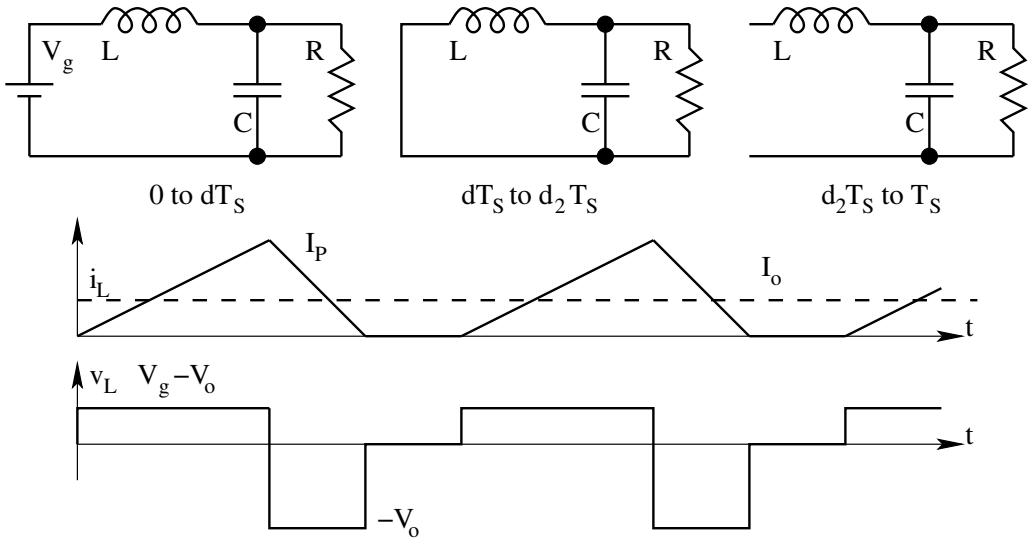

Figure 4.19: Practical Configuration of Three Basic dc to dc Converters

1. During dT_S, energy is pumped from the source and the inductor current ramps up.

2. During d_2T_S, energy from the reactors feed the load and the inductor current ramps down.

3. During $(1-d-d_2)T_S$, inductor has no energy and the capacitor supplies the load.

The analysis of the converter is done as before invoking the condition that the output voltage ripple is negligible.

Voltage Gain

Apply volt-sec balance on the inductor,

$$(V_g - V_o)dT_S + (-V_o)d_2T_S = 0 \tag{4.78}$$

$$\frac{V_o}{V_g} = \frac{d}{d+d_2} \tag{4.79}$$

This is not a very useful form of result. d is the control input and is the independent variable. d_2 depends on d and the circuit parameters T_S, L, R etc. It will be more useful to determine the gain V_o/V_g (defined M) in terms

of independent control variable d and the parameters of the circuit. d and d_2 are related through I_P and I_o.

$$I_P = \frac{d_2 T_S V_o}{L} \tag{4.80}$$

$$I_o = \frac{V_o}{R} = \frac{I_P(d + d_2)}{2} \tag{4.81}$$

Combining Eqns () and (), we get

$$d_2(d + d_2) = \frac{2L}{RT_S} = K \tag{4.82}$$

K is defined as the conduction parameter of the converter. Equation (82) relates d_2 to d and the parameters of the converter. Solving for the dependent quantity d_2, we get

$$d_2 = \frac{-d + \sqrt{d^2 + 4K}}{2} = \frac{-d + d\sqrt{1 + \frac{4K}{d^2}}}{2} \tag{4.83}$$

$$M = \frac{2}{1 + \sqrt{1 + \frac{4K}{d^2}}} \tag{4.84}$$

Equations (83) and (84) give the intermediate variable d_2 and the voltage gain under DCM in terms of the control variable d and the circuit parameters of the converter ($K = 2L/RT_S$). It may be observed that the gain under DCM is more than that obtained under CCM.

Current Ripple

In each sub period, the rate of change of current is constant; $(V_g - V_o)/L$ during dT_S, V_o/L during d_2T_S, and zero during the rest of the period.

$$\delta I_L = I_P = \frac{V_o d_2 T_S}{L} \tag{4.85}$$

$$\frac{\delta I_L}{I_L} = \delta_i = \frac{2}{d + d_2} \tag{4.86}$$

Voltage Ripple

The voltage ripple is decided by the capacitor current (hatched region in Fig. 19)

$$\delta V_o = \frac{\delta Q}{C} = \frac{(d + d_2)(I_P - I_o)^2}{2CI_P} \tag{4.87}$$

$$\frac{\delta V_o}{V_o} = \delta_v = \frac{\left(1 - \frac{1}{\delta_i}\right)^2}{RC} \tag{4.88}$$

Input Current

The input current is drawn only during dT_S.

$$I_g = \frac{I_o d}{d + d_2} \tag{4.89}$$

In order that our analysis results are valid, $\delta V_o/V_o$ must be small. We may ensure this by imposing the condition from Eq. () that $\left(1 - \frac{1}{\delta_i}\right)^2 < RC$. The most important features of buck converter in DCM are

1. The gain is less than unity; but more than that in CCM operation for the same duty ratio.
2. The gain is independent of the switching frequency through the conduction parameter ($K = 2L/RT_S$).
3. The output ripple percentage is dependent of the load on the converter through the conduction parameter K. The output ripple has a first order roll-off with the switching frequency.
4. The ideal efficiency is unity. When the nonidealities are considered the efficiency degrades.

$$\eta = \left[1 - \frac{V_{sn}}{V_g} - \frac{V_{sf} d_2}{d V_g}\right]\left[\frac{1}{1 + \frac{\alpha d_2}{K}}\right]; \alpha = \frac{R_l}{R} \tag{4.90}$$

   The efficiency of power conversion is good when $R_l, R_g << R$; $V_{sn} << V_g$; $V_{sf} << V_o$. Notice that when very low output voltages are required (V_{sf} nearly equal to V_o), the efficiency will be particularly poor.

5. The input current is discontinuous and pulsating. It will therefore be necessary to have an input filter also with the buck converter, if the source is not capable of supplying such pulsating current.
6. When the duty ratio is such that , the converter will be operating on the boundary between continuous and discontinuous mode of operation. We may find out the value of the conduction parameter K_{cri}, which will cause this boundary at the duty ratio of d. This is found by equating $d_2 = (1 - d)$ for $K = K_{cri}$.

$$d_2 = (1 - d) = \frac{-d + d\sqrt{1 + \frac{4K_{cri}}{d^2}}}{2} \tag{4.91}$$

$$K_{cri} = (1 - d) \tag{4.92}$$

Fig. 20 shows the value of K_{cri} as a function of duty ratio d. If the

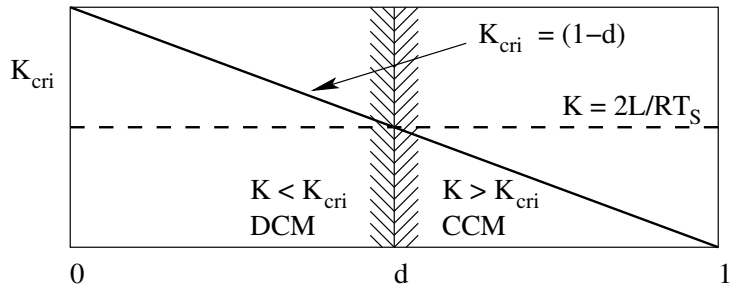

Figure 4.20: Regimes of CCM and DCM as a Function of K

conduction parameter K is known for a converter, then we may see that for all duty ratios when K is less than K_{cri}, the converter will operate in DCM. For all duty ratios when K is greater than K_{cri}, the converter will operate in CCM.

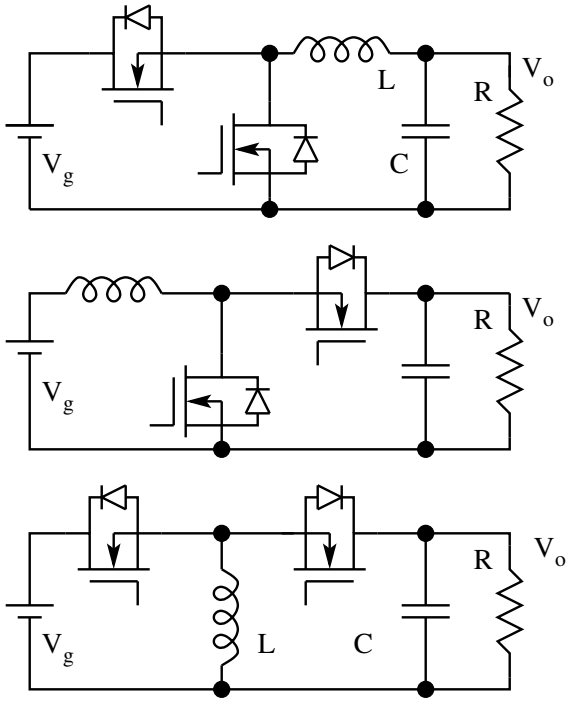

Figure 4.21: Three Basic dc to dc Converters to Operate in CCM

Table. 2 shows the quantities of interest in the other converters when they are operated in DCM. It is left as an exercise to carry out the analysis and verify these quantities. In case, the converters are to be operated only in CCM, realizing the switches in the converter with bi-directional switches as shown in Fig. 21 is needed.

Table 4.2: Steady State Performance of Basic Converters in DCM

	Buck	Boost	Buck-Boost
Ideal Gain	$\frac{d}{d+d_2}$	$\frac{d+d_2}{d}$	$-\frac{d}{d_2}$
d_2	$\frac{K}{d}\frac{2}{\left\{1+\sqrt{1+\frac{4K}{d^2}}\right\}}$	$\frac{K}{d}\frac{\left\{1+\sqrt{1+\frac{4d^2}{K}}\right\}}{2}$	$\sqrt{K}$
Peak Current	$\frac{(V_g-V_o)dT_S}{L}$	$\frac{V_g dT_S}{L}$	$\frac{V_g dT_S}{L}$
K_{cri}	$(1-d)$	$d(1-d)^2$	$(1-d)^2$
Efficiency degradation on account of different non-idealities Note: $\alpha=\frac{R_l}{R}$; $\beta=\frac{R_g}{R}$;			
R_l and R_g	$\frac{1}{1+\alpha+\beta d}$	$\frac{1}{1+\frac{\alpha+\beta}{(1-d)^2}}$	$\frac{1}{1+\frac{\alpha+\beta d}{(1-d)^2}}$
V_{sn} and V_{sf}	$1-\frac{V_{sf}}{V_g}-\frac{V_{sf}}{dV_g}$	$1-\frac{V_{sn}}{V_g}-\frac{(1-d)V_{sf}}{V_g}$	$1-\frac{V_{sn}}{V_g}-\frac{(1-d)V_{sf}}{dV_g}$

4.6 Isolated dc to dc Converters

The converters seen in the previous sections are the basic dc-to-dc converters. The outputs in those converters are not electrically isolated from each other. Though such converters find limited applications in power conversion, the

majority of the dc-to-dc converters require that the input and the output are galvanically isolated form each other. Several circuits with the feature of isolation between the input and output are derived from these basic converters. Some of these isolated converters are briefly indicated in this section.

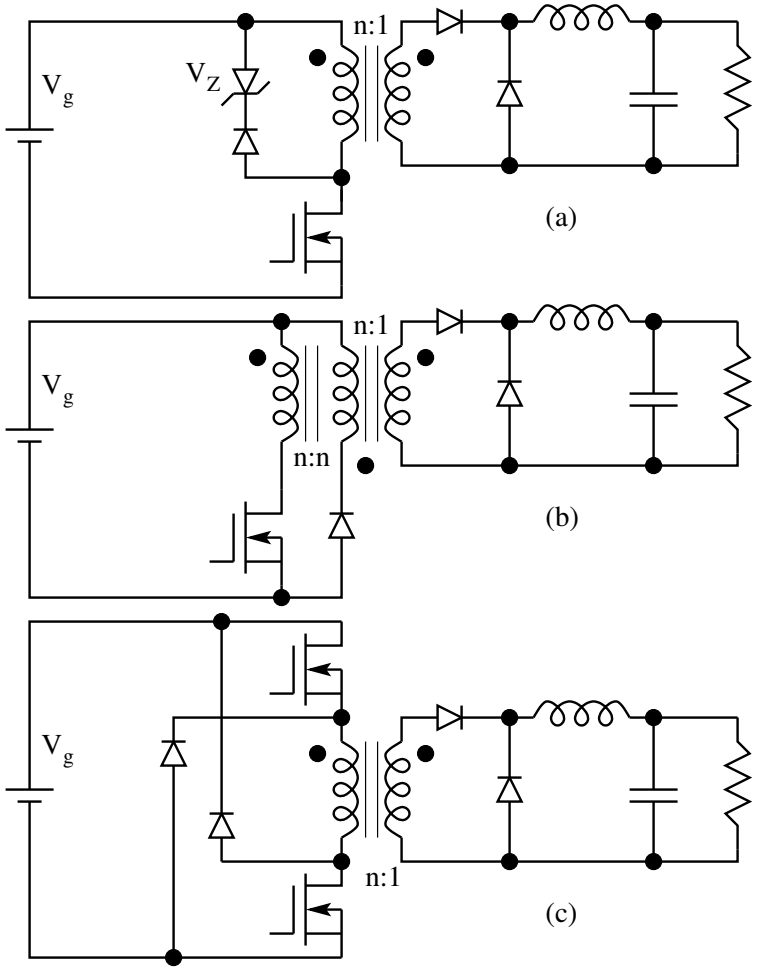

Figure 4.22: Three Versions of Forward Converter

4.6.1 Forward Converter

The forward converters are shown in Fig. 22 are derived from the buck converter. The ideal gain of this converter under CCM is $V_o/V_g = d/n$. Figure 22 shows three variations of the forward converter. The magnetizing current is reset in the circuit shown in Fig. 22a dissipatively. The same feature in the circuits shown in Fig. 22b and 22c is achieved conservatively. The duty ratio of operation is limited; $0 \leq d \leq V_z/(V_g + V_z)$ for the circuit in Fig. 22a, and $0 \leq d \leq 0.5$ for the circuits shown in Fig. 22b and 22c. The output ripple

frequency is same as the switching frequency. In all these converters, both DCM and CCM operation are possible. Next to fly-back converter (explained later in this chapter) this is the simplest among the dc-to-dc converters and is preferred topology for low power dc-to-dc converters (upto about 100W).

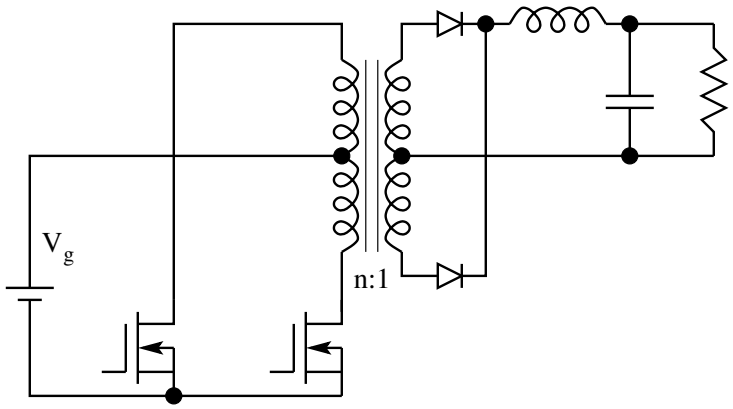

Figure 4.23: Push-Pull Converter

4.6.2 Push-Pull converter

This circuit shown in Fig. 23 is also derived from the buck converter. The ideal gain in CCM is $V_o/V_g = d/n$. The secondary switches are passive switches (diodes). The primary switches are controlled switches operating in push-pull fashion. Notice the diodes in the primary to handle the magnetising energy of the isolation transformer. The duty ratio of each of the switches is variable in the range of 0 to 0.5. The output ripple frequency is double that of the switching frequency of the primary switches. Adequate care - like matched pair of switches - has to be taken in the design to prevent the saturation of the isolation transformer. Both DCM and CCM operation are possible. This circuit is preferred for power converters with low input dc voltages (less than 12V) and medium output power (about 200W).

4.6.3 Half and Full Bridge Converter

These circuits shown in Figs. 24a and 24b are also derived from the buck converter. The control of the switches is in push-pull fashion ($0 \leq d \leq 0.5$) for the half bridge converter. The voltage gain is $V_o/V_g = d/n$. Notice the diodes used in half bridge converter to handle the magnetizing energy of the isolation transformer. In the full bridge converter the control is by the phase difference between the two halves of the bridge with the switches in each arm switched with 50% duty ratio. The primary switches are bi-directional controlled switches in order to handle the magnetising energy of the isolation

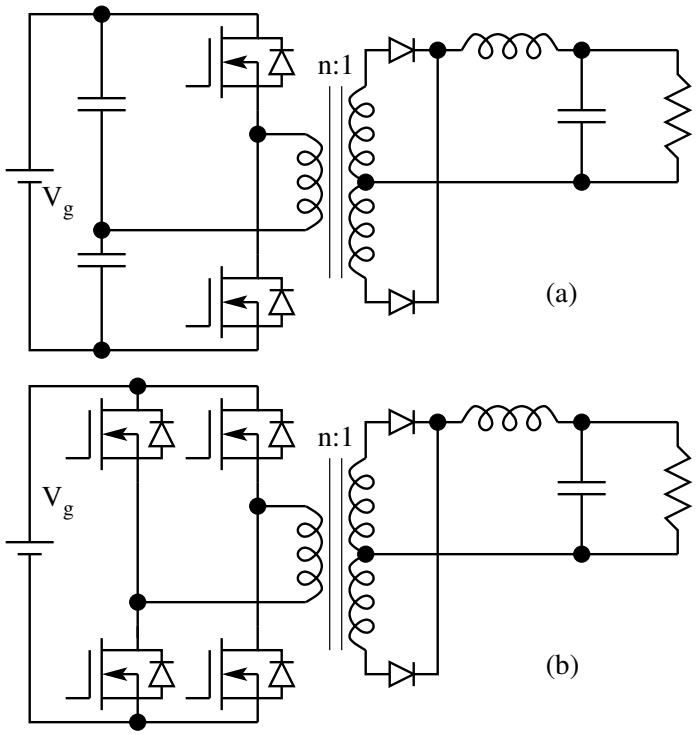

Figure 4.24: Half-Bridge and Full-Bridge Converter

transformer. The gain of the converter is $V_o/V_g = d/n$ where the duty ratio d is seen on the secondary output. The secondary switches are passive switches (diodes). There is no possibility of saturation of the isolation transformer on account of the dc blocking employed in the primary circuit. The ripple frequency at the output is double the switching frequency of the primary switches. Both DCM and CCM operation are possible. Most high power converters (above 200 W) are designed with bridge circuits.

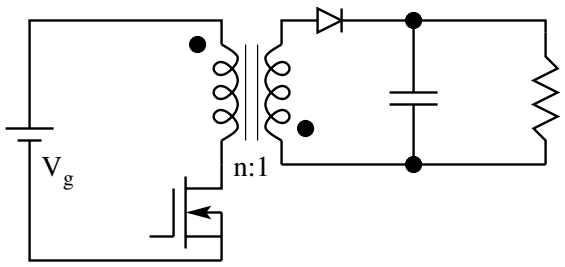

Figure 4.25: Flyback Converter

4.6.4 Fly-back Converter

The circuit shown in Fig. 25 is the fly-back converter derived from the buck-boost converter. The isolation is achieved through a coupled inductor (Note: The isolation element is not a transformer in that it is capable of storing energy). The ideal gain in CCM is $V_o/V_g = d/n(1-d)$. The output ripple frequency is same as switching frequency. Both DCM and CCM operation are possible. This circuit employs the minimum number of components among all the dc-to-dc converters. (one active switch, one passive switch, one magnetic element and one capacitor) and hence preferred circuit for low power (upto about 500W).

Circuit topologies of several other converters are given in the following link.

High frequency power converters

4.7 Problem Set

1. The following circuit shown in Fig. P1 is a zener regulator. The zener employed has a nominal voltage drop of 15V and a dynamic resistance of 15 mΩ. The minimum current required for the zener to operate in its constant voltage characteristics is 20 mA. The source voltage varies in the range of 25 to 35 V. The Series resistance is 50Ω.

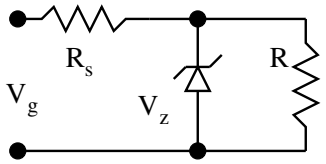

Fig. P 4.1: Shunt Regulator

   (A) Evaluate the range of load resistance for which the output voltage will be regulated.

   (B) Evaluate the maximum power dissipation in R_s and V_z.

2. The superposition principle and Thevenin's theorem may be applied to find an equivalent circuit of Fig. P1. This is shown in Fig. P2 below.

   (A) Evaluate k_1.

   (B) Evaluate k_2.

   (C) Evaluate R_{th}.

   (D) Evaluate line regulation ($\delta V_o/\delta V_g$) - for this δV_z and δI_o are zero.

   (E) Evaluate line regulation ($\delta V_o/\delta I_o$) - for this δV_z and δV_g are zero.

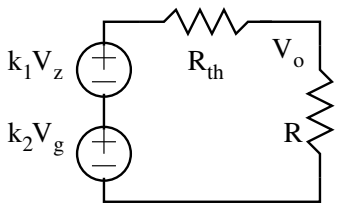

Fig. P 4.2: Equivalent Circuit of the Shunt Regulator

3. The circuit in Fig. P3 is a switched mode converter belonging to the quadratic converter family. It consists of on active switch (S_1) and three passive switches D_1, D_2 and D_3. It has four energy storage elements - two inductors (L_1, L_2) and two capacitors (C_1, C_2). Consider that the currents through the inductor and voltage across the capacitors are all continuous. The switch S_1 is on during T_{on} and Off during T_{off}. The duty ratio of S_1 may be designated as D. The switch drops may be taken to be zero during conduction.

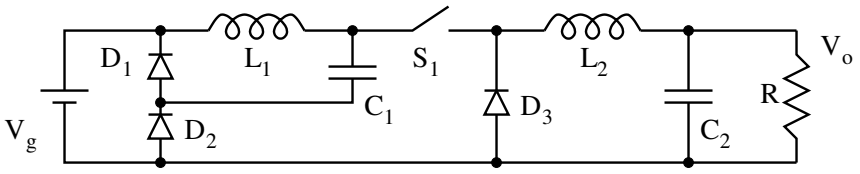

Fig. P 4.3: A Quadratic Converter

(A) Indicate the duty ratios of the three diodes D_1, D_2 and D_3.

(B) Evaluate the steady-state inductor currents (I_1, I_2) and the steady state capacitor voltages (V_{C1}, V_{C2}).

(C) Evaluate the voltage conversion ratio V_o/V_g.

(D) Sketch the steady-state waveforms of (I_1, I_2, V_{C1}, and V_{C2}).

(E) Evaluate the ripple currents δI_1 and δI_2 in terms of V_g, D, L_1, L_2 and R.

(F) Evaluate the ripple voltages δV_{C1} and δV_{C2} in terms of V_g, D, L_1, L_2, C_1, C_2, and R.

4. Figure P4 shows a forward converter operating at a duty ratio of 0.3. The transistor while ON drops a voltage of 1.0 V, and the diode while ON drops a voltage of 0.7 V.

(A) Evaluate the output voltage and efficiency of the converter.

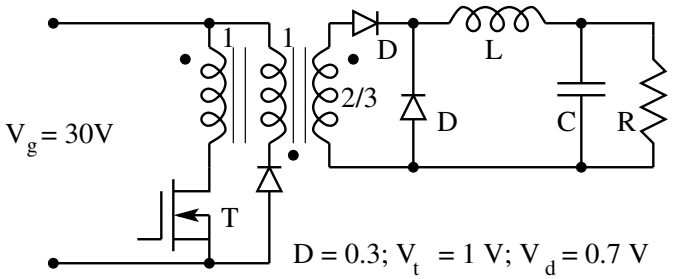

Fig. P 4.4: A Loss-less Forward Converter

5. Figure P5 shows a fly back converter operating at a duty ratio of 0.3. The transistor ON state drop is 1 V. The diode ON state drop is 0.7 V. The resistance of the inductor windings is 0.5Ω and 0.25Ω for the primary and secondary respectively.

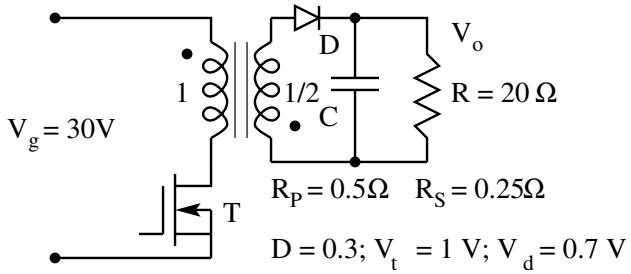

Fig. P 4.5: A Flyback Converter

(A) Evaluate the voltage conversion ratio and efficiency of the converter.

6. Figure P6 shows a forward converter operating at a duty ratio of 0.4. Assume the components to be ideal. Sketch the following waveforms under steady state.

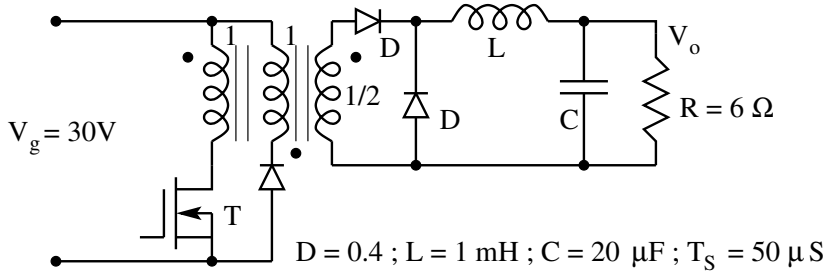

Fig. P 4.6: A Forward Converter

(A) Inductor current.

(B) Secondary current.

(C) Primary current.

(D) Output voltage.

7. Figure P7 shows a non-isolated buck converter operating at a duty ratio of 0.5 at a switching frequency of 20 kHz. The components may be taken to be ideal.

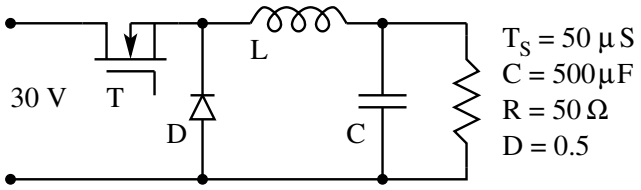

Fig. P 4.7: A Non-isolated Buck Converter

(A) Evaluate the value of L such that the converter operates in the discontinuous mode.

(B) Evaluate the diode conduction time and the output voltage under such condition.

8. The following circuit shown in Fig. P8 shows a variant of the boost converter. The inductor used is a coupled inductor. Assume the components to be ideal.

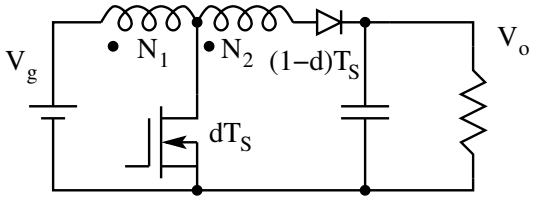

Fig. P 4.8: A Tapped Boost Converter

(A) Determine the voltage conversion ratio of the converter.

9. The following circuit shown in Fig. P9 is a converter capable of being used as a switched mode audio amplifier. Assume the components to be ideal.

(A) Determine the voltage conversion ratio of the converter.

(B) Comment on the important feature of this converter.

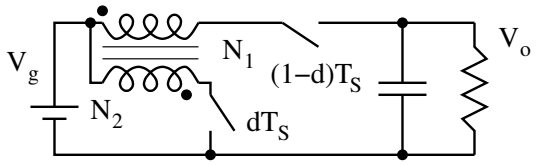

Fig. P 4.9: An Audio Amplifier

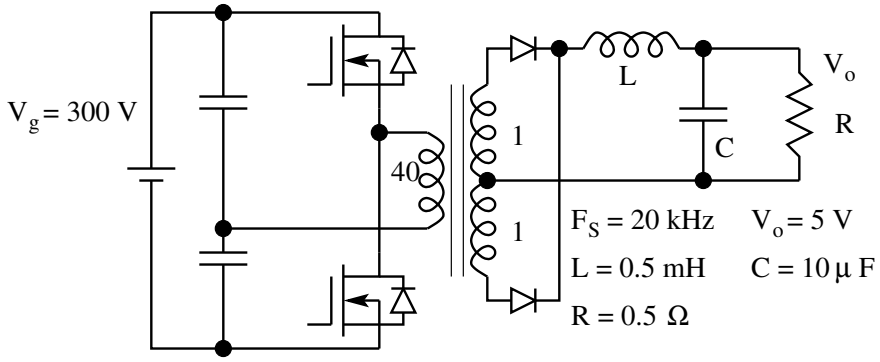

Fig. P 4.10: An Half-Bridge Converter

10. Figure P10 shows a half bridge converter. Make suitable simplifying assumptions. Evaluate the

    (A) Operating duty ratio.

    (B) Current ripple in the inductor.

    (C) Voltage ripple at the output.

    (D) Average input current under steady state.

11. The output section of an SMPS is shown in Fig. P11. The duty ratio seen on the secondary side is 0.8. The dc current through the inductor is 10A with negligible ripple.

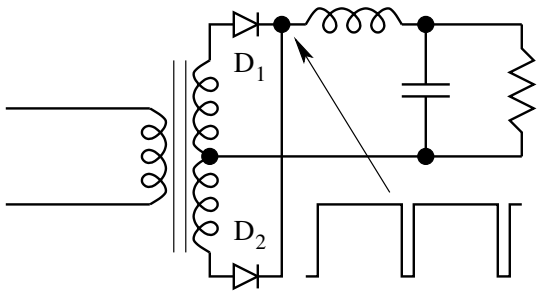

Fig. P 4.11: An Half-Bridge Converter

(A) Sketch the current through D_1 and D_2.

(B) Evaluate the average and rms current through D_1 and D_2.

(C) The diodes D_1 and D_2 have a threshold voltage of 0.85 V, and a dynamic resistance of 25 mΩ. Evaluate the conduction loss in the diodes.

12. For the switching converter circuit shown in Fig. P12, the switch S is ON during dT_S. The diode is ON during $(1-d)T_S$. Assume ideal behaviour and continuous conduction.

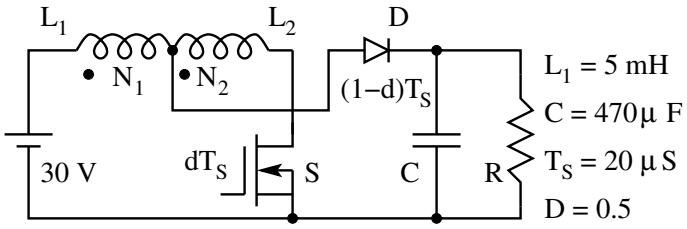

Fig. P 4.12: A Tapped Boost Converter

(A) Evaluate the voltage conversion ratio V_o/V_g.

(B) For $N_1 : N_2$ equal to 1:1, and a duty ratio of 0.5, sketch the steady state input current for one cycle.

(C) Evaluate the output voltage and the ripple voltage on the same.

13. Figure P13 shows a boost converter cascaded by a buck converter. The switches S and $\overline{S}$ are ON during dT_S and $(1-d)T_S$ respectively.

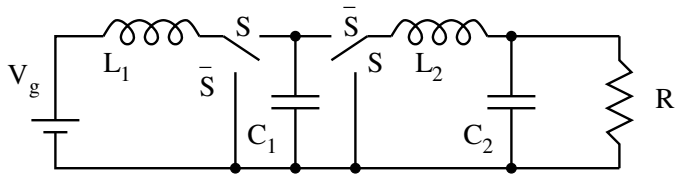

Fig. P 4.13: A Boost Converter and Buck Converter in Cascade

(A) Evaluate the steady state currents in L_1 and L_2 in terms of I_o and d.

(B) Evaluate the steady state voltages across C_1 and C_2 in terms of V_g and d.

(C) Evaluate the current ripples in L_1 and L_2.

(D) Evaluate the voltage ripple in C_1 and C_2.

14. Figure 14 shows a dc current to dc voltage converter.

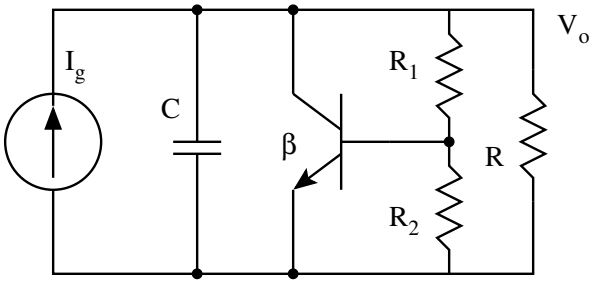

Fig. P 4.14: A Linear Shunt Regulator

(A) Draw the linear equivalent circuit of the converter.

(B) Write down the defining equations of the equivalent circuit.

(C) Solve the above equation to obtain $V_o = f(I_g, V_z, R_o, R_1, R_2, C, \beta)$.

(D) Make suitable design assumptions such that the above relationship becomes a strong function of V_o and a weak function of I_g.

(E) Write down the approximate result $V_o = g(V_z)$.

15. Figure P15 shows the power circuit of a Cuk converter. The components are ideal. Evaluate the voltage transfer ratio (V_o/V_g) of the converter.

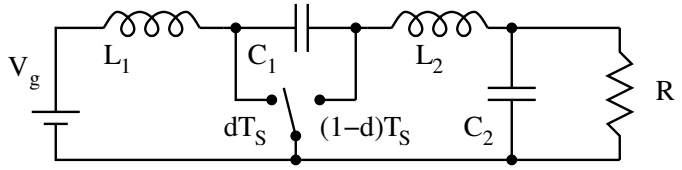

Fig. P 4.15: Cuk Converter

16. Figure P6 shows a 20 W fly back converter. Make suitable assumptions and evaluate the following.

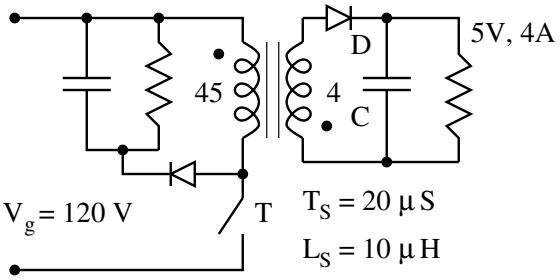

Fig. P 4.16: Flyback Converter

(A) Operating mode (CCM or DCM).

(B) Operating duty ratio.

(C) The primary current wave shape and its peak value.

(D) Voltage across.

17. Figure P17 shows a 500 W half-bridge converter. The capacitance C_f is used to block dc to the transformer. Make suitable assumptions and verify that the value of the blocking capacitor $(2.2\mu F, 400V)$ is satisfactory.

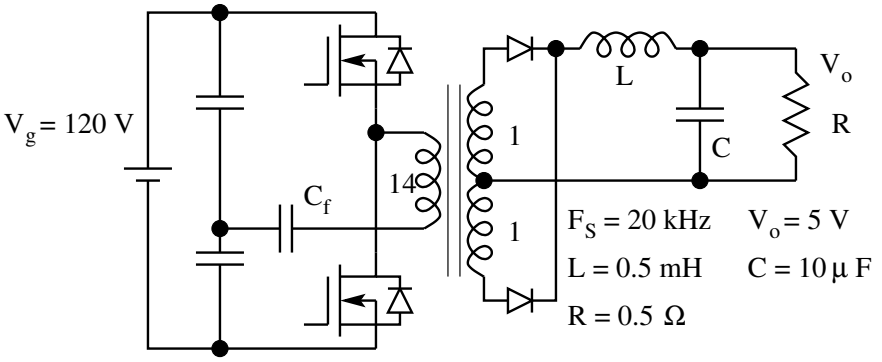

Fig. P 4.17: Half-Bridge Converter

18. Consider the circuit given in Fig. P18. Carry out the steady state analysis for the same and evaluate the following.

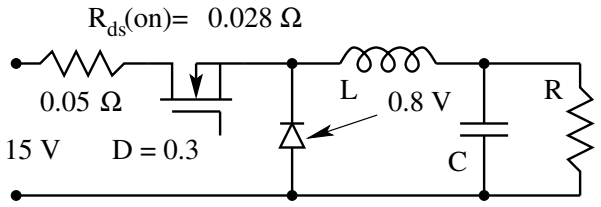

Fig. P 4.18: Buck Converter

(A) Output voltage.

(B) Average input current.

(C) Output power.

(D) Efficiency.

(E) Power dissipation in the MOSFET and the diode

19. Consider the fly back converter shown in Fig. P19. The core flux in the inductor may be considered ripple free. Evaluate the following.

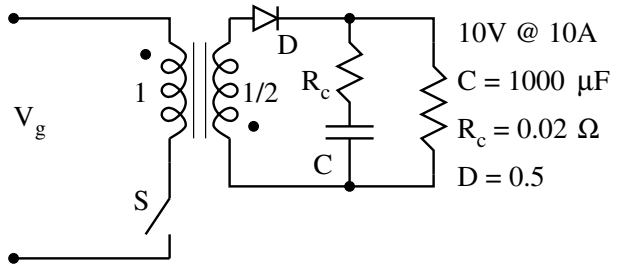

Fig. P 4.19: Buck Converter

(A) Peak and rms primary and secondary currents.

(B) Rms current in the capacitor.

(C) Losses in the ESR of the capacitor.

(D) Impedance plot of the capacitor ($|Z|$ in dBΩ vs Freq in Hz), and the frequency to which the capacitor may be considered good.

20. Consider the two switch forward converter shown in Fig. P20. The output power is 22.5W. The operation is in DCM.

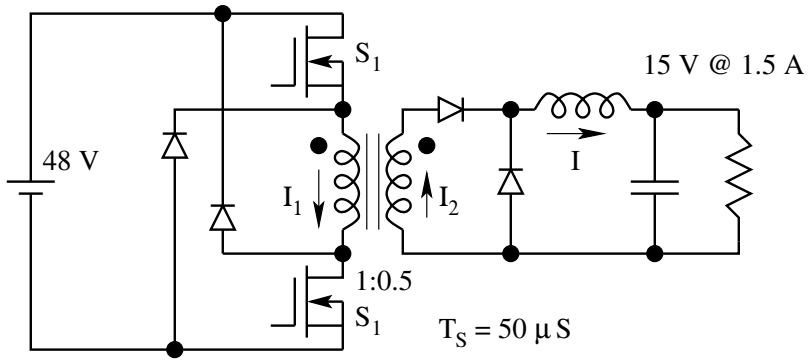

Fig. P 4.20: Buck Converter

(A) Evaluate L such that the freewheeling diode conducts for one half of the OFF interval of switch S_1.

(B) Evaluate the operating duty ratio under this condition.

(C) Evaluate the value of C such that the output voltage ripple is 1%.

(D) Sketch the waveforms of I_1, I_2, and I. Mark the salient features.

Chapter 5

DC-TO-DC Converter – Dynamics

5.1 Introduction

Switched mode power converters (SMPC) consist of switches for the control of power flow, and reactive circuit elements (inductors and capacitors) for attenuating the switching ripple (low pass function) in the output power. The basic power circuit topologies of SMPC were seen in Chapter 4. Evaluation of steady state performance of the converter such as voltage gain (V_o/V_g), efficiency (η), output voltage ripple (δ_v), inductor current ripple (δ_i), etc are shown in Chapter 4 for the ideal converter as well as converters with different types of non-idealities. Ideally the steady state gain was found to be independent of the switching frequency and load and dependent only on the switching duty ratio ($d = T_{on}/T_S$), in the continuous current mode of operation (CCM). In the discontinuous mode of operation (DCM), the voltage gain was found to be a function of switching frequency and the load as well through the conduction parameter ($K = 2L/RT_S$). The output voltage of a real converter will also depend on the non-idealities in the converter such as the switch voltage drops etc. As a result an SMPC operating with a fixed duty ratio (open loop control) will not be able to maintain the output voltage of the converter fixed. The disturbances that are encountered are changes in V_g, the switch voltage drops and their dependence on ambient conditions, parasitic elements in the converter, and drifts in the control circuit on account of ambient variations. Therefore it is essential that the SMPC be controlled in a closed loop with appropriate feedback to regulate the output voltage of the SMPC. In order to apply the theory of control and to design suitable closed loop controllers for the SMPC, it is essential that a dynamic model for different types of SMPC be developed [14, 15, 17, 29, 33]. The purpose of this chapter is to consider the SMPC as a system and develop an appropriate dynamic model for the converter.

5.2 Pulse Width Modulated Converter

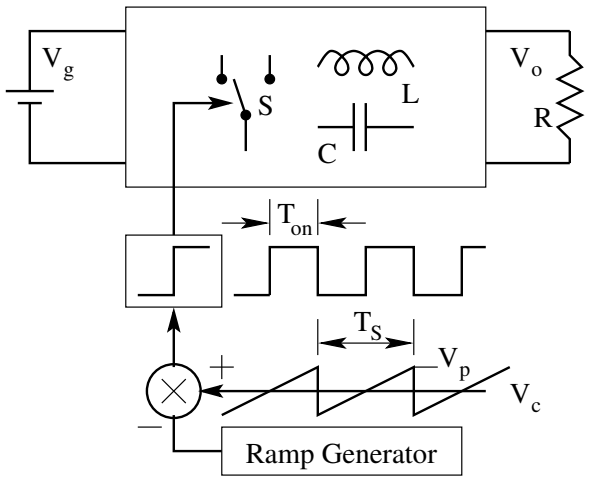

Figure 5.1: Duty Ratio Controlled dc to dc Converter

Figure 1 shows a typical pulse width modulated switched mode power converter consisting of a switch, an inductor, and a capacitor. Power is supplied to the converter at a dc voltage of V_g. The converter feeds power to the load (R) at a voltage of V_o. The switch is operated at a high switching frequency with a switching period T_S. The switch is kept ON during a fraction (dT_S) of the switching period. For the rest ($(1-d)T_S$) of the switching period, the switch is OFF. The generation of the switch control signal is by the popular ramp-control voltage comparison method. It may be verified that the switching duty ratio d is related to the control voltage V_c and the peak of the ramp voltage V_p as follows [21, 37].

$$d = \frac{V_c}{V_p} \tag{5.1}$$

The non-idealities in the converter may be identified as V_T (the ON state switch voltage drop), V_D (the OFF state switch voltage drop), R_c (parasitic resistance of the capacitor), and R_1 (parasitic resistance of the inductor). We may represent the black box model of the converter as shown in Fig. 2. The following model quantities may be identified.

- d - The duty ratio d is defined as the control input, since the output voltage control of the converter is through the control of the switch duty ratio.

- V_g - The power supply input is not under the control of the designer. Apart from the available dc level V_g, the source will also have superimposed ac input $\hat{v}_g(t)$. In a true dc-to-dc converter, the output voltage must

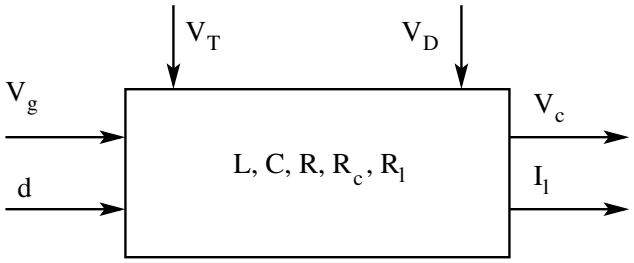

Figure 5.2: Block Diagram of the Switching Power Converter

not be influenced by either of these inputs. Therefore $\hat{v}_g(t)$ is defined as a disturbance input.

- V_T, V_D - Ideally the ON state switches drop zero voltage. In practice, there will be a small finite voltage drop across an ON state switch. This ON state drop in the switch depends on the type of switch employed, the type of drive provided for the switch and the ambient conditions. These drops are not under the control of the designer, and since their influence on the output voltage of the converter is undesirable, they are also defined as disturbance inputs.
- L, C - These are parameters of the converter. L and C are chosen for any converter based on the steady state requirements (switching frequency, current ripple, and voltage ripple). Usually L and C will be of fixed value. The value of L may be a function of the current if the effect of saturation is significant. In any design, manufacturing tolerances of $\pm 20\%$ may apply to these values. The load on the converter may be fixed or may vary considerably. It is not unusual to come across load variation in a converter as much as 5 % to 200 %.
- R_c, R_l - These are parasitic resistances of the reactive elements in the converter. Though they are small and close to zero, their dynamic effect on the converter performance may be more significant than their steady state effect.

5.2.1 Dynamic and Output Equations of the Converter

Figure 2 shows the black box model of the converter. The converter consists of linear circuit elements L, C, R as well as non-linear circuit elements, which are switches. The converter as such is not a linear system. However the circuit obtained in the converter for each of the switch options in the converter is a linear circuit. Therefore, it is possible to write the dynamic and output equations of the circuit for each of the switch positions.

What are dynamic equations? Each energy storage element (inductors and capacitors) is a dynamic element of the converter. A dynamic variable is

associated with each energy storage element of the converter. The inductor current is a dynamic variable and so also the capacitor voltage. There will be as many dynamic variables for the converter as there are energy storage elements in the converter. By dynamic equations of the converter is meant the equations, which relate the rate of change of dynamic variables, inputs and the parameters of the converter.

What are output equation? The equation relating the output(s) of the converter to the dynamic variables of the converter is the output equation of the converter. The first step in the dynamic modeling of the converter is to write down the dynamic and output equations of the converter for the circuits obtained in the converter for each of the switch positions in the converter. The following example illustrates the step of writing the dynamic equation of the converter.

5.3 An Idealized Example

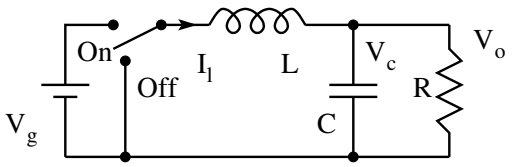

Figure 5.3: Idealised Buck Converter

Fig. 3 shows the buck converter operating in CCM. For the sake of simplicity, all elements are considered ideal. The power to the converter is supplied from the source at voltage Vg. The switch operates at high switching frequency with a switching period T_S. For a fraction (dT_S) of the switching period, the switch is in the ON state. Energy is then drawn from the source and the inductor charges up the increasing I_l. The output voltage is V_o. During the rest $[(1-d)T_S]$ of the switching period, the switch is in the OFF state. No energy is then drawn from the source. The inductor transfers part of its energy then to the load with decreasing i_l. There are two linear circuits obtained in the converter, one corresponding to each of the switch (ON & OFF) position. These two circuits are shown in Fig. 4a and 4b. The circuit in Fig. 4a is the equivalent circuit of the converter during the ON (dT_S) duration. The circuit in Fig. 4b is the equivalent circuit of the converter during the OFF $[(1-d)T_S]$ duration. The dynamic elements in the converter are L & C. The dynamic variables of the converter are i_1 and v_c. The dynamic equations relate the change of change of $[di_l/dt]$ and $[dv_c/dt]$ of the dynamic variables to the input (v_g), the parameters of the converter (L, R and C) and the dynamic variables (i_l and v_c) of the circuit. The output equations may be found by the algebraic relationship between the output of the circuit and the dynamic variables of

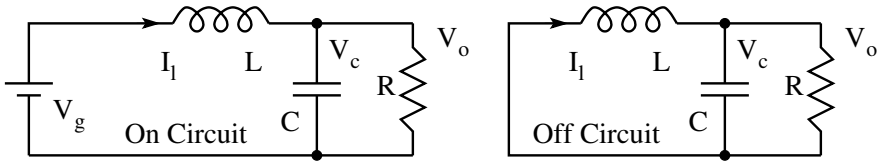

Figure 5.4: Equivalent Circuits of the Buck Converter

the circuit. They will be of the form

$$\frac{di_l}{dt} = f_1(i_l, v_c, v_g, L, R, C) \tag{5.2}$$

$$\frac{dv_c}{dt} = f_2(i_l, v_c, v_g, L, R, C) \tag{5.3}$$

$$v_o = g(i_l, v_c) \tag{5.4}$$

These equations may be obtained by applying the kirchoff's voltage and current (KVL & KCL) equations to the circuit. The dynamic and output equations of the circuit for the ON period are obtained as follows.

$$v_g = L\frac{di_l}{dt} + v_c \quad ; \quad \frac{di_l}{dt} = \frac{v_g}{L} - \frac{v_c}{L} \tag{5.5}$$

$$i_l = C\frac{dv_c}{dt} + \frac{v_c}{R} \quad ; \quad \frac{dv_c}{dt} = \frac{i_l}{C} - \frac{v_c}{RC} \tag{5.6}$$

$$v_o = v_c \tag{5.7}$$

The dynamic and output equations of the circuit for the OFF period are obtained as follows.

$$\frac{di_l}{dt} = -\frac{v_c}{L} \tag{5.8}$$

$$\frac{dv_c}{dt} = \frac{i_l}{C} - \frac{v_c}{RC} \tag{5.9}$$

$$v_o = v_c \tag{5.10}$$

It will be inconvenient to put these equations in the following form.
During ON time,

$$\dot{x} = A_1 x + b_1 v_g \tag{5.11}$$

$$v_o = q_1 x \tag{5.12}$$

During OFF time,

$$\dot{x} = A_2 x + b_2 v_g \tag{5.13}$$

$$v_o = q_2 x \tag{5.14}$$

where $\dot{x} = \begin{pmatrix} \frac{di_1}{dt} \\ \\ \frac{dv_c}{dt} \end{pmatrix}$; $A_1 = A_2 = \begin{pmatrix} 0 & -\frac{1}{L} \\ \\ \frac{1}{C} & -\frac{1}{RC} \end{pmatrix}$;

$b_1 = \begin{pmatrix} \frac{1}{L} \\ \\ 0 \end{pmatrix}$; $b_2 = \begin{pmatrix} 0 \\ \\ 0 \end{pmatrix}$; $q_1 = q_2 = [0 \quad 1]\, x$;

Equations [12] & [14] are referred to as the output equations. Equations [11] & [13] are referred to as the dynamic equations or the state equations of the converter for each of the sub-periods of the switching period.

5.4 A More Realistic Example

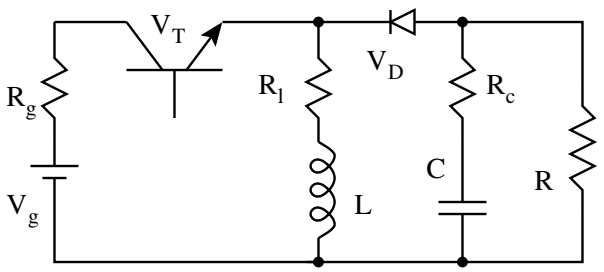

Figure 5.5: A Non-ideal Flyback Convereter

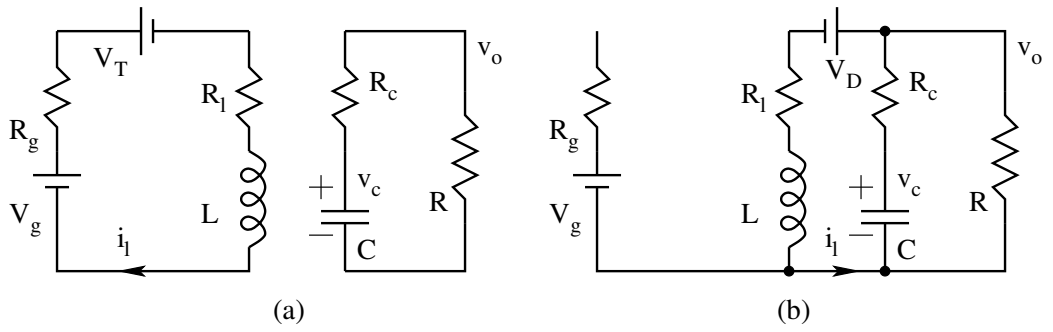

Figure 5.6: Equivalent Circuits of the Flyback Converter

We may now consider a more realistic example as shown in Fig. 5, for writing down the dynamic and output equations. Fig. 5 shows a non-isolated fly-back converter. The non-idealities considered are, the source resistance R_g, the active switch ON state drop V_T, the parasitic resistance of the inductor R_l, the passive switch ON state drop V_D, and the parasitic resistance of the

capacitor R_c. The equivalent circuit of the converter for the ON and OFF duration are as shown in Fig. 6a and 6b respectively.
The ON duration equations are

$$v_g = i_l(R_l + R_g) + V_T + L\frac{di_l}{dt} \tag{5.15}$$

$$i_c = C\frac{dv_c}{dt} = -\frac{R}{R + R_c} \tag{5.16}$$

$$v_o = v_c\frac{R}{R + R_c} \tag{5.17}$$

The OFF duration equations are

$$v_0 = i_l R_l + V_D + L\frac{di_l}{dt} \tag{5.18}$$

$$i_c = C\frac{dv_c}{dt} = -i_l - \frac{v_o}{R} \tag{5.19}$$

$$v_o = v_c\frac{R}{R + R_c} - i_l\frac{RR_c}{R + R_c} \tag{5.20}$$

Substituting for v_o from [Eqn. 20] into [Eqn. 18 & 19], we get

$$L\frac{di_l}{dt} = -V_D - i_l R_l - i_l\frac{RR_c}{R + R_c} + v_c\frac{R}{R + R_c} \tag{5.21}$$

$$C\frac{dv_c}{dt} = -i_l\frac{R}{R + R_c} - v_c\frac{R}{R + R_c} \tag{5.22}$$

We may write the dynamic equations of the converter as follows.
ON duration:

$$\frac{di_l}{dt} = \frac{v_g}{L} - \frac{R_g + R_l}{L}i_l - \frac{v_T}{L} \tag{5.23}$$

$$\frac{dv_c}{dt} = -\frac{v_c}{C(R + R_c)} \tag{5.24}$$

$$v_o = v_c\frac{R}{R + R_c} \tag{5.25}$$

OFF Duration:

$$\frac{di_l}{dt} = -\frac{v_D}{L} - \frac{i_l}{L}\left(R_l + \frac{RR_c}{R + R_c}\right) - v_c\frac{R}{L(R + R_c)} \tag{5.26}$$

$$\frac{dv_c}{dt} = -\frac{i_l}{C}\frac{R}{R + R_c} - \frac{v_c}{C(R + R_c)} \tag{5.27}$$

$$v_o = v_c\frac{R}{R + R_c} - i_l\frac{RR_c}{R + R_c} \tag{5.28}$$

The equations may be rearranged in the standard matrix form as follows.
ON Duration:

$$\dot{x} = A_1 x + b_1 v_g + e_1 v_T + n_1 v_D \tag{5.29}$$

$$v_o = q_1 x \tag{5.30}$$

OFF Duration:

$$\dot{x} = A_2 x + b_2 v_g + e_2 v_T + n_2 v_D \tag{5.31}$$

$$v_o = q_2 x \tag{5.32}$$

$$\dot{x} = \begin{pmatrix} \dfrac{di_1}{dt} \\ \\ \dfrac{dv_c}{dt} \end{pmatrix} ;\ R||R_c = \frac{RR_c}{R+R_c} ;$$

$$A_1 = \begin{bmatrix} -\dfrac{R_g + R_l}{L} & 0 \\ \\ 0 & -\dfrac{1}{C(R+R_c} \end{bmatrix} ;\ A_2 = \begin{bmatrix} -\dfrac{R_l + R||R_c}{L} & -\dfrac{R}{L(R+R_c)} \\ \\ \dfrac{R}{C(R+R_c)} & -\dfrac{1}{C(R+R_c} \end{bmatrix};$$

$$b_1 = \begin{bmatrix} \dfrac{1}{L} \\ \\ 0 \end{bmatrix} ;\ e_1 = \begin{bmatrix} -\dfrac{1}{L} \\ \\ 0 \end{bmatrix} ;\ n_1 = \begin{bmatrix} 0 \\ \\ 0 \end{bmatrix} ;\ q_1 = \begin{bmatrix} 0 & \dfrac{R}{R+R_c} \end{bmatrix} ;$$

$$b_2 = \begin{bmatrix} 0 \\ \\ 0 \end{bmatrix};\ e_2 = \begin{bmatrix} 0 \\ \\ 0 \end{bmatrix};\ n_2 = \begin{bmatrix} -\dfrac{1}{L} \\ \\ 0 \end{bmatrix};\ q_2 = \begin{bmatrix} -R||R_c & \dfrac{R}{R+R_c} \end{bmatrix} ;$$

In general the dynamic and output equations for any converter may be put in the form shown below for the ON and OFF duration.
ON Duration (during the time $kT_S \le t \le (k+d)T_S$)

$$\dot{x} = A_1 x + b_1 v_g + e_1 v_T + n_1 v_D \tag{5.33}$$

$$v_o = q_1 x \tag{5.34}$$

OFF Duration (during the time $(k+d)T_S \le t \le (k+1)T_S$)

$$\dot{x} = A_2 x + b_2 v_g + e_2 v_T + n_2 v_D \tag{5.35}$$

$$v_o = q_2 x \tag{5.36}$$

5.5 Averaged Model of the Converter

Equations [33] & [34] represent the converter during the ON duration. Eqn. [35] & [36] represents the converter during the OFF duration. The above representation is in the standard state space format for each of the intervals. The converter alternates between the two-switched states at high frequency. We

wish to represent the converter through a single equivalent dynamic representation, valid for both the ON and OFF durations. If we consider that the variation of the dynamic variables over a switching period, then

$$x = \dot{x}_{avg} T_S = \dot{x}_{dT_S} d T_S + \dot{x}_{(1-d)T_S} (1-d) T_S \tag{5.37}$$

where $\dot{x}_{avg}$ is the average rate of change of dynamic variables over a full switching period. The above equivalent description is valid if $\dot{x}_{dT_S}$ and $\dot{x}_{(1-d)T_S}$ are constant during the ON and OFF duration respectively. This will be valid assumption if the ON and OFF durations are much less compared to the natural time constants of the respective circuits. Then for the averaged dynamic variables,

$$\dot{x} = A\ x + b\ v_g + e\ v_T + n\ v_D \tag{5.38}$$

$$v_o = q\ x \tag{5.39}$$

$A = A_1\ d + A_2\ (1-d)$; $b = b_1\ d + b_2\ (1-d)$; $e = e_1\ d + e_2\ (1-d)$;
$n = n_1\ d + n_2\ (1-d)$; $q = q_1\ d + q_2\ (1-d)$;
Eqns [38] & [39] represents the equivalent dynamic and output equations of the converter. Since the averaging process has been done over a switching period, the equivalent model is valid for time durations much larger compared to the switching period (or valid for frequency variations much smaller than the switching frequency). As a thumb rule the equivalent model may be taken to be a good approximation of the real converter for a dynamic range of about a tenth of the switching frequency.

5.5.1 Steady State Solution

The steady state solution is obtained by equating the rate of change of dynamic variables to zero.

$$0 = A\ x + b\ v_g + e\ v_T + n\ v_D \tag{5.40}$$

$$X = A^{-1}\ (b\ v_g + e\ v_T + n\ v_D) \tag{5.41}$$

$$V_o = q\ A^{-1}\ (b\ v_g + e\ v_T + n\ v_D) \tag{5.42}$$

The following example illustrates the steady state solution of the boost con-

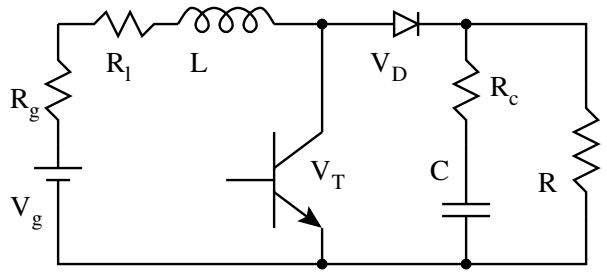

Figure 5.7: A Non-ideal Boost Converter

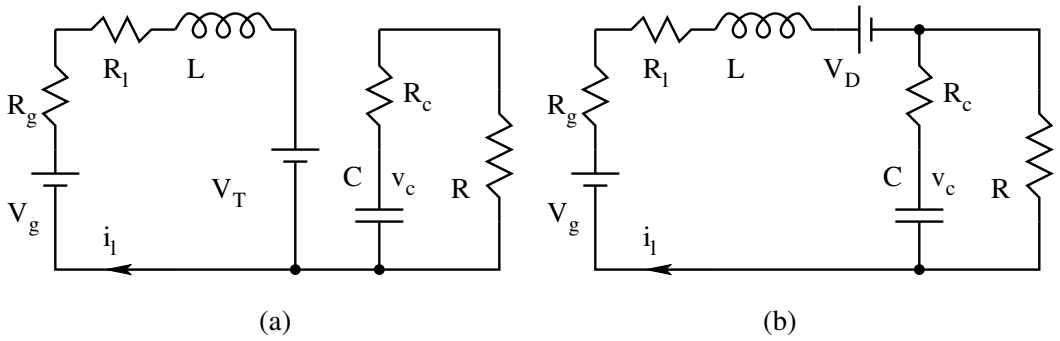

Figure 5.8: Equivalent Circuits of the Non-ideal Boost Converter

verter shown in Fig. 7. For the sake of simplicity, the converter is taken to be ideal. Fig 8a & 8b show the ON and OFF duration equivalent circuits obtained in the converter. It may be verified that the averaged model is

$$\dot{x} = A\ x + b\ v_g \tag{5.43}$$

$$v_o = q/x \tag{5.44}$$

$$\dot{x} = \begin{pmatrix} \frac{di_1}{dt} \\ \\ \frac{dv_c}{dt} \end{pmatrix};\ A = \begin{bmatrix} 0 & -\frac{1-D}{L} \\ \\ \frac{1-D}{C} & -\frac{1}{CR} \end{bmatrix};\ b = \begin{bmatrix} \frac{1}{L} \\ \\ 0 \end{bmatrix};\ q = [0 \quad 1];$$

The steady state solution is

$$X = -A^{-1}/b/V_g \tag{5.45}$$

$$V_o = q/X \tag{5.46}$$

$$A^{-1} = \frac{LC}{(1-D)^2} \begin{bmatrix} -\frac{1}{RC} & -\frac{1-D}{L} \\ \\ \frac{1-D}{C} & 0 \end{bmatrix};$$

$$\begin{pmatrix} I_l \\ \\ V_o \end{pmatrix} = \begin{bmatrix} \frac{V_g}{R(1-D)^2} \\ \\ \frac{V_g}{1-D} \end{bmatrix} \tag{5.47}$$

$$V_o = \frac{V_g}{(1-D)} \tag{5.48}$$

The ON and OFF durations models and the averaged model of the converter shown in Fig. 8, taking into account the non-idealities (R_l, R_c, V_T, V_D) are left

an exercise. The answers are given below for verification.

$$A_1 = \begin{bmatrix} -\dfrac{R_l}{L} & 0 \\ 0 & -\dfrac{a}{RC} \end{bmatrix} ; A_2 = \begin{bmatrix} -\dfrac{R_l + aR_c}{L} & -\dfrac{a}{L} \\ \dfrac{a}{C} & -\dfrac{a}{RC} \end{bmatrix};$$

$$b_1 = \begin{bmatrix} \dfrac{1}{L} \\ 0 \end{bmatrix} ; e_1 = \begin{bmatrix} -\dfrac{1}{L} \\ 0 \end{bmatrix} ; n_1 = \begin{bmatrix} 0 \\ 0 \end{bmatrix} ; q_1 = \begin{bmatrix} 0 & \dfrac{R}{R + R_c} \end{bmatrix} ; a = \frac{R}{R + R_c} ;$$

$$b_2 = \begin{bmatrix} \dfrac{1}{L} \\ 0 \end{bmatrix} ; e_2 = \begin{bmatrix} 0 \\ 0 \end{bmatrix}; n_2 = \begin{bmatrix} -\dfrac{1}{L} \\ 0 \end{bmatrix}; q_2 = [-aR_c \quad a] ;$$

$$A = \begin{bmatrix} -\dfrac{R_l + a(1-D)R_c}{L} & -\dfrac{a(1-D)}{L} \\ \dfrac{a(1-D)}{C} & -\dfrac{a}{RC} \end{bmatrix}; b = \begin{bmatrix} \dfrac{1}{L} \\ 0 \end{bmatrix} ;$$

$$e = \begin{bmatrix} -\dfrac{D}{L} \\ 0 \end{bmatrix} ; n = \begin{bmatrix} -\dfrac{1-D}{L} \\ 0 \end{bmatrix} ; q = [a(1-D)R_c \quad a] ;$$

The steady state solution is

$$I_l = \frac{V_g - DV_T - (1-D)V_D}{R\Big[\alpha + a(1-D)\beta + a(1-D)^2\Big]} ; \ \alpha = \frac{R_l}{R} \tag{5.49}$$

$$V_c = \frac{(1-D)(V_g - DV_T - (1-D)V_D)}{R\Big[\alpha + a(1-D)\beta + a(1-D)^2\Big]} ; \ \beta = \frac{R_c}{R} \tag{5.50}$$

$$V_o = \frac{(1-D)(V_g - DV_T - (1-D)V_D)}{R\Big[\alpha + a(1-D)\beta + a(1-D)^2\Big]} \tag{5.51}$$

5.5.2 Small Signal Model of The Converter

The steady state representation of the averaged system given by Eqn. [41] and [42] though linear is not time invariant. This is because the gain matrices A, b etc. are functions of time through d embedded within. Therefore it is necessary to linearise the system equations. Such a linearised model will enable us to define the different transfer functions for the converter and apply linear system theory to design closed loop controllers for the converters. We may neglect the terms containing V_T and V_D for this purpose. Such a step will be valid since these quantities are small (compared to V_g and V_o) and hence small variations in these small terms will only have a second order effect on the overall system. The dynamic equations are thus

$$\dot{x} = \Big[A_1\ d + A_2\ (1-d)\Big]\ x\ +\ \Big[b_1\ d + b_2\ (1-d)\Big]\ v_g \tag{5.52}$$

$$v_o = \Big[q_1\ d + q_2\ (1-d)\Big]\ x \tag{5.53}$$

We may now consider that the inputs d and v_g are varying around their quiescent operating points D and V_g respectively.

$d = D\ +\ \hat{d}\ ;\ \dfrac{\hat{d}}{D}\ <<\ 1\ ;\ v_g = V_g\ +\ \hat{v}_g\ ;\ \dfrac{\hat{v}_g}{V_g}\ <<\ 1\ ;$

These time varying inputs in d and v_g produce perturbations in the dynamic variables x $(X + \hat{x})$ and v_o $(V_o + \hat{v}_o)$.

$$\dot{X} + \dot{\hat{x}} = \Big[A_1 d + A_2(1-d)\Big](X + \hat{x}) + \Big[b_1 d + b_2(1-d)\Big]\Big(V_g + \hat{v}_g\Big) \tag{5.54}$$

$$V_o + \hat{v}_o = \Big[q_1\ d + q_2\ (1-d)\Big]\ (X + \hat{x}) \tag{5.55}$$

$$\hat{X} + \dot{\hat{x}} = \Big[A_1(D+\hat{d}) + A_2(1-D-\hat{d})\Big](X+\hat{x}) + \Big[b_1(D+\hat{d}) + b_2(1-D-\hat{d})\Big]\Big(V_g + \hat{v}_g\Big) \tag{5.56}$$

$$V_o + \hat{v}_o = \Big[q_1\ (D+\hat{d}) + q_2\ (1-D-\hat{d})\Big]\ (X + \hat{x}) \tag{5.57}$$

The above equations may be expanded and separated into dc (steady state) terms, linear small signal terms and non-linear terms. When the perturbations in d and V_g are small, the effect of the non-linear terms will be small on the overall response and hence may be neglected.

$$0 = A\ X\ +\ b\ V_g; \qquad DC Model \tag{5.58}$$

$$\dot{\hat{x}} = A\ \hat{x}\ +\ b\ \hat{v}_g\ +\ \Big[(A_1 - A_2)X\ +\ (b_1 - b_2)V_g\Big]\ \hat{d}; \quad Linear\ Model \tag{5.59}$$

The steady state solution (X) is obtained from Eqn. [58] and used in Eqn. [59] to get the following small signal dynamic model of the converter.

$$\dot{\hat{x}} = A\ \hat{x} + b\ \hat{v}_g\ +\ f\ \hat{d} \tag{5.60}$$

$$v_o = q\ \hat{x} +\ (q_1 - q_2)\ X\ \hat{d} \tag{5.61}$$

$A = A_1D + A_2(1-D)$; $b = b_1D + b_2(1-D)$; $q = q_1D + q_2(1-D)$;

$f = \left[\left(A_1 - A_2\right)X + \left(b_1 - b_2\right)V_g\right]$; $X = A^{-1}bV_g$;

5.5.3 Transfer Functions of the converter

From the above linear small signal model of the converter we may define the following transfer functions of the converter.
Input Transfer Functions ($\hat{d} = 0$)

$$\frac{\hat{x}(s)}{\hat{v}_g(s)} = (sI - A)^{-1}\ b \tag{5.62}$$

$$\frac{\hat{v}_o(s)}{\hat{v}_g(s)} = q\ (sI - A)^{-1}\ b \tag{5.63}$$

Control Transfer Functions ($\hat{v}_g = 0$)

$$\frac{\hat{x}(s)}{\hat{d}(s)} = (sI - A)^{-1}\ f \tag{5.64}$$

$$\frac{\hat{v}_o(s)}{\hat{d}(s)} = q\ (sI - A)^{-1}\ f \tag{5.65}$$

Nonidealities in the converter such as the winding resistance, ESR of the capacitors, switch drops etc. may be readily incorporated in this averaging method. The idealized transfer functions of the basic converters are given here.

Buck Converter:

$$\frac{\hat{i}(s)}{\hat{v}_g(s)} = \frac{D}{R}\frac{(1 + sCR)}{\left[1 + s\frac{L}{R} + s^2LC\right]} \tag{5.66}$$

$$\frac{\hat{i}(s)}{\hat{d}(s)} = \frac{V_g}{R}\frac{(1 + sCR)}{\left[1 + s\frac{L}{R} + s^2LC\right]} \tag{5.67}$$

$$\frac{\hat{v}_o(s)}{\hat{v}_g(s)} = D\frac{1}{\left[1 + s\frac{L}{R} + s^2LC\right]} \tag{5.68}$$

$$\frac{\hat{v}_o(s)}{\hat{d}(s)} = V_g\frac{1}{\left[1 + s\frac{L}{R} + s^2LC\right]} \tag{5.69}$$

Boost Converter:

$$\frac{\hat{i}(s)}{\hat{v}_g(s)} = \frac{1}{R(1-D)^2}\frac{(1+sCR)}{\left[1 + s\frac{L}{R(1-D)^2} + s^2\frac{LC}{(1-D)^2}\right]} \tag{5.70}$$

$$\frac{\hat{i}(s)}{\hat{d}(s)} = \frac{V_g}{R(1-D)^3}\frac{(2+sCR)}{\left[1 + s\frac{L}{R(1-D)^2} + s^2\frac{LC}{(1-D)^2}\right]} \tag{5.71}$$

$$\frac{\hat{v}_o(s)}{\hat{v}_g(s)} = \frac{1}{(1-D)}\frac{1}{\left[1 + s\frac{L}{R(1-D)^2} + s^2\frac{LC}{(1-D)^2}\right]} \tag{5.72}$$

$$\frac{\hat{v}_o(s)}{\hat{d}(s)} = \frac{V_g}{(1-D)^2}\frac{1 - s\frac{L}{R(1-D)^2}}{\left[1 + s\frac{L}{R(1-D)^2} + s^2\frac{LC}{(1-D)^2}\right]} \tag{5.73}$$

Buck- Boost Converter:

$$\frac{\hat{i}(s)}{\hat{v}_g(s)} = \frac{1}{R(1-D)^2}\frac{(1+sCR)}{\left[1 + s\frac{L}{R(1-D)^2} + s^2\frac{LC}{(1-D)^2}\right]} \tag{5.74}$$

$$\frac{\hat{i}(s)}{\hat{d}(s)} = \frac{V_g(1+D)}{R(1-D)^3}\frac{(1+sC\frac{R}{(1+D)})}{\left[1 + s\frac{L}{R(1-D)^2} + s^2\frac{LC}{(1-D)^2}\right]} \tag{5.75}$$

$$\frac{\hat{v}_o(s)}{\hat{v}_g(s)} = -\frac{D}{(1-D)}\frac{1}{\left[1 + s\frac{L}{R(1-D)^2} + s^2\frac{LC}{(1-D)^2}\right]} \tag{5.76}$$

$$\frac{\hat{v}_o(s)}{\hat{d}(s)} = -\frac{V_g}{(1-D)^2}\frac{1 - sD\frac{L}{R(1-D)^2}}{\left[1 + s\frac{L}{R(1-D)^2} + s^2\frac{LC}{(1-D)^2}\right]} \tag{5.77}$$

5.5.4 Example of a Boost Converter

One example of evaluating the transfer functions for the converter shown in Fig.1.7

ON Duration (Fig 1.8a)

$$v_g = L\frac{di}{dt} + iR_l + V_T \tag{5.78}$$

$$0 = C\frac{dv_c}{dt} + \frac{v_o}{R} \tag{5.79}$$

$$v_o = v_c\frac{R}{R+R_c}\ ; \qquad Define\ \frac{R}{R+R_c} = a \tag{5.80}$$

$$\begin{bmatrix} \frac{di}{dt} \\ \\ \frac{dv_c}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{R_l}{L} & 0 \\ \\ 0 & -\frac{a}{RC} \end{bmatrix} \begin{bmatrix} i \\ \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ \\ 0 \end{bmatrix} v_g + \begin{bmatrix} \frac{1}{L} \\ \\ 0 \end{bmatrix} v_T\ ;\ Note\ n_1 = 0 \tag{5.81}$$

$$= A_1x + b_1v_g + e_1v_T + n_1v_D \tag{5.82}$$

$$v_o = q_1x\ =\ \begin{bmatrix} 0 & a \end{bmatrix}\ x \tag{5.83}$$

OFF Duration (Fig.1.8a)

$$v_g = L\frac{di}{dt} + iR_l + V_D + v_o \tag{5.84}$$

$$i = C\frac{dv_c}{dt} + \frac{v_o}{R} \tag{5.85}$$

$$v_o = v_c\frac{R}{R+R_c} + i\frac{RR_c}{R+R_c} \tag{5.86}$$

$$\begin{bmatrix} \frac{di}{dt} \\ \\ \frac{dv_c}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{R_L + aR_c}{L} & -\frac{a}{L} \\ \\ \frac{a}{C} & -\frac{a}{RC} \end{bmatrix} \begin{bmatrix} i \\ \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ \\ 0 \end{bmatrix} v_g + \begin{bmatrix} \frac{1}{L} \\ \\ 0 \end{bmatrix} v_D\ ;\ Note\ e_2 = 0 \tag{5.87}$$

$$= A_2x + b_2v_g + e_2v_T + n_2v_D \tag{5.88}$$

$$v_o = q_2x\ =\ \begin{bmatrix} aR_c & a \end{bmatrix}\ x \tag{5.89}$$

Combining the above two subsystems, we get the averaged description.

$$= A\ x + b\ v_g + e\ v_T + n\ v_D \tag{5.90}$$

On modulation and separation of small signal terms we get the small signal model.

$$\dot{\hat{x}} = A\ \hat{x} + b\ \hat{v}_g\ +\ f\ \hat{d} \tag{5.91}$$

$$v_o = q\ \hat{x} +\ (q_1 - q_2)\ X\ \hat{d} \tag{5.92}$$

$A = A_1 D + A_2(1-D)$; $b = b_1 D + b_2(1-D)$; $q = q_1 D + q_2(1-D)$;

$f = \left[\left(A_1 - A_2\right)X + \left(b_1 - b_2\right)V_g\right]$; $X = A^{-1} b V_g$;

Steady State Solution

$$X\ =\ -A^{-1}\left[b\ v_g + e\ v_T + n\ v_D\right] \quad Define: \frac{R_l}{R} = \alpha/; \quad \frac{R_c}{R} = \beta \tag{5.93}$$

$$A^{-1} = \frac{LC}{D_o}\begin{bmatrix} -\dfrac{a}{RC} & \dfrac{(1-D)a}{C} \\ -\dfrac{(1-D)a}{L} & -\dfrac{R_L + a(1-D)R_c}{L} \end{bmatrix}$$

$D_o = a\alpha + (1-D)a^2\beta + a^2(1-D)^2$

$$I = \frac{V_g - DV_T - (1-D)V_D}{RD_o}\ ;\ V_c = \frac{(1-D)(V_g - DV_T - (1-D)V_D)}{D_o}$$

Small signal Transfer Functions

Define $D_s = 1 + \dfrac{s(CR_l + (1-D)aCR_c + aL/R)}{D_o} + \dfrac{s^2 LC}{D_o}$

$$\frac{\hat{v}_o(s)}{\hat{v}_g(s)} = q\ (sI - A)^{-1} b = \frac{V_g(1-D)}{D_o}\frac{(1+sCR_c)}{D_s} \tag{5.94}$$

$$\frac{\hat{v}_o(s)}{\hat{d}(s)} = q\ (sI - A)^{-1} f + (q_1 - q_2)X = \frac{V_g(1-D)}{D_o^2}\frac{(K_2 - sL/R)(1+sCR_c)}{D_s} \tag{5.95}$$

$K_2 = (1-D) - \alpha D(1-D) - \alpha(1-D)\alpha\beta$

The above expressions may be evaluated for the following component values and operating parameters. $V_g = 15V$; $R_l = 1\ \Omega$; $R_c = 0.5\ \Omega$; $D = 0.3$; $f_s = 20\ kHz$; $R = 100\ \Omega$; $L = 2\ mH$; $C = 150\ \mu F$; For the above boost converter at D = 0.3, the ideal and actual transfer functions are as follows.

Ideal Transfer Function

$$\frac{\hat{v}_o(s)}{\hat{d}(s)} = \frac{K\left(1 - \frac{s}{\omega_z}\right)}{\left(1 + \frac{s}{Q\omega_o} + \frac{s^2}{\omega_o^2}\right)} \tag{5.96}$$

The gain Magnitude and Phase plots of the control transfer functions for the

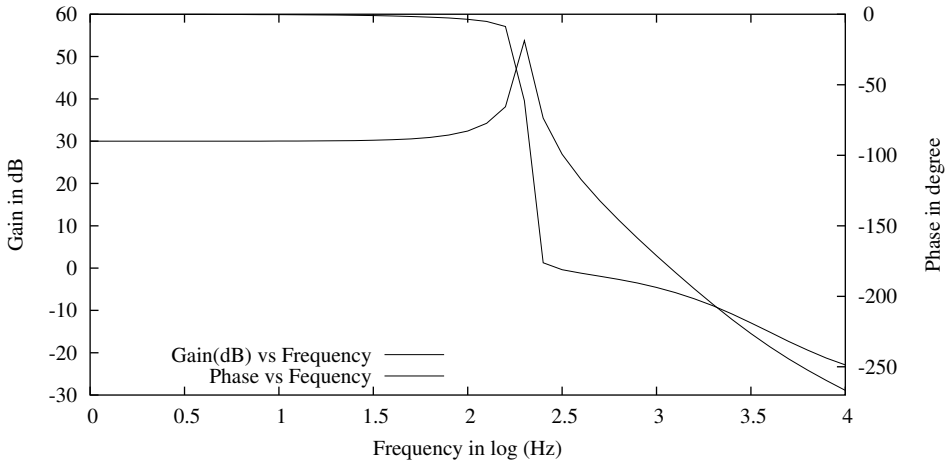

Figure 5.9: Control Gain and Phase of the Non-ideal Boost Converter

ideal and non-ideal converters are shown in Fig. 9. The important points to notice are

1. The ideal and actual complex pole pair is nearly constant.

2. The ideal and actual RHP zero is nearly same.

3. The actual Q of the complex pole pair varies widely from that of the ideal Q.

4. The zero caused by the ESR of the capacitor is important at higher frequencies. This zero is given by $\omega_d = 1/CR_c$.

5. The phase of the actual gain is less than that of the ideal gain. This is on account of the change in Q at lower end, and the presence of the ESR at higher end of frequencies.

6. The ideal gain predicts instability when unity gain feedback is employed, whereas the actual gain predicts stability (though with low stability margins). This is in general true (less losses, closer to instability).

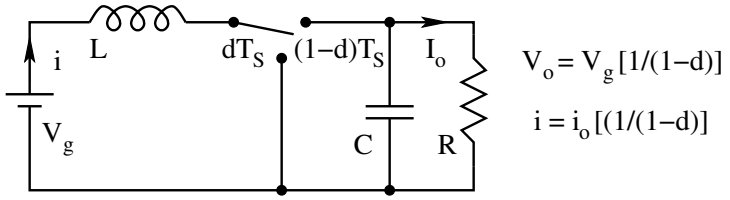

Figure 5.10: Boost Switching Converter

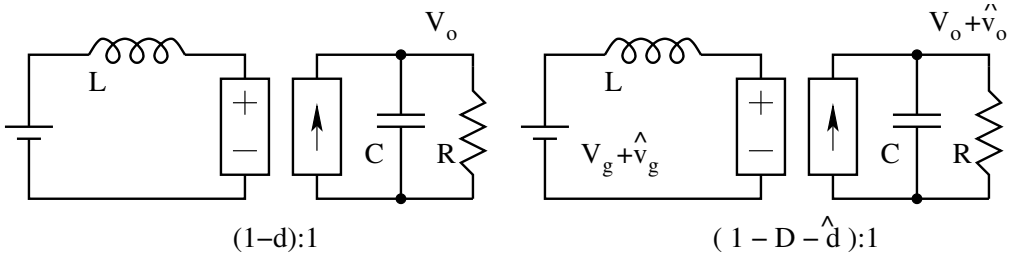

Figure 5.11: Equivalent Circuits of the Boost Converter

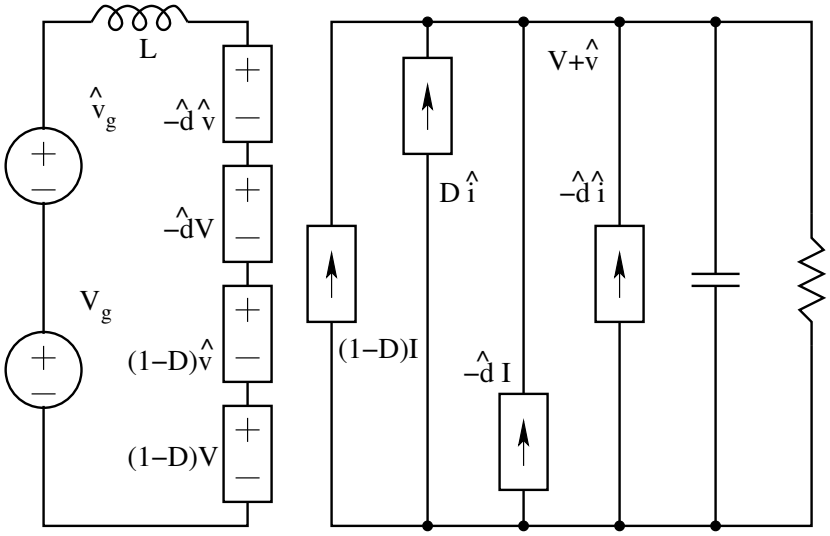

Figure 5.12: Composite Equivalent Circuit of the Boost Converter

5.6 Circuit Averaged Model of the Converters

There is another method of obtaining the small signal model and the transfer function of the converters. Consider the boost converter shown in Fig. 10. The equivalent circuit shown in Fig. 11 may represent the averaged model of the converter. On perturbation, the dynamic equivalent circuit is as shown in Fig. 12. This equivalent circuit may be transformed further as shown in

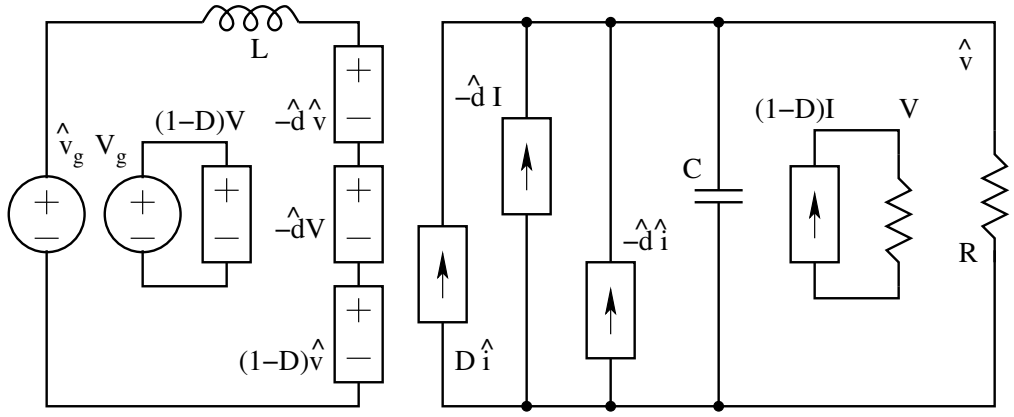

Figure 5.13: DC, Linear & Nonlinear Equivalent Circuits

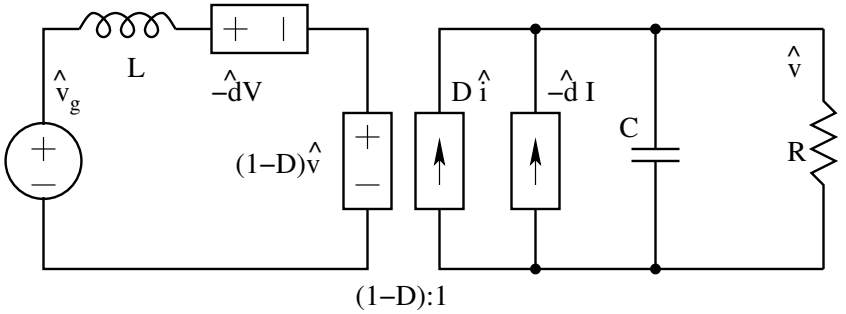

Figure 5.14: Linear Small Signal Equivalent Circuit

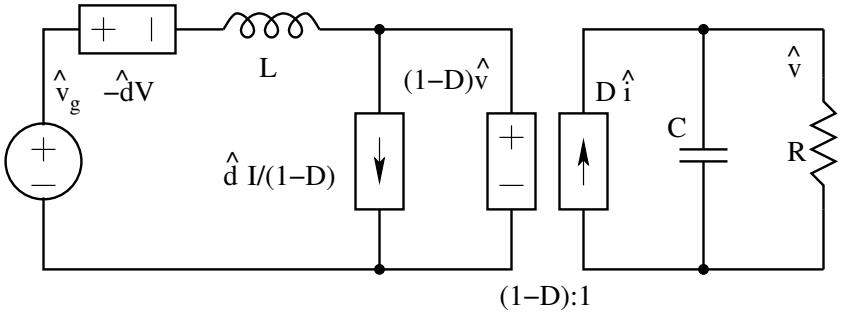

Figure 5.15: Linear Small Signal Equivalent Circuit

Fig. 12. The steady state and the transient terms may be separated as shown in Fig. 13. Notice the nonlinear terms in the model. The linear small signal model may be obtained by neglecting the nonlinear and the dc terms. Such a simplified model is shown in Fig. 14. This model may be transformed through the stages shown in Fig. 15 through Fig. 18. The canonical circuit

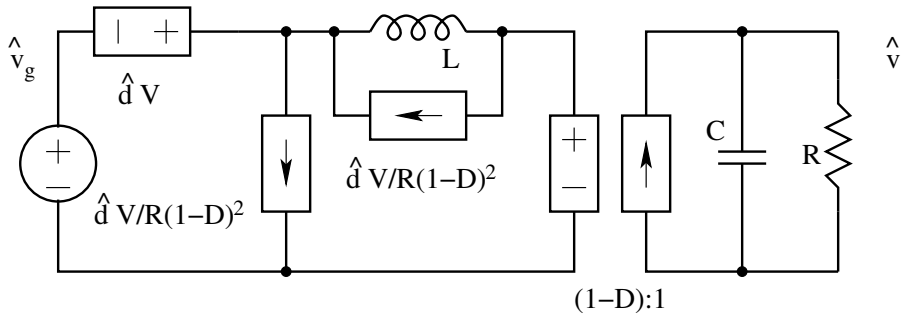

Figure 5.16: Linear Small Signal Equivalent Circuit

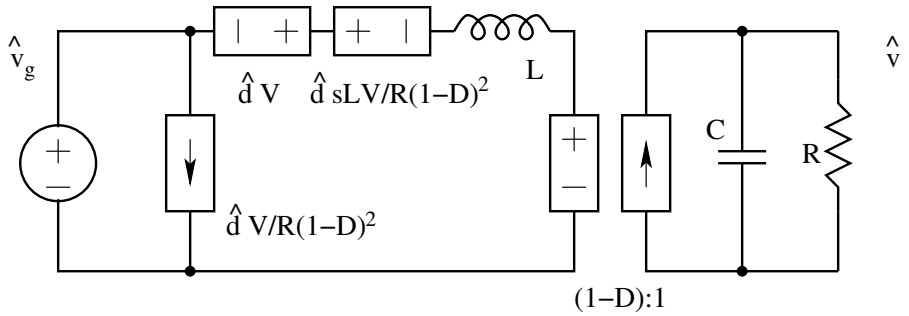

Figure 5.17: Linear Small Signal Equivalent Circuit

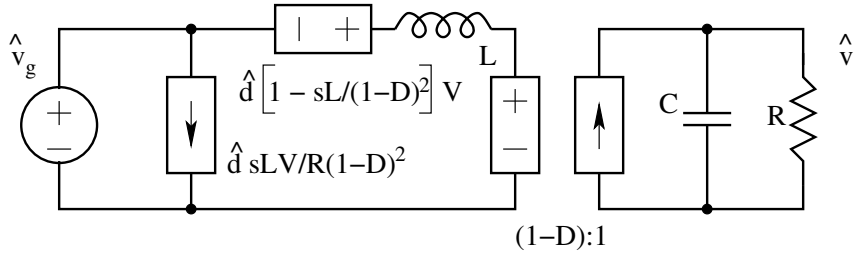

Figure 5.18: Linear Small Signal Equivalent Circuit

is then obtained by keeping all the independent and dependent on one side and reflecting all the passive elements to the load end as shown in Fig. 19. After averaging, the small signal ac dynamic model to the converter may be expressed through the canonical model given in Fig. 20.

$$u(s) = \left(1 - \frac{sL}{R(1-D)^2}\right) \tag{5.97}$$

$$J(s) = \left(\frac{V}{R(1-D)^2}\right) \tag{5.98}$$

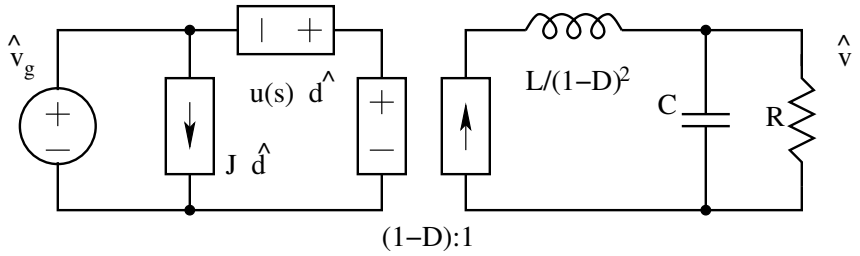

Figure 5.19: Canonical Model of the Switching Converter

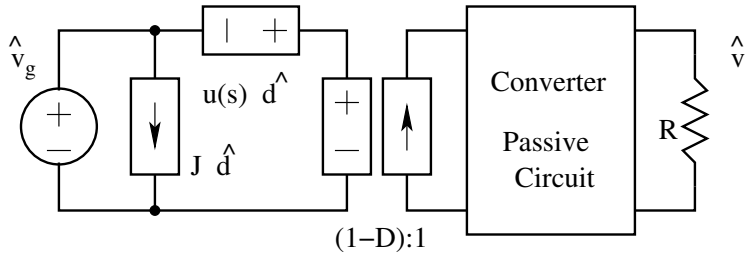

Figure 5.20: Canonical Model of the Switching Converter

5.7 Generalised State Space Model of the Converter

In the previous chapter we had seen the basis for the state space averaging method. It was possible through this method to obtain the small signal linear equivalent model for the converter. From the small signal linear model it was possible to obtain the input and control transfer functions of the converter. In many applications it will also be necessary to know the input and output impedances of the converter. These functions are required to assess the performance of the converter in a slightly different way with certain extra synthetic inputs. Such a model of the converter is referred to as the generalized model of the converter.

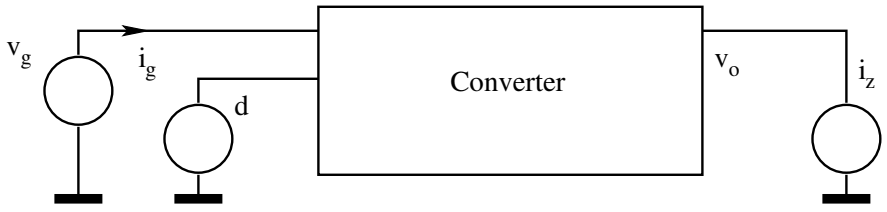

Figure 5.21: Canonical Model of the Switching Converter

5.7.1 Generalised Model

The generalised model is set up with three external inputs to the converter as shown in Fig. 21 The various input quantities are

$\hat{v}_g$: Source Modulation
$\hat{d}$: Control Duty Ratio Modulation
$\hat{i}_z$: Output Current Modulation

The out put quantities of interest are

$\hat{v}_o$: Output Voltage Variation
$\hat{i}_g$: Source Current Variation

From this setup we can selectively pair a set of input & ouput quantities to obtain the following functions of interest.

$$Z_{in} = \frac{\hat{v}_g(s)}{\hat{i}_g(s)} \ \left(\hat{d}(s) = 0; \hat{i}_z = 0;\right) : \text{Input Impedance}$$

$$Z_o = \frac{\hat{v}_o(s)}{\hat{i}_z(s)} \ \left(\hat{d}(s) = 0; \hat{v}_g = 0;\right) : \text{Output Impedance}$$

$$F = \frac{\hat{v}_o(s)}{\hat{v}_g(s)} \ \left(\hat{d}(s) = 0; \hat{i}_z = 0;\right) : \text{Audio Susceptibility}$$

$$G_v = \frac{\hat{v}_o(s)}{\hat{d}(s)} \ \left(\hat{v}_g(s) = 0; \hat{i}_z = 0;\right) : \text{Control Voltage Gain}$$

$$G_i = \frac{\hat{i}_g(s)}{\hat{d}(s)} \ \left(\hat{v}_g(s) = 0; \hat{i}_z = 0;\right) : \text{Control Current Gain}$$

The mathematical model of the general setup with all the three inputs is

$$\dot{x} \ = \ A\ x \ + \ b\ v_g \ + \ m\ i_z \tag{5.99}$$

$$v_o \ = \ q\ x \ + \ k\ i_z \tag{5.100}$$

$$i_g \ = \ p\ x \tag{5.101}$$

x = State Vector; v_g = Source Voltage;
d = duty Ratio; i_z = External Current Input;
v_o = Output Voltage; i_g = Input Current;

We may carry out the averaging process as explained in the previous chapter and obtain the following averaged matrices, perturbed variables, and small signal model respectively.

Averaged Matrices

$$A \ = \ A_1\ D \ + \ A_2\ (1-D)\ ; \qquad b \ = \ b_1\ D \ + \ b_2\ (1-D)\ ;$$
$$m \ = \ m_1\ D \ + \ m_2\ (1-D)\ ; \qquad k \ = \ k_1\ D \ + \ k_2\ (1-D)\ ;$$
$$q \ = \ q_1\ D \ + \ q_2\ (1-D)\ ; \qquad p \ = \ p_1\ D \ + \ p_2\ (1-D)\ ;$$

Perturbed Variables

$$x \ = \ X \ + \ \hat{x}\ ; \qquad v_o \ = \ V_o \ + \ \hat{v}_o\ ;$$
$$i_g \ = \ I_g \ + \ \hat{i}_g\ ; \qquad v_g \ = \ V_g \ + \ \hat{v}_g\ ;$$

$$d \;=\; D \;+\; \hat{d}\;; \qquad\qquad i_z \;=\hat{i}_z\;;$$

5.7.2 Linear Small signal Model

$$\begin{aligned}
\dot{x} &= A\,\hat{x} \;+\; b\,v_g \;+\; f\,\hat{d} \;+\; m\,\hat{i}_z\;;\\
f &= (A_1 \;-A_2)\;X \;+\; (b_1 \;-\; b_2\;)\;V_g\;;\\
\hat{v}_o &= (q_1 \;-q_2)\;X\;\hat{d} \;+\; q\,\hat{x} \;+\; k\,\hat{i}_z\;;\\
\hat{i}_g &= (p_1 \;-p_2)\;X\;\hat{d} \;+\; p\,\hat{x}\;;
\end{aligned}$$

With the above set up the dynamic performance functions of the converter may be defined in a convenient mathematical form.

5.7.3 Dynamic functions of the Converter

Audio Susceptibility:

$$F = \frac{\hat{v}_o(s)}{\hat{v}_g(s)}\left\{\hat{d}=0;\hat{i}_z=0;\right\}$$

The audio susceptibility of the converter quantifies the amount of input variations that will reach the output as a function of frequency.

$$\begin{aligned}
\dot{\hat{x}} &= A\,\hat{x} \;+\; b\,\hat{v}_g\\
\hat{x} &= (sI-A)^{-1}\,b\,\hat{v}_g\\
\hat{v} &= q\,\hat{x}
\end{aligned}$$

$$F = q\;(sI-A)^{-1}\;b \tag{5.102}$$

Input Admittance:

$$Y_{in} = \frac{\hat{i}_g(s)}{\hat{v}_g(s)}\left\{\hat{d}=0;\hat{i}_z=0;\right\}$$

Input Admittance of the converter relates as to how the converter interfaces with the load.

$$\begin{aligned}
\dot{\hat{x}} &= A\,\hat{x} \;+\; b\,\hat{v}_g\\
\hat{x} &= (sI-A)^{-1}\,b\,\hat{v}_g\\
\hat{i}_g &= p\,\hat{x}\\
\hat{i}_g &= p\;(sI-A)^{-1}\;b
\end{aligned}$$

$$Y_{in} = p\;(sI-A)^{-1}\;b \tag{5.103}$$

Output Impedance:

$$Z_o = \frac{\hat{v}_o(s)}{\hat{i}_z(s)}\left\{\hat{d}=0;\hat{v}_g=0;\right\}$$

The output impedance relates to the capacity of the converter to cater to dynamic loads.

$$\dot{\hat{x}} \;=\; A\,\hat{x} \;+\; m\,\hat{i}_z$$

$$\begin{aligned}\hat{x} &= (sI - A)^{-1}\, m\, \hat{i}_z \\ \hat{v}_o &= q\, \hat{x} + k\, \hat{i}_z \\ Z_o &= q\, (sI - A)^{-1}\, m + k \end{aligned} \tag{5.104}$$

Control Gain Functions:

$$G_v = \frac{\hat{v}_o(s)}{\hat{d}(s)} \left\{ \hat{i}_z = 0; \hat{v}_g = 0; \right\}$$

$$G_i = \frac{\hat{i}_g(s)}{\hat{d}(s)} \left\{ \hat{i}_z = 0; \hat{v}_g = 0; \right\}$$

The control transfer function relates to the gain between the control duty ratio and the output variable.

$$\begin{aligned}\dot{\hat{x}} &= A\, \hat{x} + f\, \hat{d} \\ \hat{x} &= (sI - A)^{-1}\, f\, \hat{d} \\ \hat{v}_o &= q\, \hat{x} + (q_1 - q_2)\, X\, \hat{d} \\ \hat{v}_o &= (q_1 - q_2)\, X\, \hat{d} + q\, (sI - A)^{-1}\, f\, \hat{d} \\ \hat{i}_g &= p\, \hat{x} + (p_1 - p_2)\, X\, \hat{d} \\ \hat{i}_g &= (p_1 - p_2)\, X\, \hat{d} + p\, (sI - A)^{-1}\, f\, \hat{d} \end{aligned}$$

$$G_v = (q_1 - q_2)\, X + q\, (sI - A)^{-1}\, f \tag{5.105}$$

$$G_i = (p_1 - p_2)\, X + p\, (sI - A)^{-1}\, f \tag{5.106}$$

5.7.4 Circuit Averaged Model Quantities

With reference to Fig. 20, let the inputs be simultaneously adjusted such that the output voltage is zero. Under such a condition, $u(s)\, \hat{d} = -\hat{v}_g$

$$\begin{aligned}&\dot{\hat{x}} = A\, \hat{x} + b\, \hat{v}_g + f\, \hat{d}\,; \\ &\hat{x} = (sI - A)^{-1}\, b\, \hat{v}_g + (sI - A)^{-1}\, f\, \hat{d}\,; \\ &\hat{v}_o = q\, \hat{x} + (q_1 - q_2)\, X\, \hat{d} = 0\,; \\ &q\, (sI - A)^{-1}\, b + q\, (sI - A)^{-1}\, f\, \hat{d} + (q_1 - q_2)\, X\, \hat{d} = 0\,; \\ &F\, \hat{v}_g + G_v\, \hat{d} = 0\,; \end{aligned}$$

$$u(s) = \frac{G_v}{F} \tag{5.107}$$

$$\begin{aligned}&\hat{i}_g = p\, \hat{x} + (p_1 - p_2)\, X\, \hat{d}\,; \\ &\hat{i}_g = (p_1 - p_2)\, X\, \hat{d} + p\, (sI - A)^{-1}\, f\, \hat{d} + p\, (sI - A)^{-1}\, b\, \hat{v}_g\,; \\ &J\, \hat{d} = G_i\, \hat{d} + Y_{in}\, \hat{v}_g\,; \\ &J = G_i + Y_{in}\, \frac{\hat{v}_g}{\hat{d}}\,; \\ &J = G_i - Y_{in}\, u(s)\,; \end{aligned}$$

$$J = G_i - Y_{in}\, \frac{G_v}{F} \tag{5.108}$$

5.8 Some Examples

In the following sections, the system representation of the basic converters is given in the form of the various matrices in the standard representation. The dynamic performance indices (all the transfer functions) of the converters as well as the circuit averaged model (duty cycle dependent current and voltage sources - $u(s)$ and J) quantities are given.

5.8.1 Buck Converter:

$$A_1 \;=\; A_2 \;=\; A \begin{pmatrix} 0 & -\dfrac{1}{L} \\ \dfrac{1}{C} & -\dfrac{1}{RC} \end{pmatrix};$$

$$b_1 \;=\; \begin{pmatrix} \dfrac{1}{L} \\ 0 \end{pmatrix}; b_2 \;=\; \begin{pmatrix} 0 \\ 0 \end{pmatrix}; b \;=\; \begin{pmatrix} \dfrac{D}{L} \\ 0 \end{pmatrix};$$

$$q_1 \;=\; q_2 \;=\; q \;=\; \begin{pmatrix} 0 & 1 \end{pmatrix};$$

$$m_1 \;=\; m_2 \;=\; m \;=\; \begin{pmatrix} 0 \\ \dfrac{1}{C} \end{pmatrix};$$

$$p_1 \;=\; \begin{pmatrix} 1 & 0 \end{pmatrix}; p_2 \;=\; \begin{pmatrix} 0 & 0 \end{pmatrix}; p \;=\; \begin{pmatrix} D & 0 \end{pmatrix};$$

$$k_1 \;=\; k_2 \;=\; k \;=0\,;$$

Define: $\quad D_s \;=\; 1 \;+\; s\dfrac{L}{R} \;+\; s^2LC\,;$

$$(sI - A)^{-1} \;=\; \frac{LC}{D_s} \begin{pmatrix} s + \dfrac{1}{RC} & -\dfrac{1}{L} \\ \dfrac{1}{C} & s \end{pmatrix};$$

Audio Susceptibility:

$$F = q\,(sI - A)^{-1}\,b \;=\; \frac{D}{D_s} \tag{5.109}$$

Input Admittance:

$$Y_{in} = p\,(sI - A)^{-1}\,b \;=\; \frac{D^2}{R}\frac{1 + sCR}{D_s} \tag{5.110}$$

Output Impedance:

$$Z_o = q\,(sI - A)^{-1}\,m \;=\; \frac{sL}{D_s} \tag{5.111}$$

Control Gain:

$$G_v = q\,(sI - A)^{-1}\,f \;+\; (q_1 - q_2)\;X \;=\; \frac{V_g}{D_s} \tag{5.112}$$

$$G_i = p\,(sI - A)^{-1}\,f \;+\; (p_1 - p_2)\;X \;=\; \frac{DV_g}{R}\frac{DV_g(1+sCR)}{RD_s} \tag{5.113}$$

Circuit Averaged Parameters:

$$u(s) = \;\frac{V_g}{D} \tag{5.114}$$

$$J = \;\frac{DV_g}{R} \tag{5.115}$$

5.8.2 Boost Converter

$$A_1 \;=\; \begin{pmatrix} 0 & 0 \\ 0 & -\dfrac{1}{RC} \end{pmatrix};\; A_2 \;=\; \begin{pmatrix} 0 & -\dfrac{1}{L} \\ \dfrac{1}{C} & -\dfrac{1}{RC} \end{pmatrix};$$

$$A \;=\; \begin{pmatrix} 0 & -\dfrac{(1-D)}{L} \\ \dfrac{(1-D)}{C} & -\dfrac{1}{RC} \end{pmatrix};$$

$$b_1 \;=\; b_2 \;=\; b \;=\; \begin{pmatrix} \dfrac{1}{L} \\ 0 \end{pmatrix};$$

$$m_1 \;=\; m_2 \;=\; m \;=\; \begin{pmatrix} 0 \\ \dfrac{1}{C} \end{pmatrix};$$

$$k_1 \;=\; k_2 \;=\; k \;=0\,;$$
$$p_1 \;=\; p_2 \;=\; p \;=\; \begin{pmatrix} 0 & 1 \end{pmatrix};$$
$$q_1 \;=\; q_2 \;=\; q \;=\; \begin{pmatrix} 0 & 1 \end{pmatrix};$$

$$f \;=\; \begin{pmatrix} \dfrac{V_g}{(1-D)L} \\ -\dfrac{V_g}{RC(1-D)^2} \end{pmatrix};$$

Define: $$D_s \;=\; 1 \;+\; s\frac{L}{R(1-D)^2} \;+\; s^2\frac{LC}{(1-D)^2}\;;$$

$$(sI-A)^{-1} \;=\; \frac{LC}{(1-D)^2 D_s}\begin{pmatrix} s+\dfrac{1}{RC} & -\dfrac{(1-D)}{L} \\ \dfrac{(1-D)}{C} & s \end{pmatrix};$$

Audio Susceptibility:

$$F = q\,(sI-A)^{-1}\,b \;=\; \frac{1}{(1-D)D_s} \tag{5.116}$$

Input Admittance:

$$Y_{in} = p\,(sI-A)^{-1}\,b \;=\; \frac{1}{R(1-D)^2}\frac{1+sCR}{D_s} \tag{5.117}$$

Output Impedance:

$$Z_o = q\,(sI-A)^{-1}\,m \;=\; \frac{sL}{(1-D)^2 D_s} \tag{5.118}$$

Control Gain:

$$G_v = q\,(sI-A)^{-1}\,f \;+\; (q_1-q_2)\;X \;=\; \frac{V_g}{(1-D)^2}\frac{1-\dfrac{sL}{R(1-D)^2}}{D_s} \tag{5.119}$$

$$G_i = p\,(sI-A)^{-1}\,f \;+\; (p_1-p_2)\;X \;=\; \frac{V_g}{R}\;\frac{(2+sCR)}{(1-D)^3 D_s} \tag{5.120}$$

Circuit Averaged Parameters:

$$u(s) = \;\frac{V_g}{D}\left(1-\frac{sL}{R(1-D)^2}\right) \tag{5.121}$$

$$J = \;\frac{V_g}{R(1-D)^3} \tag{5.122}$$

5.8.3 Buck-Boost Converter

$$A_1 = \begin{pmatrix} 0 & 0 \\ 0 & -\frac{1}{RC} \end{pmatrix}; A_2 = \begin{pmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{pmatrix};$$

$$A = \begin{pmatrix} 0 & -\frac{(1-D)}{L} \\ \frac{(1-D)}{C} & -\frac{1}{RC} \end{pmatrix};$$

$$b_1 = \begin{pmatrix} \frac{1}{L} \\ 0 \end{pmatrix}; b_2 = \begin{pmatrix} 0 \\ 0 \end{pmatrix}; b = \begin{pmatrix} \frac{D}{L} \\ 0 \end{pmatrix};$$

$$m_1 = m_2 = m = \begin{pmatrix} 0 \\ \frac{1}{C} \end{pmatrix};$$

$$k_1 = k_2 = k = 0;$$

$$p_1 = \begin{pmatrix} 1 & 0 \end{pmatrix}; p_2 = \begin{pmatrix} 0 & 0 \end{pmatrix}; p = \begin{pmatrix} D & 0 \end{pmatrix};$$

$$q_1 = q_2 = q = \begin{pmatrix} 0 & 1 \end{pmatrix};$$

$$f = \begin{pmatrix} \frac{DV_g}{(1-D)L} \\ -\frac{V_g}{RC(1-D)^2} \end{pmatrix};$$

Define: $D_s = 1 + s\frac{L}{R(1-D)^2} + s^2\frac{LC}{(1-D)^2};$

$$(sI - A)^{-1} = \frac{LC}{(1-D)^2 D_s} \begin{pmatrix} s + \frac{1}{RC} & -\frac{(1-D)}{L} \\ \frac{(1-D)}{C} & s \end{pmatrix};$$

Audio Susceptibility:

$$F = q\,(sI - A)^{-1}\,b = \frac{1}{(1-D)D_s} \tag{5.123}$$

Input Admittance:

$$Y_{in} = p\,(sI - A)^{-1}\,b \;=\; \frac{D^2}{R(1-D)^2}\frac{1+sCR}{D_s} \tag{5.124}$$

Output Impedance:

$$Z_o = q\,(sI - A)^{-1}\,m \;=\; \frac{sL}{(1-D)^2 D_s} \tag{5.125}$$

Control Gain:

$$G_v = q\,(sI - A)^{-1}\,f \;+\; (q_1 - q_2)\;X \;=\; \frac{V_g}{(1-D)^2}\frac{1-\dfrac{sL}{R(1-D)^2}}{D_s} \tag{5.126}$$

$$G_i = p\,(sI - A)^{-1}\,f + (p_1 - p_2)\;X \;=\; \frac{DV_g}{R(1-D)^2} + \frac{(1+D+sCR)}{R(1-D)^3 D_s} \tag{5.127}$$

Circuit Averaged Parameters:

$$u(s) = \;\frac{V_g}{(1-D)^2}\left(1 - \frac{sLD}{R(1-D)^2}\right) \tag{5.128}$$

$$J = \;\frac{DV_g}{R(1-D)^3} \tag{5.129}$$

5.9 Dynamic Model of Converters Operating in DCM

In the previous chapters we had seen the method of state space averaging applied to the switched mode converters operating in CCM. In Chapter 4, we had seen that the switched mode converters might operate under another operating mode defined as the discontinuous inductor current mode (DCM) of operation. For converters operating under DCM too, the method of state space averaging may be extended. The following section explains the method.

5.9.1 Dynamic Model

In the DCM operating mode, the converter operates with three different sub-circuits in each switching period. These three intervals are

dT_s : Active switch of the converter ON.
d_2T_s : Passive switch of the converter ON.
$(1 - d - d_2T_s$: None of the switches in the converter is ON.

The circuit equations of the converter in state space format is then given by
Interval dT_s:

$$(\dot{x}) \;=\; A_1\;x \;+\; b_1\;v_g \tag{5.130}$$

Interval d_2T_s:

$$(\dot{x}) \;=\; A_2\; x \;+\; b_2\; v_g \tag{5.131}$$

Interval $(1 - d_1 - d_2)T_s$:

$$(\dot{x}) \;=\; A_1\; x \;+\; b_1\; v_g \tag{5.132}$$

On averaging and linearising (under small signal), we get

$$\left(\dot{\hat{x}}\right) \;=\; A\; x \;+\; b\; v_g \;+\; f\; \hat{d} \;+\; g\; \hat{d}_2 \tag{5.133}$$

$$A \;=\; (A_1 - A_3)D \;+ (A_2 - A_3)D_2 \;+\; A_3 \;;$$

$$b \;=\; (b_1 - b_3)D \;+ (b_2 - b_3)D_2 \;+\; b_3 \;;$$

$$f \;=\; (A_1 - A_3)X \;+ (b_1 - b_3)V_g \;;$$

$$g \;=\; (A_2 - A_3)X \;+ (b_2 - b_3)V_g \;;$$

$$\left(\dot{\hat{x}}\right) \;=\; f_1 \;\left(\hat{x}, \hat{v}_g, \hat{d}, \hat{d}_2\right) \;;$$

Now the relationship between $\hat{d}$ and $\hat{d}_2$ may be found from the boundary condition on I_p.

$$D_2 \;=\; f_2 \;(D, V_g, V_o) \;;$$

This on perturbation will lead to,

$$\hat{d}_2 \;=\; f_3 \;\left(\hat{d}, \hat{v}_g, \hat{v}_o\right) \;;$$

Substitution of Eqn. (3.4) into (3.2) will lead to

$$\left(\dot{\hat{x}}\right) \;=\; f_4 \;\left(\hat{x}, \hat{v}_g, \hat{d}\right) \tag{5.134}$$

If the above step is done correctly, the state velocity for the inductor current will turn out to be zero, because the net change in inductor current from the beginning of a cycle to the end of a cycle is zero. The system equations will then be

$$\hat{v}_o \;=\; f_5 \;\left(\hat{i}, \hat{v}_o, \hat{v}_g, \hat{d}\right) \tag{5.135}$$

Eqn. (3.6) is still not the desired form because is present in it. The inductor current may be eliminated from Eq. (3.6) as follows.

$$i \;= \frac{i_{max}}{2} \;=\; f_6 \;\left(\hat{d}, \hat{v}_g, \hat{v}_o\right) \;;$$

On perturbation,

$$\hat{i} \;=\; f_7\;\left(\hat{v}_o, \hat{v}_g, \hat{d}\right)\;;$$

Substitution of (3.8) into (3.6) will give

$$\hat{v}_o \;=\; f^*\;\left(\hat{v}_o, \hat{v}_g, \hat{d}\right) \tag{5.136}$$

Eqn. (3.9) represents the small signal linearised dynamic model of the converter in DCM. The method is illustrated in the following section for the fly back converter.

5.9.2 Fly back Converter Example

For the ideal converter shown in Fig. 22 operating in the discontinuous conduction mode without isolation, the state equations of the converter are

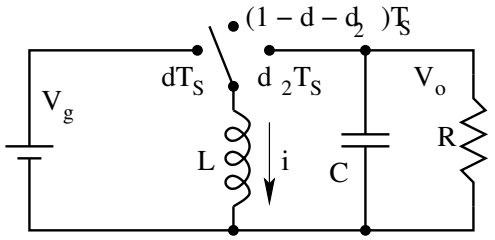

Figure 5.22: Flyback Converter in Discontinuous Conduction

Interval dT_s:

$$L\;\frac{di}{dt} \;=\; v_g\;;\; C\;\frac{dv_o}{dt} \;=\; -\frac{v_o}{R}\;;$$

Interval d_2T_s:

$$L\;\frac{di}{dt} \;=\; v_o\;;\; C\;\frac{dv_o}{dt} \;=\; -i \;-\; \frac{v_o}{R}\;;$$

Interval $(1 - d_1 - d_2)T_s$:

$$L\;\frac{di}{dt} \;=\; 0\;;\; C\;\frac{dv_o}{dt} \;=\; -\frac{v_o}{R}\;;$$

The state equation in the usual notation are:

$$\left(\dot{\hat{x}}\right) \;=\; A\;x \;+\; b\;v_g \;+\; f\;\hat{d} \;+\; g\;\hat{d}_2 \tag{5.137}$$

$$A_1 \;=\; \begin{pmatrix} 0 & 0 \\ 0 & -\dfrac{1}{RC} \end{pmatrix}\;;\; A_2 \;=\; \begin{pmatrix} 0 & -\dfrac{1}{L} \\ \dfrac{1}{C} & -\dfrac{1}{RC} \end{pmatrix}\;;\; A_3 \;=\; \begin{pmatrix} 0 & 0 \\ 0 & -\dfrac{1}{RC} \end{pmatrix}$$

$$b_1 = \begin{pmatrix} \frac{1}{L} \\ 0 \end{pmatrix}; b_2 = \begin{pmatrix} 0 \\ 0 \end{pmatrix}; b_3 = \begin{pmatrix} 0 \\ 0 \end{pmatrix};$$

$$A = \begin{pmatrix} 0 & -\frac{D_2}{L} \\ \frac{D_2}{C} & -\frac{1}{RC} \end{pmatrix}; b = \begin{pmatrix} \frac{D}{L} \\ 0 \end{pmatrix};$$

Steady state solution:

$$X = -A^{-1}bV_g = -\frac{LC}{D_2^2} \begin{pmatrix} -\frac{1}{RC} & \frac{D_2}{L} \\ -\frac{D_2}{C} & 0 \end{pmatrix} \begin{pmatrix} \frac{D}{L} \\ 0 \end{pmatrix} V_g;$$

$$X = \begin{pmatrix} \frac{DV_g}{RD_2^2} \\ -\frac{DV_g}{D_2} \end{pmatrix};$$

$$V_o = -\frac{D}{D_2} V_g \tag{5.138}$$

$$I = \frac{V_g}{RK} \tag{5.139}$$

The small signal model of the converter is

$$f = (A_1 - A_3)X + (b_1 - b_3)V_g = \begin{pmatrix} \frac{V_g}{L} \\ 0 \end{pmatrix};$$

$$g = (A_2 - A_3)X + (b_2 - b_3)V_g = \begin{pmatrix} -\frac{DV_g}{D_2 L} \\ -\frac{DV_g}{RCD_2^2} \end{pmatrix};$$

The small signal model in the state space form is

$$\dot{\hat{x}} = \begin{pmatrix} 0 & \frac{D_2}{L} \\ -\frac{D_2}{C} & -\frac{1}{RC} \end{pmatrix} \hat{x} + \begin{pmatrix} \frac{D}{L} \\ 0 \end{pmatrix} \hat{v}_g + \begin{pmatrix} \frac{V_g}{L} \\ 0 \end{pmatrix} \hat{d} + \begin{pmatrix} -\frac{DV_g}{D_2 L} \\ -\frac{DV_g}{RCD_2^2} \end{pmatrix} \hat{d}_2$$

From the above equation $\hat{d}_2$ may be eliminated with the help of the following relationship.

$$I_p = \frac{v_g d T_S}{L} = -\frac{v_o d_2 T_S}{L};$$

$$\hat{d}_2 = -\frac{V_g}{V_o}\hat{d} - \frac{D}{V_o}\hat{v}_g - \frac{D_2}{V_o}\hat{v}_o \ ;$$

The system equation on elimination of $\hat{d}_2$, reduces to

$$\dot{\hat{x}} = \begin{pmatrix} 0 & 0 \\ -\frac{D_2}{C} & -\frac{2}{RC} \end{pmatrix} \hat{x} + \begin{pmatrix} 0 \\ -\frac{D}{D_2 RC} \end{pmatrix} \hat{v}_g + \begin{pmatrix} 0 \\ -\frac{V_g}{D_2 RC} \end{pmatrix} \hat{d}$$

From the above equation $\hat{i}$ may be eliminated with the help of the following relationship

$$I = \frac{DV_g}{RK} \ ; \ K = \frac{2L}{RT_s} \ ; \ \hat{i} = \frac{V_g}{KR}\hat{d} + \frac{D}{KR}\hat{v}_g \ ;$$

Substitution for $\hat{i}$ leads to

$$\hat{v}_o = -\frac{2}{RC}\hat{v}_o - \frac{2D}{D_2 RC}\hat{v}_g - \frac{2V_g}{D_2 RC}\hat{d} \tag{5.140}$$

Or, in frequency domain

$$\frac{\hat{v}_o(s)}{\hat{d}(s)} = \frac{V_g}{\sqrt{K}} \frac{1}{1 + \frac{s}{\omega_p}} \ ; K = \frac{2L}{RT_s} \ ; \omega_p = \frac{2}{RC} \tag{5.141}$$

$$\frac{\hat{v}_o(s)}{\hat{v}_g(s)} = \frac{M}{1 + \frac{s}{\omega_p}} \ ; \ M \ = \frac{V_o}{V_g} \tag{5.142}$$

As expected the inductor current in the converter operating under DCM has ceased to be a state of the converter and hence the order of the converter has reduced by 1. However both the gain as well as the characteristic frequency of the converter is not very much dependent on the operating point through M (V_o/V_g), the conduction parameter K, as well as load $(\omega_p = \frac{2}{RC})$.

5.10 Problem Set

1. Figure 1 shows a non-isolated boost converter operating under CCM. For this converter, evaluate the small signal dynamic model in the standard form.

$$\begin{pmatrix} \dot{\hat{i}} \\ \dot{\hat{v}} \end{pmatrix} = \begin{pmatrix} x & x \\ x & x \end{pmatrix} \begin{pmatrix} \hat{i} \\ \hat{v} \end{pmatrix} + \begin{pmatrix} x \\ x \end{pmatrix} \hat{v}_g + \begin{pmatrix} x \\ x \end{pmatrix} \hat{d}$$

2. Figure 2 shows a non-isolated boost converter. Evaluate the small signal output impedance (Z_o) of the converter at f = 0 Hz, and at f = ∞ Hz.

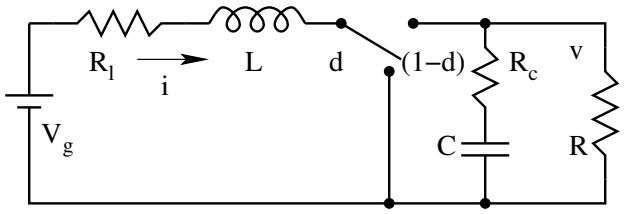

Fig. P 5.1: Non-isolated Boost Converter in CCM

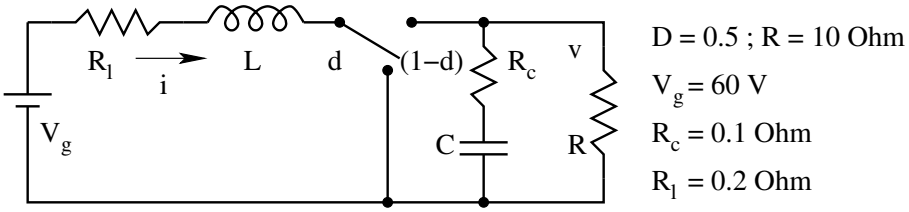

Fig. P 5.2: Output Impedance of Non-isolated Boost Converter

3. Consider the buck converter shown in Fig. 3. The dynamic model of the converter may be written as

$$\dot{\hat{x}} \;=\; A\,\hat{x} \;+\; b\,\hat{v}_g \;+\; f\,\hat{d}_p$$

Where d_p is the duty ratio of the power switch. The control transfer function is given by

$$\frac{\hat{v}(s)}{\hat{d}_p(s)} \;=\; \frac{10}{1 \;+\; \dfrac{s}{Q\omega_o} \;+\; \dfrac{s^2}{\omega_o^2}}\;;$$

$$Q \;=\; 3.8\;;\; \omega_o = 2\pi(2055) rad/sec\;;$$

In real converters, the duty ratio of the power switch and the duty ratio as commanded by the driver (d_c) are not the same on account of the storage delay time of the power-switching device. This is illustrated in Fig. 4b. The duty ratios and are related to each other as follows

$$d_p \;=\; d_c \;+\; \left(1 - \frac{i}{i_{max}}\right)\,\frac{t_s}{T_S}$$

Where t_s, T_S , I_{max}, and I are respectively, storage delay time of the switch, switching period of the switch, maximum current through the switch, and the switching period of the converter. For the above converter,

$$T_S = 25\mu S\;;\; t_s = 5\mu S\;;\; I_{max} = 10A\;;$$

Take into account the storage delay effect as modeled above and evaluate the corrected control transfer function of the buck converter. Make comments on your result.

4. The converter shown in Fig. 4 is a tapped boost converter. Consider the core flux Φ and the capacitor voltage V_c as the state variables.

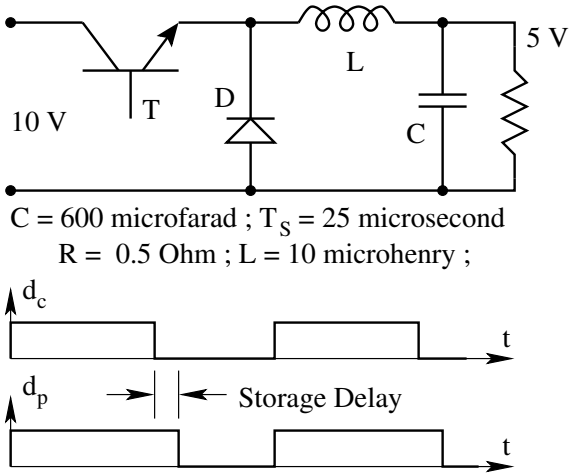

Fig. P 5.3: Buck Converter with Storage Delay Time

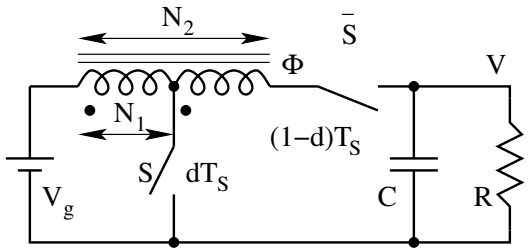

Fig. P 5.4: Tapped Boost Converter

(A) Write down the dynamic equations of the converter during the ON time (S ON) and OFF time ($\overline{S}$ ON).

(B) Write down the averaged dynamic equations.

(C) Find the steady state solution of the core flux Φ and the capacitor voltage V_c.

5. Consider the buck-boost converter shown in Fig. 5. The converter is operating under DCM, the state space averaged model for the converter is

$$\begin{pmatrix} \dot{i} \\ \\ \dot{v} \end{pmatrix} = \begin{pmatrix} 0 & \dfrac{d_2}{L} \\ \\ -\dfrac{d_2}{L} & -\dfrac{1}{RC} \end{pmatrix} \begin{pmatrix} i \\ \\ v \end{pmatrix} + \begin{pmatrix} \dfrac{d}{L} \\ \\ 0 \end{pmatrix} v_g$$

Under steady state, $D_2 = \sqrt{K}$, where K is the conduction parameter $2L/RT_S$.

(A) Find the steady state values for V and I.

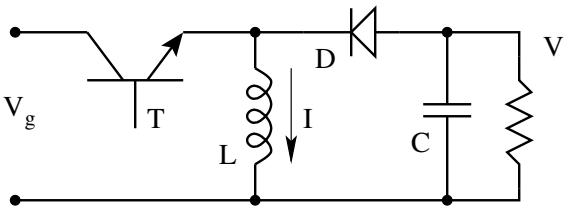

Fig. P 5.5: Frequency Modulated Flyback Converter

(B) We wish to control this converter by keeping the duty ratio D and input voltage V_g constant and by varying the switching frequency $f_s = (F_s + \hat{f}_s)$, around the steady state operating frequency F_s. Under such a condition, we have also seen that the small signal model is

$$\dot{\hat{v}} \;=\; -D_2\frac{\hat{i}}{C} \;-\; 2\frac{\hat{v}}{RC}$$

(C) Evaluate the small signal transfer function $\dfrac{\hat{v}(s)}{\hat{f}(s)}$ for the converter and comment on the salient points of this transfer function.

6. The following circuit in Fig. 6 shows a three state boost converter [$0 < d_1 < 0.5$; $0 < d_2 < 0.5$].

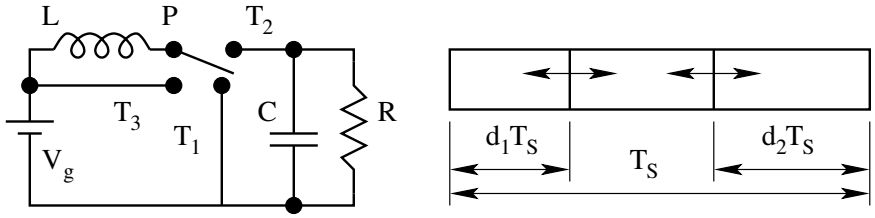

Fig. P 5.6: Three State Boost Converter

(A) How many independent switch control inputs are there? What are they?

(B) Evaluate the gain as a function of the control inputs.

(C) Sketch the steady-state inductor current waveform for one cycle.

(D) Write down the state equations of the converter for each switch position.

(E) How will you realize the switches PT_1, PT_2, and PT_3.

7. Figure 7a shows a Cuk converter. Its averaged model and canonical small signal ac model are shown in Figs 7b and 7c respectively.

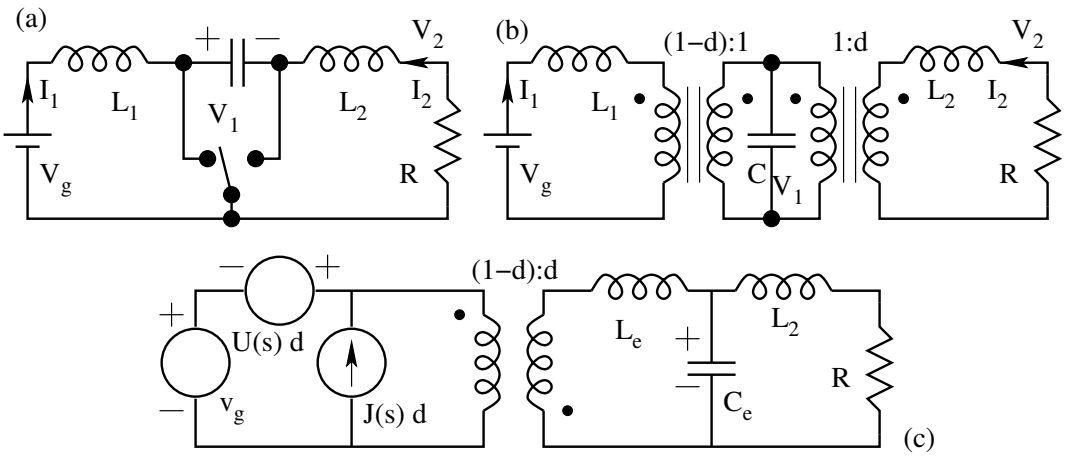

Fig. P 5.7: Cuk Converter

(A) Find the steady state values of V_1, I_1, I_2 and V_3 in terms of V_g, R, and D.

(B) Through circuit manipulations, evaluate the model parameters L_e, C_e, $U(s)$, and $J(s)$ of the small signal ac model shown in Fig. 7c.

8. The circuits obtained in a buck converter in its ON duration and OFF duration are shown in Fig. 8. The dynamic variables of the converter are i and v_o.

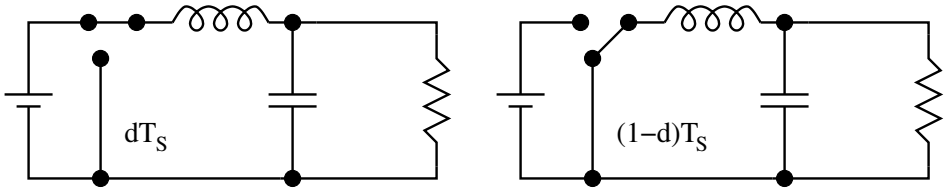

Fig. P 5.8: Buck Converter

(A) Evaluate the averaged model of the converter in the following format.

$$\begin{aligned} \frac{di}{dt} &= f_1(i, v_o, v_g, d) \\ \frac{dv_o}{dt} &= f_2(i, v_o, v_g, d) \\ v_o &= g(i, v_o) \end{aligned}$$

(B) Evaluate the small signal linear model of the converter when excited with inputs $d = D + \hat{d}$, $v_g = V_g + \hat{v}_g$, in the state space format where $x = [i \quad v_o]^T$, and the dynamic quantities are the ac perturbations in the variables.

$$\dot{\hat{x}} = A\,\hat{x} + b\,\hat{v}_g + f\,\hat{d}$$
$$\hat{v}_o = q\,\hat{x}$$

(C) Evaluate the small signal transfer function $\left(\frac{\hat{v}_o(s)}{\hat{d}(s)}\right)_{\hat{v}_g=0}$ of the converter

9. The circuits of a boost converter in its ON duration and OFF duration are shown in Fig. 9. The dynamic variables of the converter are i and v_o. The output of the converter is i.

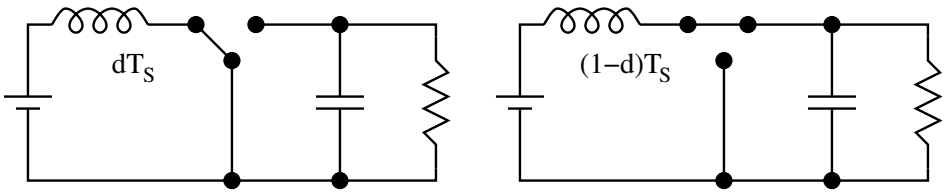

Fig. P 5.9: Boost Converter

(A) For each of the circuits, write down the state equations and the output equation in the following format, where $x = [i \quad v_o]^T$.

$$\dot{\hat{x}} = A_1\,\hat{x} + b_1\,\hat{v}_g$$
$$\hat{i} = p_1\,\hat{x}$$
$$\dot{\hat{x}} = A_2\,\hat{x} + b_2\,\hat{v}_g$$
$$\hat{i} = p_2\,\hat{x}$$

(B) Evaluate the averaged model of the converter when the converter is operating with a duty ratio D in the following format.

$$\dot{\hat{x}} = A\,\hat{x} + b\,\hat{v}_g$$
$$\hat{i} = p\,\hat{x}$$

(C) Solve the system of equations to get the steady state current I in the inductor and the steady state voltage V_o.

(D) Evaluate the steady state input impedance of the converter $\left(\frac{\hat{i}(s)}{\hat{v}_g(s)}\right)$ of the converter.

10. The circuits of a boost converter in its ON duration and OFF duration are shown in Fig. 10. The dynamic variables of the converter are i and v_o.

(A) Evaluate the averaged model of the converter in the following format.

$$\frac{di}{dt} = f_1(i, v_o, v_g, d)$$

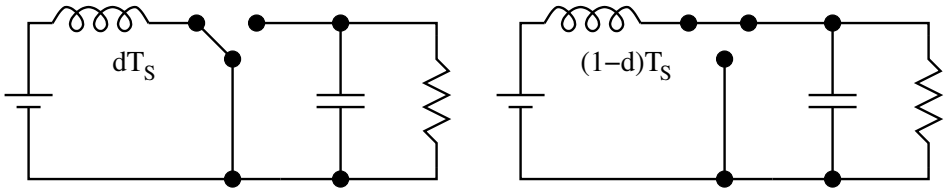

Fig. P 5.10: Boost Converter

$$\frac{dv_o}{dt} = f_2(i, v_o, v_g, d)$$
$$v_o = g(i, v_o)$$

(B) Evaluate the small signal linear model of the converter when excited with inputs $d = D + \hat{d}$, $v_g = V_g + \hat{v}_g$, in the state space format where $x = [i \quad v_o]^T$, and the dynamic quantities are the ac perturbations in the variables.

$$\dot{\hat{x}} = A\,\hat{x} + b\,\hat{v}_g + f\,\hat{d}$$
$$\hat{v}_o = q\,\hat{x}$$

(C) Evaluate the small signal transfer function $\left(\frac{\hat{v}_o(s)}{\hat{d}(s)}\right)_{\hat{v}_g=0}$ of the converter

11. The circuits of a buck-boost converter in its ON duration and OFF duration are shown in Fig. 11. The dynamic variables of the converter are i and v_o. The output of the converter is i_g.

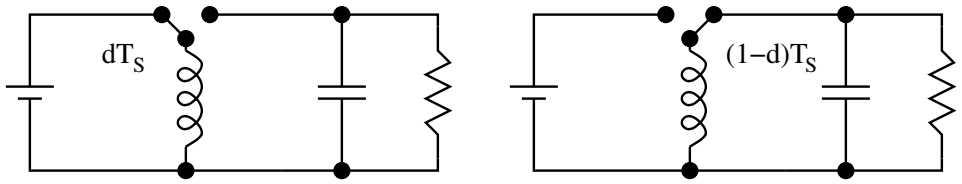

Fig. P 5.11: Buck-Boost Converter

(A) For each of the circuits, write down the state equations and the output equation in the following format, where $x = [i \quad v_o]^T$.

$$\hat{x} = A_1\,\hat{x} + b_1\,\hat{v}_g$$
$$\hat{i} = p_1\,\hat{x}$$
$$\hat{x} = A_2\,\hat{x} + b_2\,\hat{v}_g$$
$$\hat{i} = p_2\,\hat{x}$$

(B) Evaluate the averaged model of the converter when the converter is operating with a duty ratio D in the following format.

$$\hat{x} = A\,\hat{x} + b\,\hat{v}_g$$

$$\hat{i} \;=\; p\;\hat{x}$$

(C) Solve the system of equations to get the steady state current I in the inductor and the steady state voltage V_o.

(D) Evaluate the steady state input impedance of the converter $\left(\frac{\hat{i}_g(s)}{\hat{v}_g(s)}\right)$ of the converter.

12. Figure 12 shows a multiple output forward converter. The converter data are as follows.

$V_g \;=\; 100V\;;\; D \;=\; 0.4\;;\; N : N_1 : N_2 \;=\; 1 : 0.3 : 0.125\;;$
$R_1 \;=\; 12\;\Omega\;;\; R_2 \;=\; 0.5\;\Omega\;;\; L_1 \;=\; 1.5\;mH\;;$
$L_2 \;=\; 0.15\;mH\;;\; C_1 \;=\; 33\;\mu F\;;\; C_2 \;=\; 33\;\mu F\;;$
$R_{c1} \;=\; 0.1\;\Omega\;;\; R_{c2} \;=\; 0.05\;\Omega\;;\; R_{l1} \;=\; 0.5\;\Omega\;;$
$R_{l2} \;=\; 0.03\;\Omega\;;\; R_{s1} \;=\; 0.3\;\Omega\;;\; R_{s2} \;=\; 0.01\;\Omega\;;$
$R_p \;=\; 0.02\;\Omega\;;$

Circuit Equations in dT_S:

$$P\dot{x} \;=\; A_1\;x \;+\; b_1\;v_g \;+\; m_1\;i_z$$
$$v_o \;=\; q_1\;x \;+\; k_1\;i_z$$
$$i_g \;=\; p_1\;x$$

$$P \;=\; \begin{pmatrix} L_1 & 0 & 0 & 0 \\ 0 & L_2 & 0 & 0 \\ 0 & 0 & C_1 & 0 \\ 0 & 0 & 0 & C_2 \end{pmatrix}\;;\; v_o \;=\; \begin{pmatrix} v_{o1} \\ v_{o2} \end{pmatrix}\;;\; i_z \;=\; \begin{pmatrix} i_{z1} \\ i_{z2} \end{pmatrix}\;;$$

$$x \;=\; \begin{pmatrix} i_{L1} & i_{L2} & v_{C1} & v_{C2} \end{pmatrix}^T\;;$$

Circuit Equations in $(1-d)T_S$:

$$P\dot{x} \;=\; A_2\;x \;+\; b_2\;v_g \;+\; m_2\;i_z$$
$$v_o \;=\; q_2\;x \;+\; k_2\;i_z$$
$$i_g \;=\; p_2\;x$$

(A) Evaluate the system matrices.

13. Figure 13 shows a multiple output flyback converter. The converter data are as follows.

$V_g \;=\; 50V\;;\; D \;=\; 0.3\;;\; N : N_1 : N_2 \;=\; 1 : 1 : 0.5\;;$
$R_1 \;=\; 5\;\Omega\;;\; R_2 \;=\; 2\;\Omega\;;\; L_p \;=\; 1.0\;mH\;;$
$L_{s1} \;=\; 1.0\;mH\;;\; L_{s2} \;=\; 0.25\;mH\;;\; C_1 \;=\; 470\;\mu F\;;$
$C_2 \;=\; 1000\;\mu F\;;\; R_{c1} \;=\; 0.05\;\Omega\;;\; R_{c2} \;=\; 0.03\;\Omega\;;$
$R_{s1} \;=\; 0.1\;\Omega\;;\; R_{s2} \;=\; 0.04\;\Omega\;;\; R_p \;=\; 0.1\;\Omega\;;$

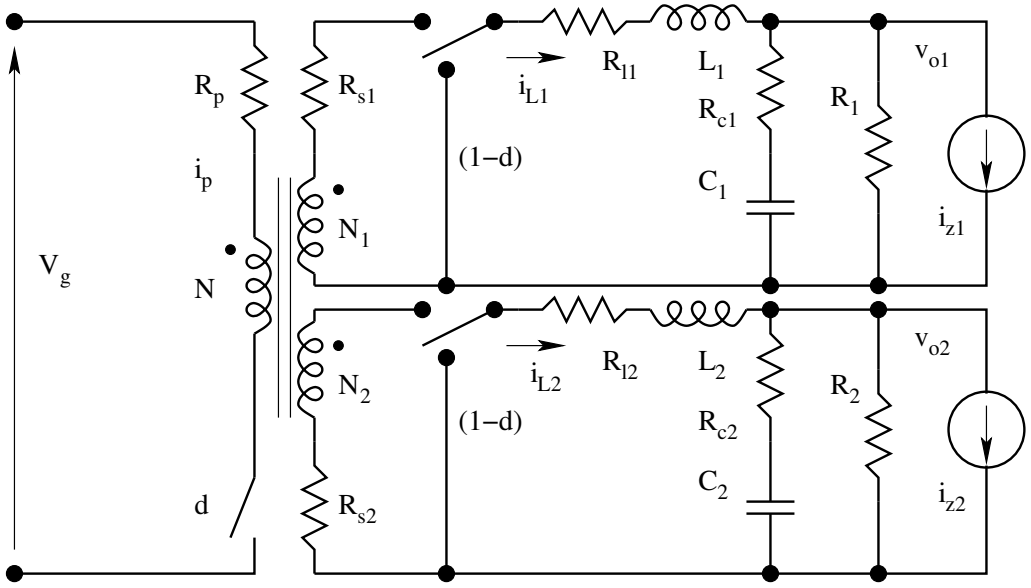

Fig. P 5.12: Buck-Boost Converter

Circuit Equations in dT_S:

$$P\dot{x} = A_1\, x + b_1\, v_g + m_1\, i_z$$
$$v_o = q_1\, x + k_1\, i_z$$
$$i_g = p_1\, x$$

$$P = \begin{pmatrix} L_p & 0 & 0 \\ 0 & C_1 & 0 \\ 0 & 0 & C_2 \end{pmatrix}\ ;\ v_o = \begin{pmatrix} v_{o1} \\ v_{o2} \end{pmatrix}\ ;\ i_z = \begin{pmatrix} i_{z1} \\ i_{z2} \end{pmatrix}\ ;$$

$$x = \begin{pmatrix} i_p & v_{C1} & v_{C2} \end{pmatrix}^T\ ;$$

Circuit Equations in $(1-d)T_S$:

$$P\dot{x} = A_2\, x + b_2\, v_g + m_2\, i_z$$
$$v_o = q_2\, x + k_2\, i_z$$
$$i_g = p_2\, x$$

(A) Evaluate the system matrices.

14. The circuit shown in Fig. 14 is an isolated fly back converter. Evaluate the system matrices $A_1, A_2, b_1, b_2, m_1, m_2, q_1, q_2, k_1, k_2, p_1$, and p_2.

$$V_g = 100V\ ;\ D = 0.3\ ;\ N_p : N_s = 1 : 0.2\ ;$$
$$R_p = 1.0\ \Omega\ ;\ R_s = 0.5\ \Omega\ ;\ L = 1.5\ mH\ ;$$
$$C = 100\ \mu F\ ;\ R_c = 0.1\ \Omega\ ;\ R_l = 0.5\ \Omega\ ;$$
$$R = 20.0\ \Omega\ ;$$

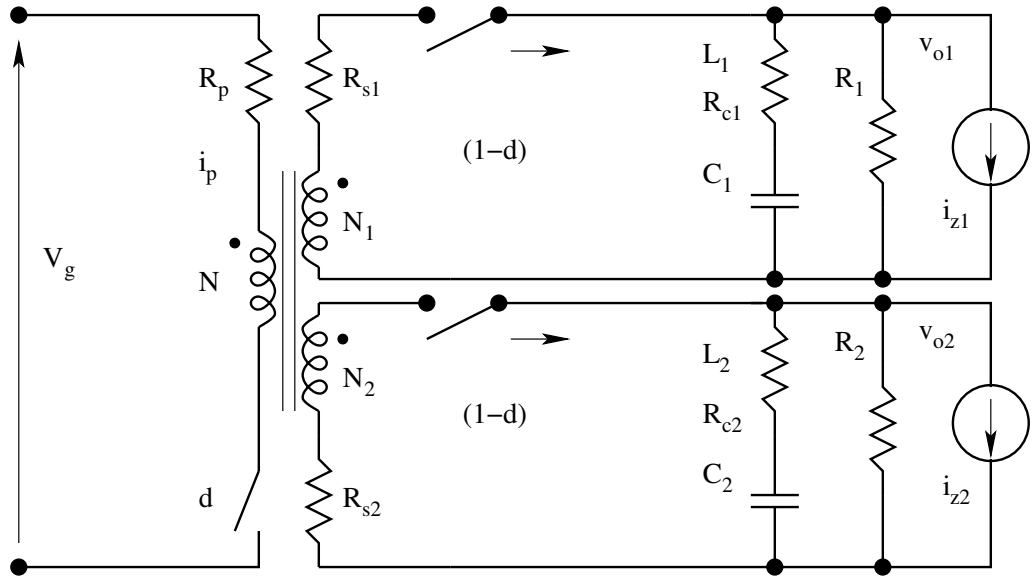

Fig. P 5.13: Buck-Boost Converter

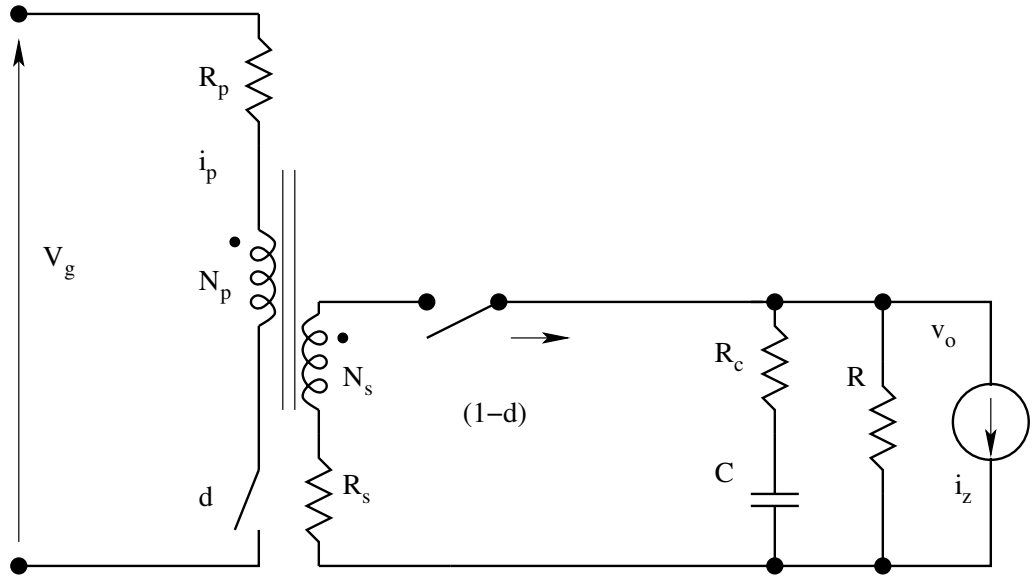

Fig. P 5.14: Buck-Boost Converter

15. For the converter shown in Fig. 15, the various ON state and OFF state matrices are given.
ON Time:

$$\begin{pmatrix} \dot{i} \\ \\ \dot{v} \end{pmatrix} = \begin{pmatrix} 0 & 0 \\ \\ 0 & -\frac{1}{RC} \end{pmatrix} \begin{pmatrix} i \\ \\ v \end{pmatrix} + \begin{pmatrix} \frac{1}{L} \\ \\ 0 \end{pmatrix} v_g + \begin{pmatrix} 0 \\ \\ -\frac{1}{C} \end{pmatrix} i_z$$

$$v = [0 \quad 1]\ [i \quad v]^T$$

$$i_g = [1 \quad 0]\ [i \quad v]^T$$

OFF Time:

$$\begin{pmatrix} \dot{i} \\ \\ \dot{v} \end{pmatrix} = \begin{pmatrix} 0 & -\frac{1}{L} \\ \\ \frac{1}{C} & -\frac{1}{RC} \end{pmatrix} \begin{pmatrix} i \\ \\ v \end{pmatrix} + \begin{pmatrix} \frac{1}{L} \\ \\ 0 \end{pmatrix} v_g + \begin{pmatrix} 0 \\ \\ -\frac{1}{C} \end{pmatrix} i_z$$

$$v = [0 \quad 1]\ [i \quad v]^T$$

$$i_g = [1 \quad 0]\ [i \quad v]^T$$

$D = 0.4$; $V_g = 15V$; $L = 2\ mH$; $R = 100\ Ohm$; $C = 10\ \mu F$;

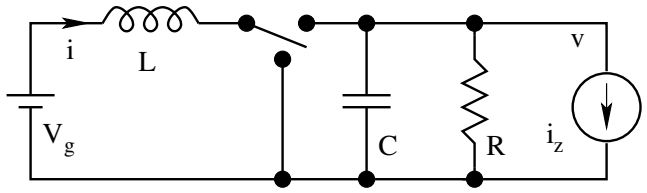

Fig. P 5.15: Buck-Boost Converter

(A) Evaluate the expression for steady state quantities I and V.

(B) Find I and V for the given component values and operating condition.

(C) Evaluate the expression for output impedance for the converter

$$Z_o = \left(\frac{\hat{v}}{\hat{i}_z}\right)_{(\hat{d} = 0\ ;\ \hat{v}_g = 0)}$$

(D) Find out the same at the given operating condition for the given component values.

Chapter 6

Closed Loop Control of Power Converters

6.1 Introduction

We have seen the objective of obtaining constant dc output voltage from the converter is achieved through the closed loop control of the output i.e. constant duty ratio is automatically adjusted in order to obtain the desired output voltage. In the last chapter we had seen the basic theory of linear dynamics and the principles of closed loop control [16]. In this chapter the control requirements of the dc-dc converter are stated and are related to the frequency domain performance indices such as the loop gain, cross-over frequency, dc loop-gain, phase margin of the loop gain and so on. The closed loop controller design is briefly outlined and then demonstrated through the example of a boost converter.

6.2 Closed Loop Control

6.2.1 Control Requirements

The control specification of the converter will be in two parts.

- Steady state accuracy
- Settling time and allowed transient overshoot in the event of disturbances or command changes.

The steady state error is related to the loop gain T of the closed loop at dc. The steady state error is approximately $1/T(0)$. For example, a loop gain at dc $T(0)$ of 100 will result in a steady state error of about 1%. The settling time and transient overshoot are related to the 0 dB crossover frequency of the loop gain and the phase margin. If ω_c is the 0 dB crossover frequency of the loop gain, then the settling time (for a stable system) will be about to

$3/\omega_c$ to $4/\omega_c$ seconds. The approximate transient overshoot is related to the phase margin (ϕ_m) of the loop gain according to the Table 1 For acceptable

Table 6.1: Phase Margin vs Transient Overshoot

Phase Margin (Degree)	30°	35°	40°	45°	50°	55°	60°
Transient Overshoot (%)	37%	30%	25%	16%	9%	5%	1%

transient overshoot, the phase margin may be taken as 45°. The first design step in closed loop controller design is to convert the control specification to the following.

- Desired T(0) [to meet the steady state error]
- Desired ω_c [to meet the settling time]
- Desired phase margin ϕ_m [to meet the transient overshoot]

6.2.2 Compensator Structure

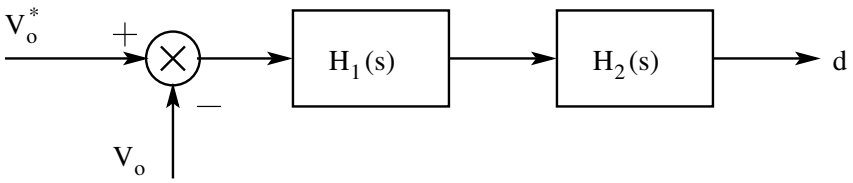

Figure 6.1: Structure of the Closed Loop Controller

The requirement in the design of a closed loop controller is to identify and design a compensator $H(s)$ such that the loop gain $T(s)$ $[G(s)H(s)]$ satisfies the above requirements. The structure of the closed loop controller $H(s)$ is shown in Fig.1. The blocks $H_1(s)$ and $H_2(s)$ are the cascaded stages of the compensator. The closed loop compensator design is considered in $[H(s) = H_1(s)H_2(s)]$ two parts. The first stage $H_1(s)$ of the compensator achieves the desired bandwidth ω_c and the desired phase margin ϕ_m, and the second stage is designed to meet the desired steady state error.

6.2.3 Design of Compensator

The important rule that is used here is that, if the loop gain crosses 0 dB (unity gain) with a single slope (-20dB/decade), then the closed loop system will be stable. The reason is that the phase gain of a function crossing 0 dB with a single slope at a frequency of ω_c is approximately the same as the function $K/\omega_c(s)$ and is equal to $-90°$. This argument is valid only when the loop gain is a minimum phase function. The actual phase angle will depend

on the poles and zeroes nearest to the crossover frequency. With the above simple rule in mind, the compensator function $H_1(s)$ is selected to be simple lead-lag compensator.

$$H_1(s) \;=\; K_1 \frac{1+\dfrac{s}{\omega_{z1}}}{1+\dfrac{s}{\omega_{p1}}} \tag{6.1}$$

The purpose of is to make the slope of crossover section of the loop gain to -20 dB/decade near the desired crossover frequency, and to improve the phase margin.

- If G(s) is a first order system in the vicinity of ω_c, then H_1 may be just K_1.
- If G(s) is a second order system in the vicinity of ω_c, then select ω_{z1} and ω_{p1} such that $\omega_{z1} \;<\; \omega_c \;<\; \omega_{p1}$
- If G(s) is a second order system with a complex pole pair ω_o then $\omega z1$ may be taken as ω_o. ω_{p1} is usually as ten times ω_{z1}.
- Now K_1 may be selected to meet the requirements of ω_c and ϕ_m.

The next part of the compensator $H_2(s)$ is needed to meet the steady state error specification. If $G(0)H_1(0)$ is already compatible with the steady state error, then $H_2(s)$ is 1. However, if $G(0)H_1(0)$ is not compatible with the desired steady state error, $H_2(s)$ is different from unity. The conditions on $H_2(s)$ are

- $G(0)H_1(0)H_2(0) \;=\; T(0)$.
- $H_2(s)$ must not affect the gain & phase margin already designed. Or in the other words, phase and magnitude gain of $H_2(s)$ in the vicinity of ω_c must be 0° and 0dB respectively.
- A PI controller of the form $H_2(s) \;=\; \dfrac{1+\dfrac{s}{\omega_{z2}}}{\dfrac{s}{\omega_{z2}}}$ satisfies the above requirements.

The overall compensator is

$$H(s) \;=\; \frac{1+\dfrac{s}{\omega_{z2}}}{\dfrac{s}{\omega_{z2}}}\; K_1 \frac{1+\dfrac{s}{\omega_{z1}}}{1+\dfrac{s}{\omega_{p1}}} \tag{6.2}$$

and can be realized using operational amplifiers (as shown in the example).

6.2.4 A Simple Design Example

The design method is illustrated for the following example.
Boost Converter:

$$V_g = 15\ V\ ;\ R = 100\ \Omega\ ;\ R_l = 0.5\ \Omega\ ;$$
$$C = 150\ \mu F\ ;\ L = 2\ mH\ ;\ T_S = 50\ \mu S\ ;\ D = 0.3\ ;$$

Design Specifications

1. Steady state error less than 1%.
2. Bandwidth to be greater than 1000Hz (6280 rad/sec).
3. Phase margin to be better than 45°.

The open loop control transfer function of the converter is

$$G(s) = \frac{\left(1-\frac{s}{\omega_z}\right)\left(1+\frac{s}{\omega_a}\right)}{1+\frac{s}{Q\omega_o}+\frac{s^2}{\omega_o^2}} \tag{6.3}$$

$$\omega_o \Rightarrow 205\ Hz\ ;\ \omega_z \Rightarrow 3800\ Hz\ ;\ \omega_a \Rightarrow 2100\ Hz\ ;$$

The open loop control transfer function of the converter is plotted in Fig.2.

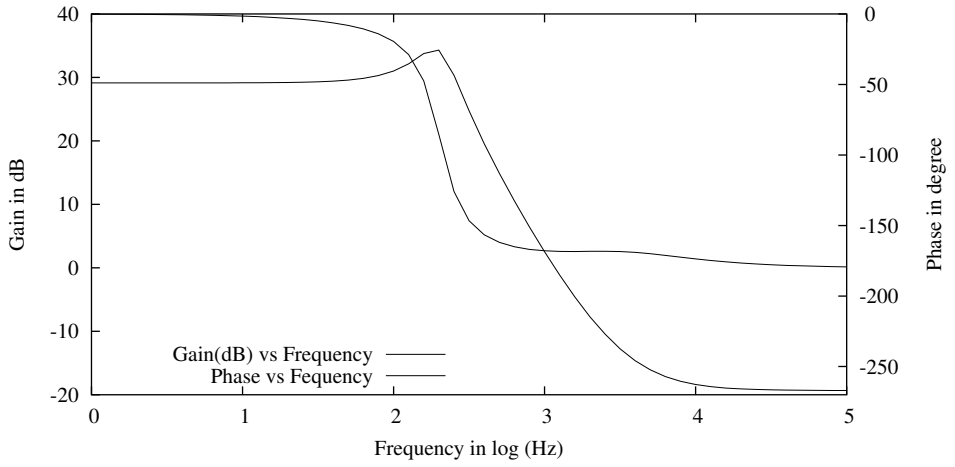

Figure 6.2: Magnitude and Phase Plot of the Open Loop Transfer Function

It may be noticed that the 0dB crossover frequency is about 2000 rad/sec, & the phase margin with unity feedback is about 5°. The dc gain of 28 leads to steady state error with unity feedback of about 4%. To meet the given specifications therefore a compensator has to be added. As a first step in the design of compensator, we select $H_1(s)$ (to meet bandwidth & phase margin) as follows

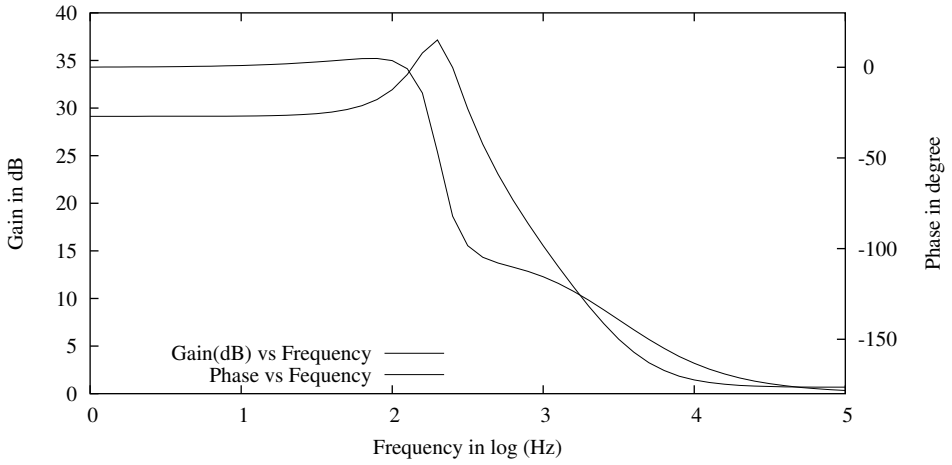

Figure 6.3: Gain and Phase with the First Part of the Compensator

$$H_1(s) \;=\; \frac{1+\dfrac{s}{1288.0}}{1+\dfrac{s}{12880.0}} \tag{6.4}$$

Notice that the compensating zero is taken as the same as ω_o. The Bode

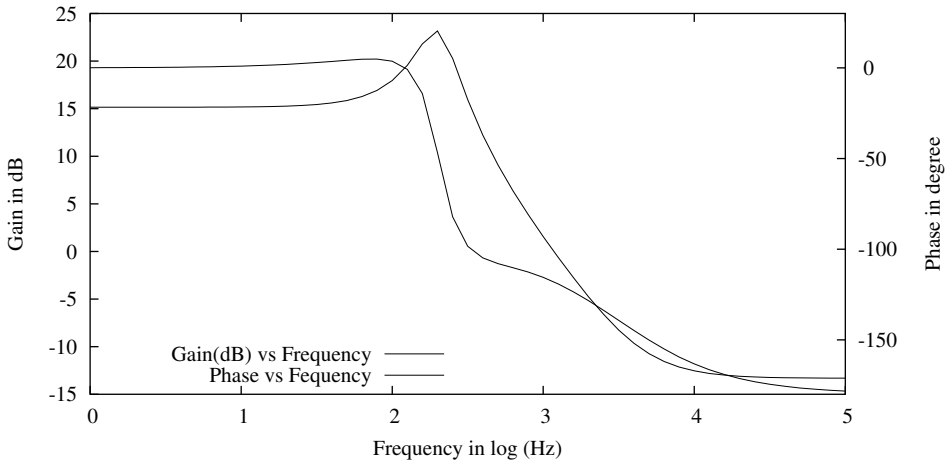

Figure 6.4: Gain and Phase with the Second Part of the Compensator

plot of $G(s)H_1(s)$ is plotted in Fig.3. It is seen that the phase has improved. The 0 dB crossover may now be set near 1000Hz by selecting K_1 equal to 0.2. The loop gain of is plotted in Fig.4 for this new. It is seen that for this new the 0 dB crossover frequency is about 7000 rad/sec, and the phase margin is more than 55°. The first part of the design is complete. With $H_1(s)$ as a compensator both bandwidth and phase margin requirements are met. Notice

also that the dc gain is only about 5 (15 dB). Therefore to meet the steady state error specification we chose a PI controller of the form

$$H_2(s) = \frac{1 + \frac{s}{\omega_{z2}}}{\frac{s}{\omega_{z2}}} \tag{6.5}$$

ω_{z2} (700) is chosen much less than ω_c. The loop gain of $G(s)H_1(s)H_2(s)$

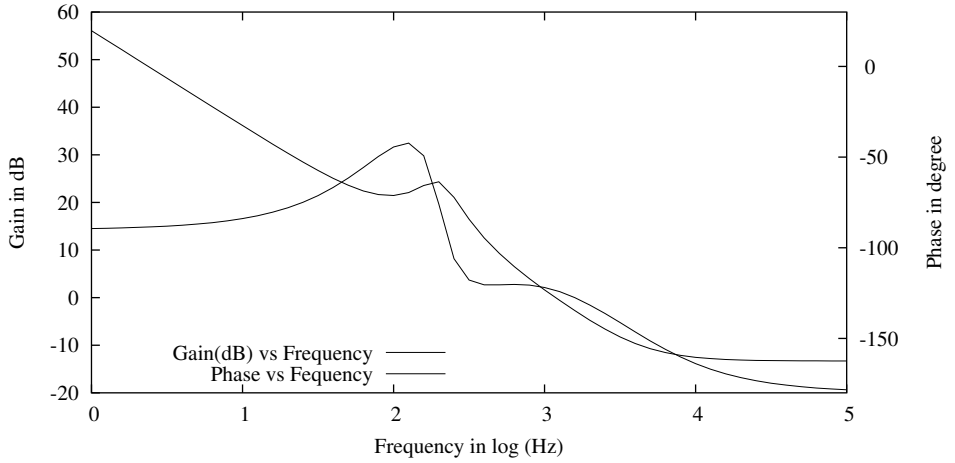

Figure 6.5: Gain and Phase Plot of the Loop Gain

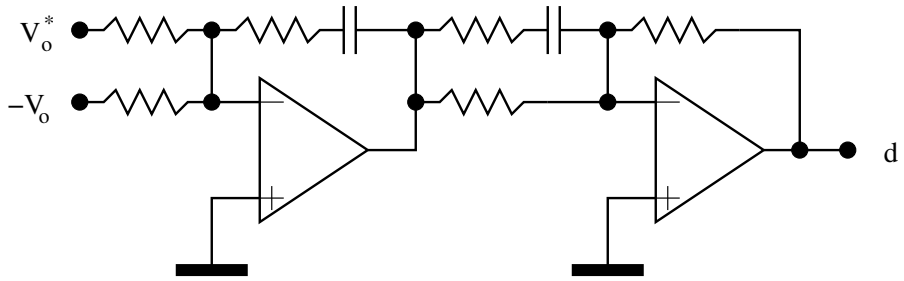

Figure 6.6: Circuit Realisation of the Compensator

is shown in Fig. 5. Figure 6 shows a circuit realisation of the closed loop compensator incorporating, $H_1(s)$, $H_2(s)$, and K_1.

6.3 Closed Loop Performance Functions

We have seen a number of performance figures of the converter under open loop namely

F : Audio Susceptibility;
Y_{in} : Input Admittance
Z_o : Output Impedance
When a closed loop compensator is added to the converter the overall structure

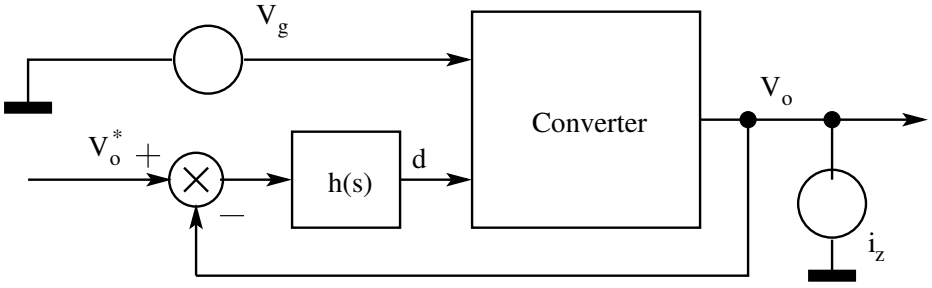

Figure 6.7: Converter Under Closed Loop Operation

of the converter changes as shown in Fig. 7 and as a result some of these performance figures also change. Under closed loop operation, feedback gain is $-h(s)$.

$$\hat{d} \;=\; -\,h\;\hat{v}_o \tag{6.6}$$

With the above constraint, we find out the following closed loop performance figures.

6.3.1 Audio Susceptibility

$$F' \;=\; \frac{\hat{v_o}(s)}{\hat{v_g}(s)}\left(\hat{i}_z \;=\; 0\;;\; \hat{d} \;=\; -h\hat{v}_o\right)$$

$$\left(\dot{\hat{x}}\right) \;=\; A\;\hat{x} \;+\; b\;\hat{v}_g \;+\; f\;\hat{d} \tag{6.7}$$

$$\hat{v}_o \;=\; (\;q_1 \;-\; q_2)\;X\;\hat{d} \;+\; q\;\hat{x} \tag{6.8}$$

$$\hat{d} \;=\; -\,h\;\hat{v}_o \tag{6.9}$$

$$\hat{v}_o \;=\; -h\,(\;q_1 \;-\; q_2)\;X\;\hat{v}_o \;+\; q\;\hat{x} \;=\; \frac{q}{1 \;+\; h(q_1 - q_2)X}\;\hat{x} \tag{6.10}$$

Substituting the result of Eq. (10) in Eq. (7), we get

$$\hat{x} \;= (sI - A)^{-1}\;b\;\hat{v}_g \;-\; \frac{hq\,[sI - A]^{-1}\,f}{1 + h(q_1 - q_2)X}\;\hat{x} \tag{6.11}$$

$$q\;\hat{x} \;=\; q\,(sI - A)^{-1}\;b\;\hat{v}_g \;-\; \frac{hq\,[sI - A]^{-1}\,fq}{1 + h(q_1 - q_2)X}\;\hat{x} \tag{6.12}$$

$$\frac{q\hat{x} + q\hat{x}h(q_1 - q_2)X + hq(sI - A)^{-1}fq\hat{x}}{1 + h\,(q_1 - q_2)\,X} \;=\; q\,(sI - A)^{-1}\,b\hat{v}_g \tag{6.13}$$

$$\hat{v}_o \; + \; h \; G \; \hat{v}_o \; = \; F \; \hat{v}_g \tag{6.14}$$

$$\frac{\hat{v}_o}{\hat{v}_g} \; = \; \frac{F}{1+T} \tag{6.15}$$

6.3.2 Input Admittance

$$Y'_{in} \; = \; \frac{\hat{i_g}(s)}{\hat{v_g}(s)} \left(\hat{i}_z \; = \; 0 \; ; \; \hat{d} \; = \; -h\hat{v}_o \right)$$

$$\hat{i}_g \; = \; (p_1 - p_2) X \hat{d} \; + \; p\hat{x} \tag{6.16}$$

$$\hat{i}_g \; = \; p(sI - A)^{-1} b \hat{v}_g \; - \; h(p_1 - p_2) X \hat{v}_o \; - \; hp(sI - A)^{-1} f \hat{v}_o \tag{6.17}$$

$$Y'_{in} \; = \; Y_{in} - hG_i F' \; = \; Y_{in} \; - \; hG_i \frac{F}{1+T} \tag{6.18}$$

$$Y'_{in} \; = \frac{Y_{in}}{1+T} \; - \; \frac{T}{1+T} \left(\frac{G_i F}{G_v} \; - \; Yin \right) \tag{6.19}$$

6.3.3 Output Impedance

$$Z'_o \; = \; \frac{\hat{v_o}(s)}{\hat{i_z}(s)} \left(\hat{v}_g \; = \; 0 \; ; \; \hat{d} \; = \; -h\hat{v}_o \right)$$

$$\left(\dot{\hat{x}} \right) \; = \; A \; \hat{x} \; + \; f \; \hat{d} \; + \; m \; \hat{i}_z \tag{6.20}$$

$$\hat{v}_o \; = \; (\; q_1 \; - \; q_2) \; X \; \hat{d} \; + \; q \; \hat{x} \tag{6.21}$$

$$\hat{x} \; = \; (sI - A)^{-1} f \hat{d} \; + \; (sI - A)^{-1} m \hat{i}_z \tag{6.22}$$

It is left as an exercise to simplify the above to obtain the following result.

$$Z'_o \; = \; \frac{Z_o}{1+T} \tag{6.23}$$

Closed loop operation is seen to be advantageous for the following reasons.

- Audio Susceptibility is reduced by a factor of (1+T).
- Output Impedance falls by a factor of (1+T).
- Input Admittance falls nearly by a factor of (1+T).
- But one cause of concern is that the input admittance (under closed loop operation) for dc is negative. This may be seen by the fact that since the dc output voltage and power is constant in closed loop operation, and the losses being small, any increase in input voltage will result in a decrease in the input current.

We had seen the design of the closed loop controller for a duty cycle controlled switched mode power converter in this section based on a few simple rules applied to the control gain of the open loop converter. It is also seen that such a closed loop compensator also improves the audio susceptibility and the output impedance of the converter. The negative input impedance of the converter can lead to instability of the converter when it is connected to a source with finite source impedance. The design guidelines to overcome such problems are covered in the following sections.

6.4 Effect of Input Filter on the Converter Performance

We have already seen that the following are the performance figures of the converter (with the defined notations) under open loop.
Audio Susceptibility:

$$F \;=\; q\;(sI - A)^{-1}\;b$$

Input Admittance:

$$Y_i \;=\; p\;(sI - A)^{-1}\;b$$

Output Impedance:

$$Z_o \;=\; q\;(sI - A)^{-1}\;m$$

Control Voltage Gain:

$$G_v \;=\; (q_1 - q_2)X \;+\; q\;(sI - A)^{-1}\;f$$

Control Current Gain:

$$G_i \;=\; (p_1 - p_2)X \;+\; p\;(sI - A)^{-1}\;f$$

Circuit Averaged Voltage Source:

$$U(s) \;=\; \frac{G_v}{F}$$

Circuit Averaged Current Source:

$$J(s) \;=\; G_i \;-\; Y_i\frac{G_v}{F}$$

With a feedback compensator h(s), we have also seen that the loopgain T [$T \;=\; G_v h$], and the converter performance figures are affected in the following way.
Loop gain:

$$T \;=\; G_v h$$

Audio Susceptibility:

$$F' \;=\; \frac{F}{1+T}$$

Input Admittance:

$$Y' \;=\; \frac{Y_i}{1+T} \;-\; \frac{T}{1+T}\frac{J}{U(s)}$$

Output Impedance:

$$Z_o' \;=\; \frac{Z_o}{1+T}$$

Control Voltage gain:

$$G_v' \;=\; G_v$$

Control Current gain:

$$G_i^{'} \;=\; G_i$$

Circuit Averaged Voltage Source:

$$U(s) \;=\; \frac{G_v}{F}$$

Circuit Averaged Current Source:

$$J(s) \;=\; G_i \;-\; Y_i\,\frac{G_v}{F}$$

In the presence of input filter, some of the performance figures undergo a change. If we know how the performance figures are affected by the performance of the input filter, we may develop suitable design criterion for the input filter. Extra element theorem (Appendix B) may be applied for this purpose. In the presence of the input filter, let the loop gain, audio susceptibility, input admittance, output impedance, control voltage gain, control current gain all be altered as follows.

Loop gain with input filter: $T^{''}$
Audio Susceptibility with input filter: $F^{''}$
Input Admittance with input filter: $Y_i^{''}$
Output Impedance with input filter: $Z_o^{''}$
Control Voltage gain: $G_v^{''}$
Control Current gain: $G_i^{''}$

The set up is shown in Fig. 8 (source V_g with the source impedance Z_s). It is

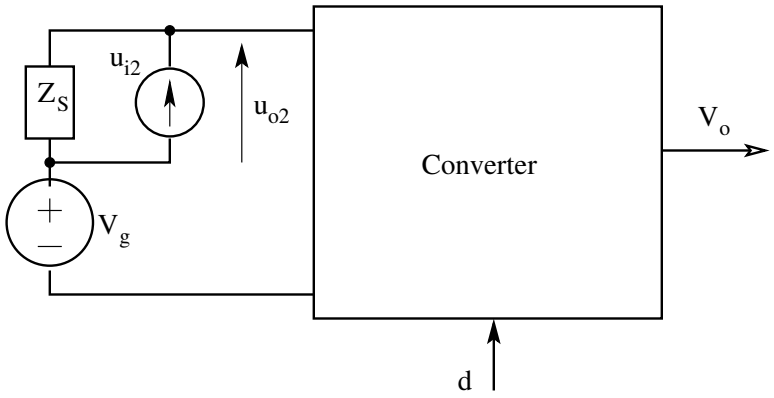

Figure 6.8: Converter with Source with Impedance

set up as per the extra element theorem given in Appendix B, with the second input and the second output defined as u_{i2} and u_{o2} respectively. The duty ratio input is also shown in Fig. 8 as d.

1. Effect on Audio Susceptibility

$$F^{''} \;=\; \left[\frac{\hat{v}_o}{\hat{v}_g}\right]_{(Z_s = Z_s)} \;=\; \left[\frac{\hat{v}_o}{\hat{v}_g}\right]_{(Z_s = 0)} \frac{1 + Z_s Y_n}{1 + Z_s Y_d}$$

$$Y_n = \left[\frac{u_{i2}}{u_{o2}}\right](\hat{v}_o = Null) \; ; Y_d = \left[\frac{u_{i2}}{u_{o2}}\right](\hat{v}_g = 0)$$

$$\left(\dot{\hat{x}}\right) = A\,\hat{x} + b\,(u_{o2} + \hat{v}_g) + f\,\hat{d}$$

$$\hat{v}_o = (q_1 - q_2)X\hat{d} + q\,\hat{x}$$

$$\hat{i}_g = u_{i2} = (p_1 - p_2)X\hat{d} + p\,\hat{x}$$

Y_d: $\hat{v}_g = 0$

$$\hat{x} = (sI - A)^{-1}bu_{o2} + p(sI - A)^{-1}f\hat{d}$$

$$u_{i2} = (p_1 - p_2)X\hat{d} + p(sI - A)^{-1}bu_{o2} + p(sI - A)^{-1}f\hat{d}$$

$$u_{i2} = G_i\hat{d} + Y_i u_{o2}$$

$$u_{i2} = -G_i h\hat{v}_o + Y_i u_{o2}$$

$$Y_d = Y_i - G_i h\frac{F}{1+T}$$

$$Y_d = Y_i^{'}$$

Y_n: $\hat{v}_o = 0 \Rightarrow \hat{d} = 0$

$$\left(\dot{\hat{x}}\right) = A\,\hat{x} + b\,(u_{o2} + \hat{v}_g)$$

$$\hat{v}_o = q\hat{x} = 0$$

$$u_{i2} = p\hat{x}$$

$$\left(\dot{\hat{x}}\right) = (sI - A)^{-1}b\,(u_{o2} + \hat{v}_g)$$

$$q\hat{x} = q(sI - A)^{-1}b\,(u_{o2} + \hat{v}_g) = F\,(u_{o2} + \hat{v}_g) = 0$$

$$u_{o2} = -\hat{v}_g$$

$$Y_n = \frac{u_{i2}}{u_{o2}} = 0$$

$$F^{''} = F^{'}\frac{1}{1 + Z_s Y_i^{'}}$$

2. Effect of Input Admittance

$$Y_i^{''} = \left[\frac{\hat{i}_g}{\hat{v}_g}\right](Z_s = Z_s) = \left[\frac{\hat{i}_g}{\hat{v}_g}\right](Z_s = 0)\frac{1 + Z_s Y_n}{1 + Z_s Y_d}$$

$$Y_n = \left(\frac{u_{i2}}{u_{o2}}\right)_{\hat{i}_g = 0};$$

$$Y_d = \left(\frac{u_{i2}}{u_{o2}}\right)_{\hat{v}_g = 0};$$

$$\hat{i}_g = 0 \Rightarrow Y_n = 0 \; ; \hat{v}_g = 0 \Rightarrow Y_d = Y_i^{'}$$

$$Y_i^{''} = Y_i^{'} \frac{1}{1 + Z_s Y_i^{'}}$$

3. Effect on Output Impedance

$$Z_o^{''} = \left[\frac{\hat{v}_o}{\hat{i}_z}\right]_{(Z_s = Z_s)} = \left[\frac{\hat{v}_o}{\hat{i}_z}\right]_{(Z_s = 0)} \frac{1 + Z_s Y_n}{1 + Z_s Y_d}$$

$$Y_n = \left(\frac{u_{i2}}{u_{o2}}\right)_{\hat{v}_g = 0 \; ; \; \hat{v}_o = 0};$$

$$Y_d = \left(\frac{u_{i2}}{u_{o2}}\right)_{\hat{v}_g = 0 \; ; \; \hat{i}_z = 0};$$

$$\left(\dot{\hat{x}}\right) = A\,\hat{x} + b\,(u_{o2} + \hat{v}_g) + f\,\hat{d} + m\,\hat{i}_z$$

$$\hat{v}_o = (q_1 - q_2) X \hat{d} + q\,\hat{x}$$

$$\hat{i}_g = u_{i2} = (p_1 - p_2) X \hat{d} + p\,\hat{x}$$

Y_d: $\quad \hat{v}_g = 0 \Rightarrow \hat{i}_z = 0$

$$\hat{x} = (sI - A)^{-1} b u_{o2} + (sI - A)^{-1} f \hat{d}$$

$$u_{i2} = (p_1 - p_2) X \hat{d} + p(sI - A)^{-1} b u_{o2} + p(sI - A)^{-1} f \hat{d}$$

$$u_{i2} = G_i \hat{d} + Y_i u_{o2}$$

$$u_{i2} = -G_i h \hat{v}_o + Y_i u_{o2}$$

$$Y_d = Y_i - G_i h \frac{F}{1 + T}$$

$$Y_d = Y_i^{'}$$

Y_n: $\quad \hat{v}_o = 0 \Rightarrow \hat{d} = 0$

$$\left(\dot{\hat{x}}\right) = A\,\hat{x} + b\,u_{o2} + m\,\hat{i}_z$$

$$\hat{v}_o = q\hat{x} = 0$$

$$\hat{i}_g \;=\; u_{i2} \;=\; p\hat{x}$$

$$\left(\dot{\hat{x}}\right) \;=\; (sI-A)^{-1}bu_{o2} + \;(sI-A)^{-1}m\hat{i}_z$$

$$q\hat{x} \;=\; q(sI-A)^{-1}bu_{o2} \;+\; q(sI-A)^{-1}m\hat{i}_z \;=\; 0$$

$$Fu_{o2} \;+\; Z_o\hat{i}_z \;=\; 0 \;\Rightarrow\; \hat{i}_z \;=\; -\frac{F\;u_{o2}}{Z_o}$$

$$u_{i2} \;=\; p\hat{x} \;= p(sI-A)^{-1}bu_{o2} + p(sI-A)^{-1}m\hat{i}_z$$

$$\text{Define } Y_x \;= \frac{p(sI-A)^{-1}mF}{Z_o}$$

$$Y_n \;=\; Y_i \;-\; Y_x$$

$$Z_o'' \;=\; Z_o\frac{1+Z_s(Y_i-Y_x)}{1+Z_sY_i'}$$

4. Effect on Control Voltage Gain

$$G_v'' \;=\; \left[\frac{\hat{v}_o}{\hat{d}}\right]_{(Z_s=Z_s)} \;=\; \left[\frac{\hat{v}_o}{\hat{d}}\right]_{(\hat{v}_g=0\;;\,Z_s=0)}\frac{1+Z_sY_n}{1+Z_sY_d}$$

$$Y_n \;=\; \left(\frac{u_{i2}}{u_{o2}}\right)_{\hat{v}_g \;=\; 0\;;\;\hat{v}_o \;=\; 0}\;;$$

$$Y_d \;=\; \left(\frac{u_{i2}}{u_{o2}}\right)_{\hat{v}_g \;=\; 0\;;\;\hat{i}_z \;=\; 0\;;\;\hat{d} \;=\; 0}\;;$$

$$\left(\dot{\hat{x}}\right) \;=\; A\;\hat{x} \;+\; b\;(u_{o2}+\hat{v}_g) \;+\; f\;\hat{d}$$

$$\hat{v}_o \;=\; (q_1-q_2)X\hat{d} \;+\; q\;\hat{x}$$

$$\hat{i}_g \;=\; u_{i2} \;=\; (p_1-p_2)X\hat{d} \;+\; p\;\hat{x}$$

Y_d: $\quad \hat{v}_g \;=\; 0\;;\;\hat{d} \;=\; 0$

$$\hat{x} \;=\; (sI-A)^{-1}bu_{o2}$$

$$u_{i2} \;=\; p(sI-A)^{-1}bu_{o2} \;\Rightarrow\; Y_d \;=\; Y_i$$

Y_n: $\quad \hat{v}_o \;=\; 0\;;\hat{v}_g \;=\; 0\;;$

$$\left(\dot{\hat{x}}\right) \;=\; A\;\hat{x} \;+\; b\;u_{o2} \;+\; f\;\hat{d}$$

$$\hat{v}_o \;=\; (q_1-q_2)X\hat{d} \;+\; q\hat{x} \;=\; 0$$

$$u_{i2} \;=\; (p_1-p_2)X\hat{d} \;+\; p\hat{x}$$

$$\left(\dot{\hat{x}}\right) \;=\; (sI-A)^{-1}bu_{o2} + \;+\; (sI-A)^{-1}f\hat{d}$$

$$(q_1-q_2)X\hat{d} \;+\; q(sI-A)^{-1}bu_{o2} + q(SI-A)^{-1}f\hat{d} \;=\; 0$$

$$q(sI-A)^{-1}bu_{o2} \;=\; -\left((q_1-q_2)X + q(sI-A)^{-1}f\right)\hat{d}$$

$$Fu_{o2} \;= -\; G_v\hat{d} \;\Rightarrow\; \hat{d} \;=\; -\frac{F\;u_{o2}}{G_v}$$

$$u_{i2} \;=\; (p_1-p_2)X\hat{d} \;+\; p(sI-A)^{-1}bu_{o2} + p(sI-A)^{-1}f\hat{d}$$

$$\;=\; G_i\hat{d} + Y_iu_{o2} \;=\; -\frac{G_iFu_{o2}}{G_v} + Y_iu_{o2}$$

$$Y_n \;=\; Y_i \;-\; \frac{G_iF}{G_v} \;=\; -\frac{J}{U(s)}$$

$$G_v'' \;=\; G_v\frac{1-\dfrac{Z_sJ}{U(s)}}{1+Z_sY_i}$$

$$T'' \;=\; T\frac{1-\dfrac{Z_sJ}{U(s)}}{1+Z_sY_i}$$

5. Effect on Control Current Gain

$$G_i'' \;=\; \left[\frac{\hat{i}_g}{\hat{d}}\right]_{(Z_s=Z_s)} \;=\; \left[\frac{\hat{i}_g}{\hat{d}}\right]_{(\hat{v}_g=0\;;\,Z_s=0)}\frac{1+Z_sY_n}{1+Z_sY_d}$$

$$Y_n \;=\; \left(\frac{u_{i2}}{u_{o2}}\right)_{\hat{v}_g \;=\; 0\;;\;\hat{i}_g \;=\; 0}\;;$$

$$Y_d \;=\; \left(\frac{u_{i2}}{u_{o2}}\right)_{\hat{v}_g \;=\; 0\;;\;\hat{d} \;=\; 0}\;;$$

$$\left(\dot{\hat{x}}\right) \;=\; A\;\hat{x} \;+\; b\;(u_{o2}+\hat{v}_g) \;+\; f\;\hat{d}$$

$$\hat{v}_o \;=\; (q_1-q_2)X\hat{d} \;+\; q\;\hat{x}$$

$$\hat{i}_g \;=\; u_{i2} \;=\; (p_1-p_2)X\hat{d} \;+\; p\;\hat{x}$$

Y_d: $\quad \hat{v}_g \;=\; 0\;;\;\hat{d} \;=\; 0$

$$\hat{x} \;=\; (sI-A)^{-1}bu_{o2}$$

$$u_{i2} \;=\; p(sI-A)^{-1}bu_{o2} \;\Rightarrow\; Y_d \;=\; Y_i$$

Y_n: $\quad \hat{i}_g \;=\; 0\;;\;\hat{v}_g \;=\; 0;$

$$\left(\dot{\hat{x}}\right) \;=\; A\,\hat{x} \;+\; b\,u_{o2} \;+\; f\,\hat{d}$$

$$q\hat{x} \;=\; q(sI-A)^{-1}bu_{o2} + q(sI-A)^{-1}f\hat{d}$$

$$\hat{v}_o = (q_1-q_2)X\hat{d} \;+\; q(sI-A)^{-1}bu_{o2} + q(sI-A)^{-1}f\hat{d}$$

$$\hat{v}_o \;=\; Fu_{o2} \;+\; G_v\hat{d} \;=\; Fu_{o2} - G_vh\hat{v}_o$$

$$u_{i2} \;=\; \hat{i}_g \;=\; 0\;;\; Y_n \;=\; 0$$

$$G_i^{''} \;=\; G_i\frac{1}{1+Z_sY_i}$$

6. Effect of Input Filter on Converter Functions

$$F^{''} \;=\; F^{'}\frac{1}{1+Z_sY_i^{'}}$$

$$Y_i^{''} \;=\; Y_i^{'}\frac{1}{1+Z_sY_i^{'}}$$

$$Z_o^{''} \;=\; Z_o\frac{1+Z_s(Y_i-Y_x)}{1+Z_sY_i^{'}}$$

$$T^{''} \;=\; T\frac{1-\dfrac{Z_sJ}{U(s)}}{1+Z_sY_i^{'}}$$

$$G_i^{''} \;=\; G_i\frac{1}{1+Z_sY_i}$$

6.5 Design Criteria For Selection of Input Filter

It may be seen from the denominators of the above expressions, it is necessary that

$$\left|\frac{Z_s}{Z_i^{'}}\right| \;<\; 1\;;\; \left|\frac{Z_s}{Z_i}\right| \;<\; 1\;;\text{ for stability.}$$

Notice that the second inequality is more stringent. Further

$$\left|\frac{Z_s}{Z_i}\right| \;<<\; 1\;;\; \left|\frac{Z_sJ}{u(s)}\right| \;<\; 1\;;\text{ for loop gain to be unaffected.}$$

6.5.1 Design Example

Consider the circuit shown in Fig.9. It consists of a simple buck converter supplied from a source through an LC filter. The component values are as follows.

$$R_l \;=\; 0.5\;\Omega\;;\; R_c \;=\; 0.1\;\Omega\;;\; R \;=\; 20\;\Omega\;;\; L \;=\; 82\;mH\;;$$
$$C \;=\; 19\;\mu F\;;\; D \;=\; 0.7\;\;;\; f_s \;=\; 100\;kHz\;;$$

The system matrices are

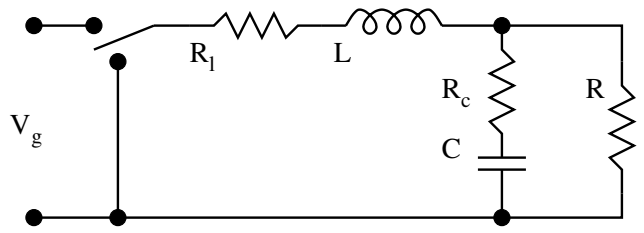

Figure 6.9: A Buck Converter

$$A = A_1 = A_2 = \begin{pmatrix} -\frac{R_1 + R||R_c}{L} & -\frac{R}{(R+R_c)L} \\ \frac{R}{(R+R_c)C} & -\frac{1}{(R+R_c)C} \end{pmatrix}$$

$$b_1 = \begin{pmatrix} \frac{1}{L} \\ 0 \end{pmatrix}; b_1 = \begin{pmatrix} 0 \\ 0 \end{pmatrix}; b = \begin{pmatrix} \frac{D}{L} \\ 0 \end{pmatrix};$$

$$m_1 = m_2 = m = \begin{pmatrix} 0 \\ \frac{1}{C} \end{pmatrix};$$

$$p_1 = \begin{pmatrix} 1 & 0 \end{pmatrix}; p_2 = \begin{pmatrix} 0 & 0 \end{pmatrix}; p = \begin{pmatrix} D & 0 \end{pmatrix};$$

$$q_1 = q_2 = q = \begin{pmatrix} R||R_c & \frac{R}{R+R_c} \end{pmatrix};$$

$$f = (A_1 - A_2)X + (b_1 - b_2)V_g = \begin{pmatrix} \frac{V_g}{L} \\ 0 \end{pmatrix};$$

Define

$$\alpha = \frac{R}{R+R_c}\ ;\ \beta = \frac{R_l}{R}\ ;\ \gamma = \frac{R_c}{R}\ ;$$

$$A = \begin{pmatrix} -\frac{R(\beta+\alpha\gamma)}{L} & -\frac{\alpha}{L} \\ \frac{\alpha}{C} & -\frac{\alpha}{(RC} \end{pmatrix}$$

$$(sI-A)^{-1} = \frac{1}{\omega_o^2\left(1 + \frac{s}{Q\omega_o} + \frac{s^2}{\omega_o^2}\right)} \begin{pmatrix} s + \frac{\alpha}{RC} & -\frac{\alpha}{L} \\ \frac{\alpha}{C} & s + \frac{R(\beta+\alpha\gamma)}{L} \end{pmatrix}$$

$$\omega_o^2 = \frac{\alpha(\alpha+\beta+\alpha\gamma)}{LC}\ ;\ \frac{\omega_o}{Q} = \frac{\alpha}{RC} + \frac{R(\beta+\alpha\gamma)}{L}\ ;$$

Input Admittance: Define $D_s = 1 + \frac{s}{Q\omega_o} + \frac{s^2}{\omega_o^2}$

$$Y_i = p[sI - A]^{-1}b = \frac{D^2(s + \alpha/RC)}{\omega_o^2 LD_s}$$

$$Y_i = \frac{D^2\alpha}{R\omega_o^2 LC}\frac{1 + sCR/\alpha}{D_s}$$

$$Y_i = K_1\frac{1 + s/\omega_1}{1 + \frac{s}{Q\omega_o} + \frac{s^2}{\omega_o^2}}$$

$$Z_i = K\frac{1 + \frac{s}{Q\omega_o} + \frac{s^2}{\omega_o^2}}{1 + s/\omega_1}\ ;$$

$$K \ \Rightarrow\ 32\ dB\ ; Q\ \Rightarrow\ 7\ dB\ ;\ \omega_1\ \Rightarrow\ 416\ Hz\ ;\ \omega_o\ \Rightarrow\ 4072\ Hz$$

The bode plot of is shown in Fig.10. Consider the input filter shown in

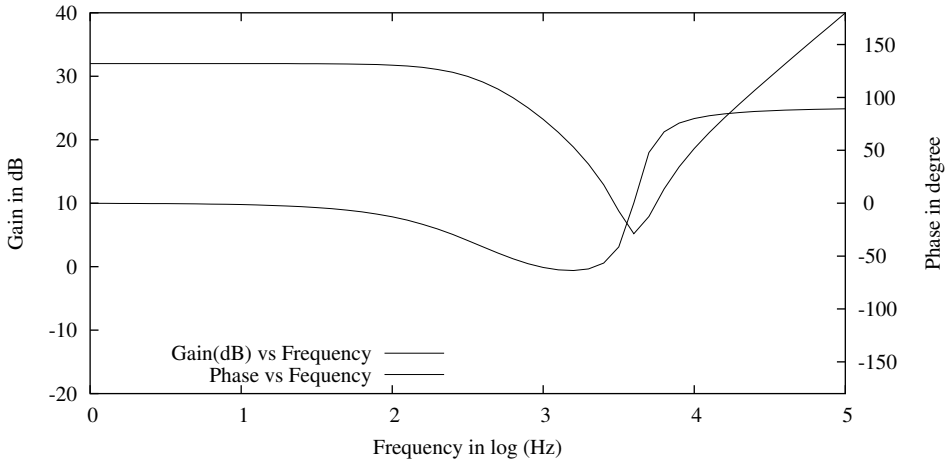

Figure 6.10: The Input Impedance of the Buck Converter

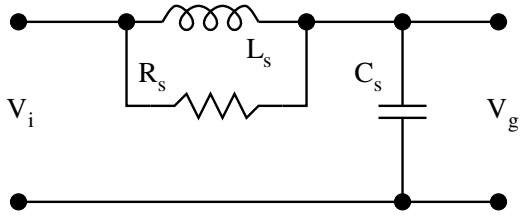

Figure 6.11: The Input Filter

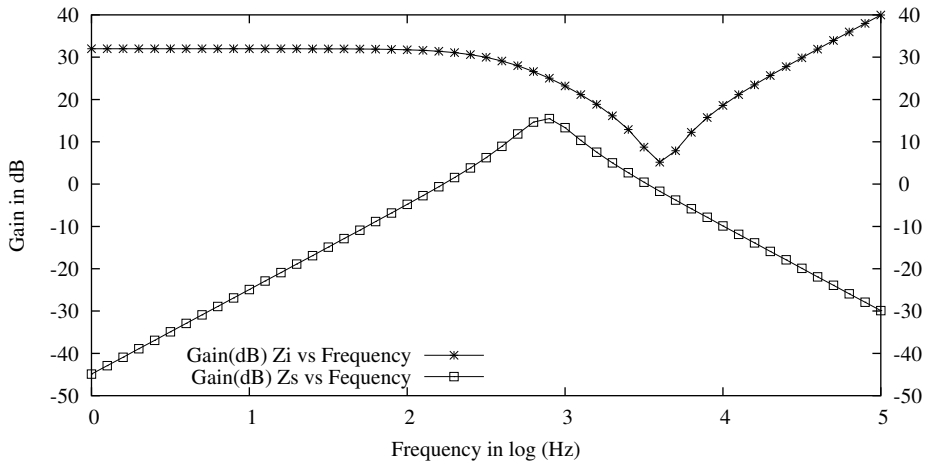

Figure 6.12: The Criterion for Input Filter Design

Fig. 11. ($L_s = 900\ \mu H$; $C_s = 50\ \mu F$; $R_s = 6\ \Omega$). The input impedance of the input filter is,

$$Z_s = \frac{sL_s}{1 + \frac{sL_s}{R_s} + s^2 L_s C_s}\ ;$$

$$Z_s = \frac{s/\omega_z}{1 + \frac{s}{Q_s\omega_s} + \frac{s^2}{\omega_s^2}}\ ;$$

$$\omega_z\ \Rightarrow\ 176\ Hz\ ;\ \omega_s\ \Rightarrow\ 750\ Hz\ ;\ Q_s\ \Rightarrow\ 3\ dB\ ;$$

The plot of the source impedance is shown in Fig. 12. It may be seen that in the the entire frequency range, the inequality Z_s/Z_i is satisfied ensuring stability.

There are several controller ICs available in the market. Some of the commercially available controller ICs are given in the following links.

Advanced pulsewidth modulator

Advanced pulsewidth modulator

Voltage mode PWM controller

General purpose PWM controller

6.6 Problem Set

1. The following compensator is required for the closed loop control of a converter.

$$h(s) = 0.5\frac{1 + s/\omega_1}{1 + s/\omega_2} \qquad \omega_1 \Rightarrow 1000Hz;\ \omega_2 \Rightarrow 20000Hz$$

The circuit shown in Fig. P1 realizes the compensator. The opamp used

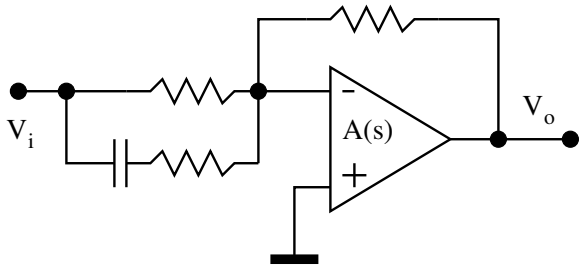

Fig. P 6.1: Closed Loop Compensator

is $\mu A741$ which has a transfer function of

$$A(s) = 10^5\frac{1}{1 + s/\omega} \qquad \omega \Rightarrow 10Hz\ ;$$

If the phase error of the compensator is not to exceed 15° compared to ideal realization, estimate the range of frequencies in which the above compensator may be used. Hint: Use graphical method

2. Consider the converter shown in Fig. 2 operating at a duty ratio of around 0.5 in CCM. It is desired to design an input RC filter for the converter as shown in the Fig. 2. Evaluate the values of R_s and C_s such that the converter is immune to input filter induced oscillations. Comment on the consequences of the input filter on the operation of the converter. Hint: Use Graphical Method.

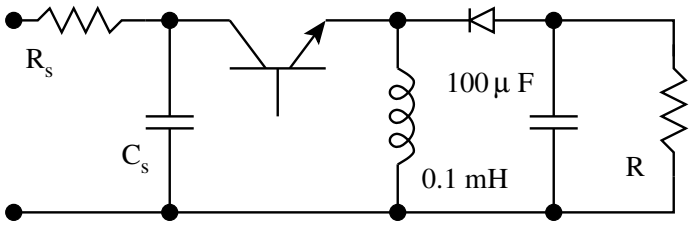

Fig. P 6.2: Flyback Converter with Input Filter

3. It is desired to design a compensator with the transfer function H(s) for a converter.

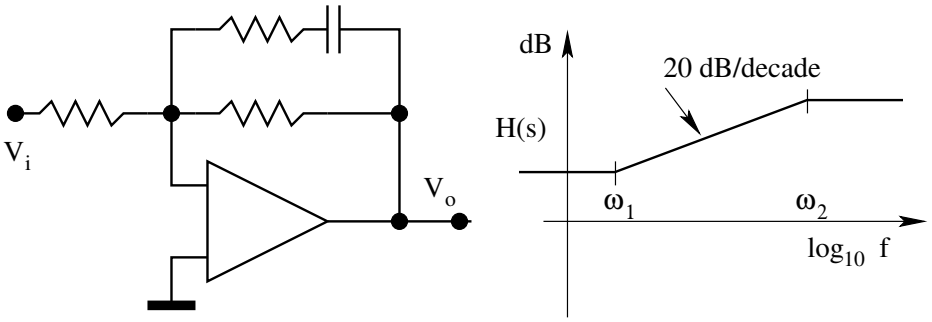

Fig. P 6.4: A Lead Lag Compensation

$$H(s) \;=\; -25\frac{1+s/2\pi 600}{s/2/pi600}$$

Design the compensator circuit using the ideal opamp.

4. Is it possible to obtain the gain shown in Fig. (4b) with the circuit shown in Fig. (4a)

5. Figure 5 shows a PI controller and its asymptotic magnitude bode plot. Select R_1, R_2, and C.

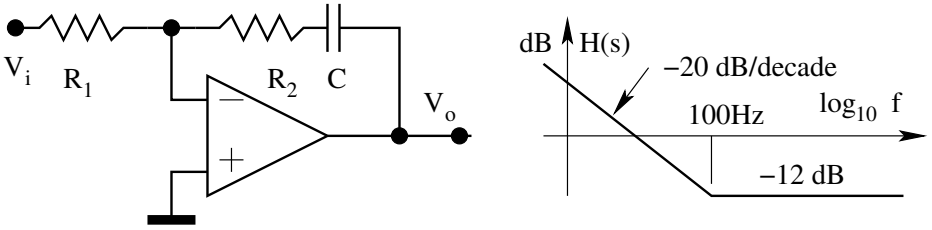

Fig. P 6.5: A PI Compensator

6. A closed loop controlled converter has a bandwidth of 100Hz and a phase margin of 90°. Estimate the transient settling time for the converter.

7. Table P7 shows the control of output $(\hat{v}/\hat{d})$ frequency response of a fly back converter obtained through actual measurement. The frequency-gain table is given below.

   (A) Write down the approximate control transfer function of the converter.

   (B) Design a suitable feed back controller for this converter to realise a bandwidth above 750 Hz and steady-state accuracy above 99%.

Table P 6.7: Frequency Response Measurements

Sl No.	Frequency (Hz)	Gain (dB)
1	20	18
2	40	18
3	60	21
4	80	23
5	100	16.5
6	200	4
7	400	-7
8	600	-12.5
9	1000	-20
10	2000	-28
11	4000	-35

8. Fig. 8 shows the block diagram of a closed loop controlled converter. The converter has a transfer function of

$$G(s) = \frac{40}{\left(1 + \frac{2s}{100\pi} + \frac{s^2}{(100\pi)^2}\right)}$$

The compensator has a transfer function of

$$H(s) = \frac{1 + \frac{s}{100\pi}}{\left(1 + \frac{s}{4000\pi}\right)}$$

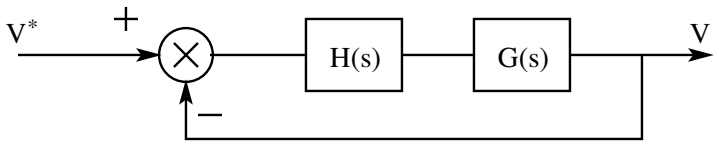

Fig. P 6.8: A Closed Loop Controller

(A) Sketch the asymptotic gain bode plot of G(s)

(B) Sketch the asymptotic gain bode plot of H(s)

(C) Sketch the asymptotic gain bode plot of G(s)H(s)

(D) Will the closed loop control be stable?

(E) What is the phase margin of the controller?

(F) What is the closed loop bandwidth of the controller?

(G) What is the steady state error (%) of the controller?

9. Fig. 9 shows the block diagram of a closed loop controlled converter. The converter has a transfer function of

$$G(s) = 40\frac{1 - \frac{s}{4000\pi}}{\left(1 + \frac{2s}{80\pi} + \frac{s^2}{(80\pi)^2}\right)}$$

The compensator has a transfer function of

$$H(s) = \frac{1 + \frac{s}{80\pi}}{\left(1 + \frac{s}{4000\pi}\right)}$$

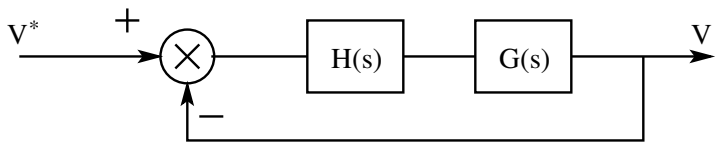

Fig. P 6.9: A Closed Loop Controller

(A) Sketch the asymptotic gain bode plot of G(s)

(B) Sketch the asymptotic gain bode plot of H(s)

(C) Sketch the asymptotic gain bode plot of G(s)H(s)

(D) Will the closed loop control be stable?

(E) What is the phase margin of the controller?

(F) What is the closed loop bandwidth of the controller?

(G) What is the steady state error (%) of the controller?

10. An SMPS has open loop audio susceptibility (F) transfer function with parameters (dc gain = 0.1; a complex pole pair with a Q of 5 at 150 Hz). The converter has a closed loop controller with a bandwidth of 1500 Hz ($T = 2000\pi/s$).

(A) Sketch the asymptotic bode plot (magnitude plot only) of audio susceptibility.

(B) Sketch the asymptotic loop gain (magnitude plot only) of the controller.

(C) Sketch the closed loop audio-susceptibility (magnitude plot only) of the converter.

(D) Write down the gain provided by the converter for 300 Hz ripple at input both in magnitude and phase.

11. A boost converter operating in discontinuous conduction has an open loop gain of

$$\frac{\hat{v}_o}{\hat{d}} = \frac{40}{1 + \frac{s}{500}}$$

For closed loop control a PI controller is chosen. The closed loop bandwidth required is 5000 rad/sec. Steady state accuracy required is better than 1%. Design a suitable compensator and give its normalized transfer function.

12. The push pull converter shown in Fig.12 is operated in current control mode. The control transfer function for the converter is as follows.

$$G(s) = \frac{V_o(s)}{V_c(s)} = \frac{15}{\left(1 + \frac{s}{2\pi 75}\right)\left(1 + \frac{s}{2\pi 16000}\right)}$$

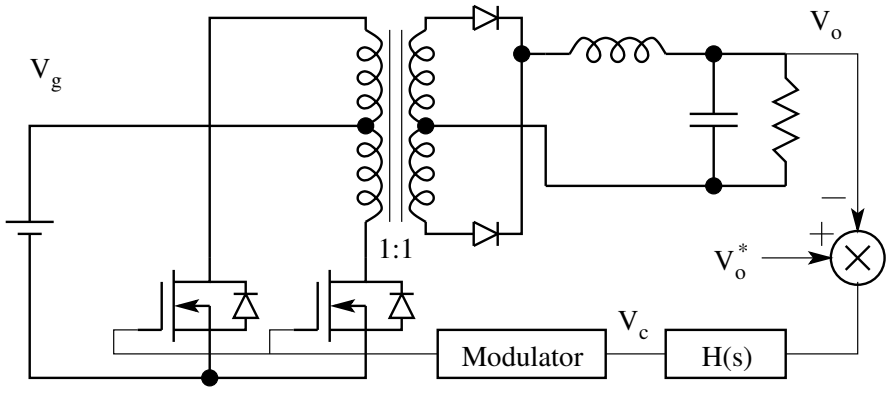

Fig. P 6.12: A Push-Pull Converter

(A) Design a closed loop controller H(s) in order to obtain a bandwidth of 2000Hz and a steady state accuracy of better than 1%.

(B) Express H(s) as a normalized function.

(C) Show an analogue circuit realization of H(s).

13. Figure 13a shows the boost converter. Figure 13b gives the small signal linear model of the same. You may verify that the small signal audio susceptibility gain is given by

$$\frac{\hat{v}_o(s)}{\hat{v}_g(s)} = \frac{R}{(1-D)(R+sL_e)} \; ; \; L_e = \frac{L}{(1-D)^2}$$

Figure 13c gives the same circuit with an additional capacitor with ESR

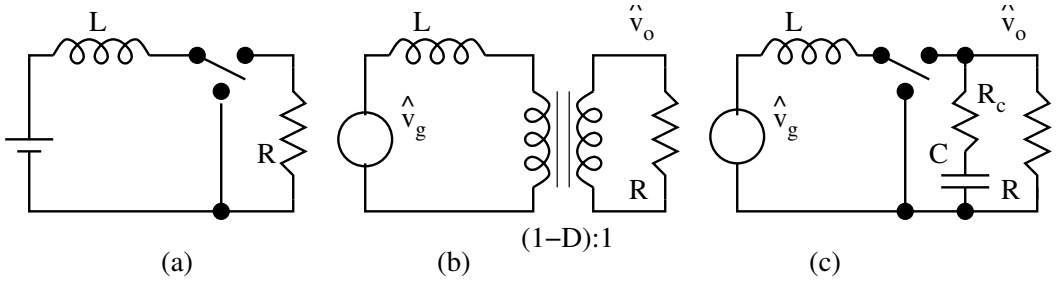

Fig. P 6.13: A Boost Converter

$(C+R_c)$ connected across the load. Apply the extra element theorem and evaluate the corrected audio susceptibility function with the new elements in the circuit.

14. A switched mode converter has an input (Z_i) impedance given by the following function.

$$Z_i = 10\frac{1 + \dfrac{s}{1000\pi} + \dfrac{s^2}{(200\pi)^2}}{1 + \dfrac{s}{20\pi}}$$

Figure 14 shows the input filter employed with the source for this con-

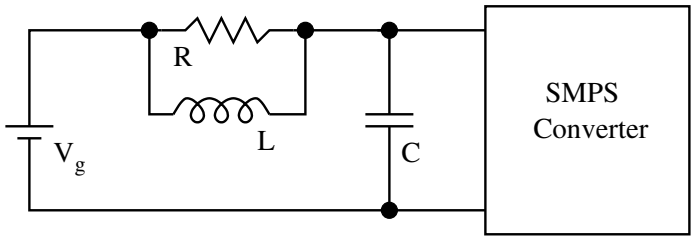

Fig. P 6.14: Converter with Input Filter

verter.

(A) Plot the input impedance of the SMPS converter in the form of a bode plot and mark the salient features of the function Z_i.

(B) Apply the appropriate design criteria and evaluate L, C, and R of the source filter.

Chapter 7

Current Programmed Control of DC to DC Converters

7.1 Introduction

We have seen the control of PWM converters where the duty ratio is controlled in proportion to a control input V_c. Schematically this method of control is represented by the schematic shown in Fig. 1. Such a method is called 'duty ratio programmed control' and is quite popular. A number of special purpose IC's (such as 3524, 494, etc) are available for this purpose from a number of IC manufacturers. Another popular method of control of PWM

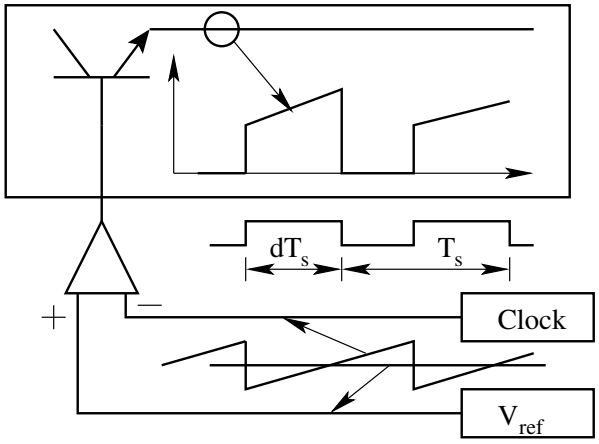

Figure 7.1: Structure of the Duty Ratio Controller

converters is called the constant frequency current programmed (or simply current programmed) control. In this method of control, the turn-on instants of the switch is clocked periodically, and the turn-off instants are determined by the times at which the switch current reaches the threshold value determined by the control signal . The scheme is illustrated in Fig. 2. It can be seen

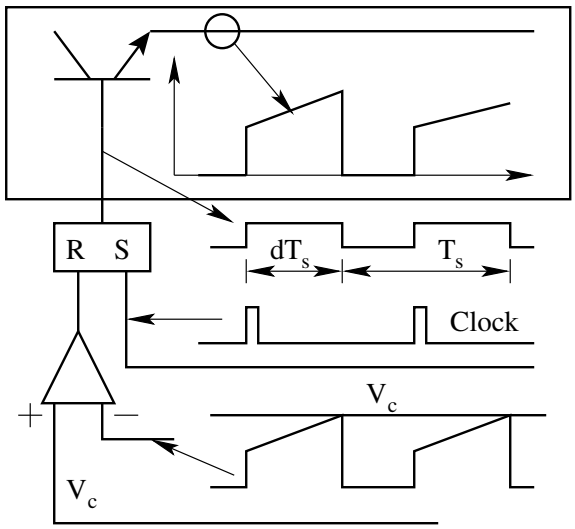

Figure 7.2: Structure of the Current Programmed Controller

from the schematic that there is a local feedback loop. This is on account of the current through the switch in turn determining the duty ratio. There are several advantages in such a control scheme.

1. The switch (usually an electronic device) is turned off when its current reaches a set level. Failure to excessive switch current can be prevented by simply limiting the maximum value of the control signal V_c. Such a scheme will protect the entire converter from overloads.

2. Several converters can be operated in parallel without a load-sharing problem, because all of the power switches receive the same control signal from the regulator feedback circuit and carry the same maximum current.

3. Current programmed control, since it establishes a constant switch (peak inductor current) current, effectively eliminates the inductor current as a state variable of the converter. The overall order of the converter then reduces by 1, resulting in a simpler gain function.

The stated advantages are shown in Fig.3. There is however an accompanying disadvantages in the current programmed control.

7.2 Sub-harmonic Instability in Current Programmed Control

The local feedback in the control scheme introduces instability when the duty ratio exceeds 0.5. This instability on account of the local feedback can best be understood graphically. This effect can be explained with the help of the

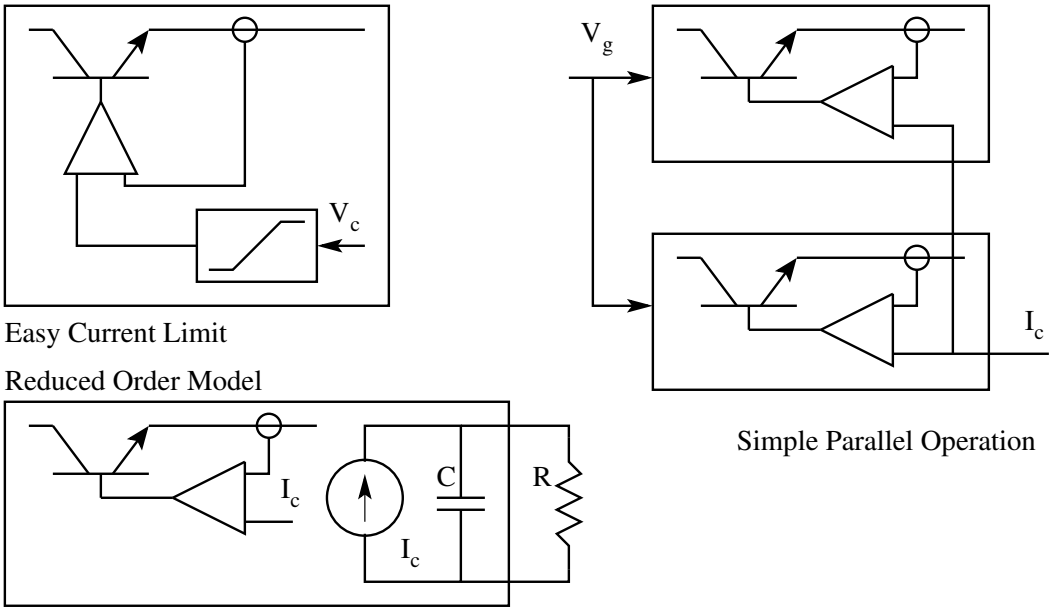

Figure 7.3: Advantages of Current Programmed Control

steady state inductor current waveform shown in Fig. 4. This inductor current is represented by straight lines in each of the intervals DT_s and $(1-D)T_s$ and since the switching frequency is very much higher than the system time constants. The control signal I_c indicating the current threshold is also shown. Suppose that the inductor current has a rising slope of m_1 and falling slope of m_2,

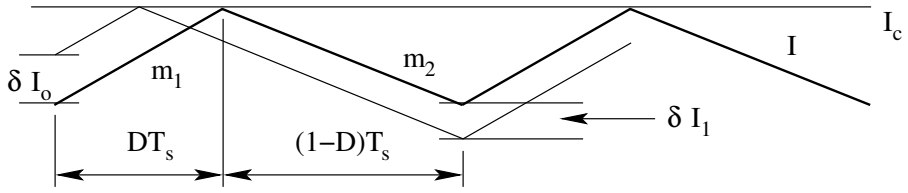

Figure 7.4: Stability of Operating Point in Current Programmed Control

$$\frac{m_2}{m_1} = \frac{D}{1-D} \tag{7.1}$$

If there is a perturbation, relative to the steady state, of δI_o in the inductor current at the beginning of the cycle, the waveform shows that after one period the perturbation will propagate to δI_1.

$$\delta I_1 = -\frac{m_2}{m_1}\delta I_o \tag{7.2}$$

Thus after n cycles, the error will be,

$$\delta I_n = \left(-\frac{D}{1-D}\right)^n \delta I_o \tag{7.3}$$

Clearly the steady state is not stable for $D > 0.5$.

7.2.1 Compensation to Overcome Sub-harmonic Instability

This potential instability can be eliminated by the addition of a suitable periodic ramp to either the switch current waveform or to the control signal. Waveforms for this modification are shown in Fig. 5, in which a control signal is given a periodic falling slope $-m_c$. An argument similar to that used

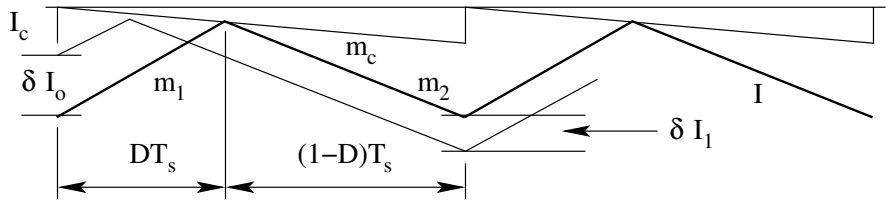

Figure 7.5: Compensating Slope in Current Programmed Control

previously shows that now a perturbation is carried into δI_n after n cycles.

$$\delta I_n = \left(-\frac{m_2 - m_c}{m_2 + m_c}\right)^n \delta I_o \tag{7.4}$$

A suitable choice of the ramp slope m_c can thus cause this perturbation to die out even if the duty ratio is more than 0.5. In particular if m_c is chosen to be equal to m_2, the magnitude of the falling current slope, any perturbation in inductor current will disappear at the end of one cycle. Thus selection of the stabilising ramp enables inner loop stability and simultaneously provides the fastest possible transient response as shown in Fig. 6.

Note that for duty ratios less than 0.5, the control is stable. While the

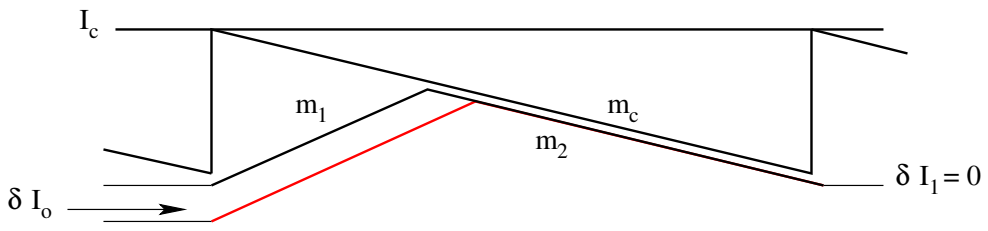

Figure 7.6: With $m_c = m_2$, correction is over in one cycle

system is stable (for $D < 0.5$) in the absence of a stabilizing ramp, even

in these situations the best possible transient response is obtained only if a compensating ramp of correct slope is used. Thus the compensating ramp performs the dual functions of enhancing the inner loop stability and improving the transient recovery. The same result may be obtained if a ramp of slope m_c is added to the switch current instead of being subtracted from the control signal. Two more points of practical interest are as follows. If the switch current is monitored with a transformer, its magnetizing current acts as a destabilising ramp. Hence in the absence of compensating ramp, the minimum value of duty ratio for which the oscillation occurs is less than 0.5. Likewise the compensating ramp has to be adjusted to compensate for this additional influence. The second point is that the slope may change with operating conditions. In this case if a fixed compensating ramp is used the compensation will be perfect only at one operating point. In such cases sophisticated ramps might be used to achieve compensation.

7.3 Determination of Duty Ratio for Current Programmed Control

We have already developed the small signal models for various converters based on the duty ratio control $\hat{d}$. If we can relate the current programmed control to an equivalent duty ratio programmed control, the earlier results can be readily used for the small signal model of the converters. This may be readily achieved with the help of Fig. 7.

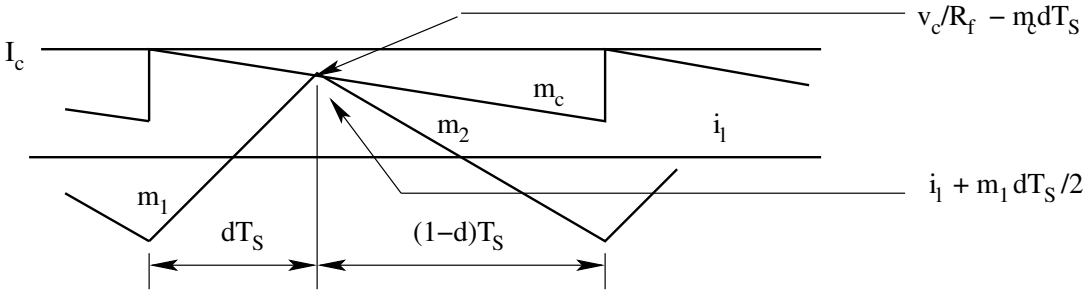

Figure 7.7: Development of Dynamic Model for Current Controller

$$i_1 + m_1 \frac{dT_s}{2} = \frac{V_c}{R_f} - m_c \; d \; T_s \tag{7.5}$$

The dc and small signal ac relations are found by setting,

$$d = D + \hat{d} \; ; \; i_l = I_l + \hat{i}_l \; ; \; v_c = V_c + \hat{v}_c \; ; \; m_1 = M_1 + \hat{m}_1 \tag{7.6}$$

The compensating ramp is constant.

$$m_c = M_c \tag{7.7}$$

$$D = \frac{KR}{nM_1L}\left[\frac{V_c}{R_f} - I_l\right] \tag{7.8}$$

From the above dc and ac relations for d are as follows.

$$\hat{d} = \frac{KR}{nM_1L}\left[\frac{\hat{v}_c}{R_f} - \hat{i}_l\right] - \frac{D}{nM_1}\hat{m}_1 \tag{7.9}$$

$K = \dfrac{2L}{RT_s}$ = conduction parameter of the converter.

$R = \dfrac{V_o}{I_o}$ = Output load resistance on the converter.

$n = 1 + \dfrac{2M_c}{M_1}$ = compensation ratio of the current control.

$n = 1$ for no compensation.

$n = \dfrac{1+D}{1-D}$ for optimum compensation $M_c = M_2$

The above results apply to any converter. However, the dependence of the inductor current ramp m_1 on the operating conditions is different for different converters. The relationship between $\hat{d}$ and the control input $\hat{v}_c$ and other parameters of the converter for three different basic converters are given in the following sections.

7.3.1 Buck Converter

During the switch-on interval, the inductor is connected between the line input and dc output (v_g and v_o).

$$m_1 = \frac{v_g - v_o}{L} \tag{7.10}$$

The dc conversion ratio is $V_o = DV_g$

$$M_1 = \frac{V_o(1-D)}{DL} \; and \; \hat{m}_1 = \frac{\hat{v}_g - \hat{v}_o}{L} \tag{7.11}$$

$$\hat{d} = \frac{KRD}{n(1-D)V_o}\left[\frac{\hat{v}_c}{R_f} - \hat{i}_l\right] - \frac{D^2}{n(1-D)V_o}\hat{v}_g + \frac{D^2}{n(1-D)V_o}\hat{v}_o \tag{7.12}$$

7.3.2 Boost Converter

During the switch-on interval, the inductor is connected across the line input v_g

$$m_1 = \frac{v_g}{L} \tag{7.13}$$

(13) The dc conversion ratio is $V_o = V_g/(1-D)$

$$M_1 = \frac{V_o(1-D)}{L} \; and \; \hat{m}_1 = \frac{\hat{v}_g}{L} \tag{7.14}$$

$$\hat{d} = \frac{KR}{n(1-D)V_o}\left[\frac{\hat{v}_c}{R_f} - \hat{i}_l\right] - \frac{D}{n(1-D)V_o}\hat{v}_g \tag{7.15}$$

7.3.3 Buck-Boost Converter

During the switch-on interval, the inductor is connected across the line input v_g

$$m_1 = \frac{v_g}{L} \tag{7.16}$$

The dc conversion ratio is $V_o = DV_g/(1-D)$

$$M_1 = \frac{V_o(1-D)}{DL} \; and \; \hat{m}_1 = \frac{\hat{v}_g}{L} \tag{7.17}$$

$$\hat{d} = \frac{KR}{n(1-D)V_o}\left[\frac{\hat{v}_c}{R_f} - \hat{i}_l\right] - \frac{D^2}{n(1-D)V_o}\hat{v}_g \tag{7.18}$$

The parameter n is a function of the compensating ramp M_c. If $M_c = M_2$, then $n = (1+D)/(1-D)$. If no compensating ramp is used, then $n = 1$. Therefore for all three converters, n is between unity for zero compensating ramp and $(1+D)/(1-D)$ for optimum compensating ramp. The above equations show the relationship between $\hat{d}$ and the other parameters for different converters. We may substitute for $\hat{d}$ in the standard small signal state space model in terms of $\hat{v}_g$, $\hat{v}_o$, $\hat{v}_c$, $\hat{i}_l$, and obtain the necessary (control and input) transfer functions of the converter. These transfer functions may then be used to design a compensator for closing the voltage loop for the overall converter. The control transfer functions of the basic converters are given in the following sections.

7.4 Transfer Functions

7.4.1 Buck Converter

In the duty-programmed mode of control, in continuous conduction, the small signal description of buck converter is

$$\dot{\hat{x}} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \hat{x} + \begin{bmatrix} \frac{D}{L} \\ 0 \end{bmatrix} \hat{v}_g + \begin{bmatrix} \frac{V_g}{L} \\ 0 \end{bmatrix} \hat{d} \tag{7.19}$$

With current programmed control,

$$\hat{d} = \frac{KRD}{n(1-D)V_o}\left[\frac{\hat{v}_c}{R_f} - \hat{i}_l\right] - \frac{D^2}{n(1-D)V_o}\hat{v}_g + \frac{D^2}{n(1-D)V_o}\hat{v}_o \tag{7.20}$$

We may substitute for $\hat{d}$ in the above equation to get the state equation under current programmed control.

$$\dot{\hat{x}} = \begin{bmatrix} -\frac{R_d}{L} & -\frac{a}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \hat{x} + \begin{bmatrix} \frac{bD}{L} \\ 0 \end{bmatrix} \hat{v}_g + \begin{bmatrix} \frac{R_d}{LR_f} \\ 0 \end{bmatrix} \hat{v}_c \tag{7.21}$$

Where

$$R_d = \frac{KR}{n(1-D)}$$
$$a = 1 - \frac{D}{n(1-D)}$$
$$b = 1 - \frac{1}{n(1-D)}$$

Notice the structure of the system matrix. The converter behaves as if the inductor in the circuit is L/a, and the parasitic resistance in the circuit is R_d/a. In other words, the current programming introduces extra damping in the system so that the system poles are now real.

n may be defined as the degree of compensation. n varies from 1 for no compensation to $(1 + D)/(1 - D)$ for optimum compensation. R_d may be defined as the loss-less damping resistance in the system. R_d varies from $KR/(1-D)$ for no compensation to $KR/(1+D)$ for optimum compensation. K is the conduction parameter of the converter and is usually more than 1 for CCM. R_d therefore is greater than R. a varies in the range of $(1-2D)/(1-D)$ for no compensation $1/(1 + D)$ for full compensation. a is therefore positive and less than 1.

From the above equations, the transfer functions of the converter may be readily found out.

$$[sI - A] = \begin{bmatrix} s + \frac{R_d}{L} & \frac{a}{L} \\ -\frac{1}{C} & s + \frac{1}{RC} \end{bmatrix} \tag{7.22}$$

The characteristic polynomial of the converter is

$$s^2 + s\left(\frac{R_d}{L} + \frac{1}{RC}\right) + \frac{a}{LC} + \frac{R_d}{RLC} \tag{7.23}$$

$$s^2 + s\left(\frac{R_d}{L} + \frac{1}{RC}\right) + \frac{a + \frac{K}{n(1-D)}}{LC} \tag{7.24}$$

Since $a < 1$, and $K/n(1-D) > 1$, the above polynomial may be approximated

as follows

$$s^2 + s\left(\frac{R_d}{L} + \frac{1}{RC}\right) + \frac{\dfrac{K}{n(1-D)}}{LC} \tag{7.25}$$

$$s^2 + s\left(\frac{R_d}{L} + \frac{1}{RC}\right) + \frac{R_d}{RLC} \;=\; \left(s + \frac{R_d}{L}\right)\left(s + \frac{1}{RC}\right) \tag{7.26}$$

The system poles are seen to be real. This is the effect of current programming, which introduces loss-less damping in the system to break the complex conjugate pole pair of the original system into two real poles. The state control transfer function and the two output transfer functions may be readily computed.

$$\frac{\hat{x}(s)}{\hat{v}_c(s)} \;=\; \frac{1}{\left(s + \dfrac{R_d}{L}\right)\left(s + \dfrac{1}{RC}\right)} \begin{bmatrix} \left(s + \dfrac{1}{RC}\right) & -\dfrac{a}{L} \\ \dfrac{1}{C} & \left(s + \dfrac{R_d}{L}\right) \end{bmatrix} \begin{bmatrix} \dfrac{R_d}{LR_f} \\ 0 \end{bmatrix} \tag{7.27}$$

$$\frac{\hat{i}_l(s)}{\hat{v}_c(s)} \;=\; \frac{1}{R_f\left(1 + \dfrac{sL}{R_d}\right)} \tag{7.28}$$

$$\frac{\hat{v}_o(s)}{\hat{v}_c(s)} \;=\; \frac{R}{R_f}\frac{1}{\left(1 + \dfrac{sL}{R_d}\right)(1 + sCR)} \tag{7.29}$$

The current transfer function is a single pole transfer function with a bandwidth of $\omega_c = R_d/L$.

$$f_c = \frac{R_d}{2\pi L} = \frac{KR}{2\pi n(1-D)L} = \frac{2L}{RT_s}\frac{R}{2\pi n(1-D)L} = \frac{f_s}{\pi n(1-D)} \tag{7.30}$$

When n varies from 1 to $(1+D)/(1-D)$, the current loop bandwidth varies in the range of

$$\frac{f_s}{6} \;\le\; f_c \;\le\; \frac{2f_s}{3} \tag{7.31}$$

The minimum value of current loop bandwidth is one sixth of the switching frequency. This is obtained with optimum ramp compensation. The next transfer function of importance is

$$\frac{\hat{v}_o(s)}{\hat{v}_c(s)} \;=\; \frac{K_v}{\left(1 + \dfrac{sL}{R_d}\right)(1 + sCR)} \;;\; K_v \;=\; \frac{R}{R_f} \tag{7.32}$$

From this transfer function, the feedback compensator design for the control of the output voltage of the converter may be designed.

7.4.2 Boost Converter

With current programming, the boost converter system equations are represented by

$$\hat{\dot{x}} = A\hat{x} + b\hat{v}_g + f^*\hat{v}_c \tag{7.33}$$

$$A = \begin{bmatrix} -\dfrac{R_d}{L} & -\dfrac{1-D}{L} \\ \dfrac{1-D}{C} - \dfrac{R_d}{(1-D)RC} & -\dfrac{1}{RC} \end{bmatrix};$$

$$b = \begin{bmatrix} -\dfrac{a}{L} \\ \dfrac{-D}{nRC(1-D)^2} \end{bmatrix}; \; f^* = \begin{bmatrix} -\dfrac{R_d}{LR_f} \\ \dfrac{R_d}{RCR_f(1-D)} \end{bmatrix};$$

With similar approximations as carried out for the buck converter, the transfer functions are

$$\frac{\hat{i}_l(s)}{\hat{v}_c(s)} = \frac{2}{R_f} \frac{1 + \dfrac{sCR}{2}}{\left(1 + \dfrac{sL}{R_d}\right)(1 + sCR)} \tag{7.34}$$

$$\frac{\hat{v}_o(s)}{\hat{v}_c(s)} = \frac{(1-D)R}{R_f} \frac{1 - \dfrac{sL}{R(1-D)^2}}{\left(1 + \dfrac{sL}{R_d}\right)(1 + sCR)} \tag{7.35}$$

7.4.3 Buck-Boost Converter

With current programming, the buck-boost converter system equations are represented by

$$\hat{\dot{x}} = A\hat{x} + b\hat{v}_g + f^*\hat{v}_c \tag{7.36}$$

$$A = \begin{bmatrix} -\dfrac{R_d}{L} & -\dfrac{1-D}{L} \\ \dfrac{1-D}{C} - \dfrac{R_d}{(1-D)RC} & -\dfrac{1}{RC} \end{bmatrix};$$

$$b = \begin{bmatrix} -\dfrac{aD}{L} \\ \dfrac{-D^2}{nRC(1-D)^2} \end{bmatrix}; \; f^* = \begin{bmatrix} -\dfrac{R_d}{LR_f} \\ \dfrac{DR_d}{RCR_f(1-D)} \end{bmatrix};$$

With similar approximations as carried out for the buck converter, the transfer functions are

$$\frac{\hat{i}_l(s)}{\hat{v}_c(s)} = \frac{1+D}{R_f} \frac{1+\dfrac{sCR}{1+D}}{\left(1+\dfrac{sL}{R_d}\right)(1+sCR)} \tag{7.37}$$

$$\frac{\hat{v}_o(s)}{\hat{v}_c(s)} = \frac{(1-D)R}{R_f} \frac{1-\dfrac{sL}{R(1-D)^2}}{\left(1+\dfrac{sL}{R_d}\right)(1+sCR)} \tag{7.38}$$

The Bode plot of the control transfer functions (programmed current and

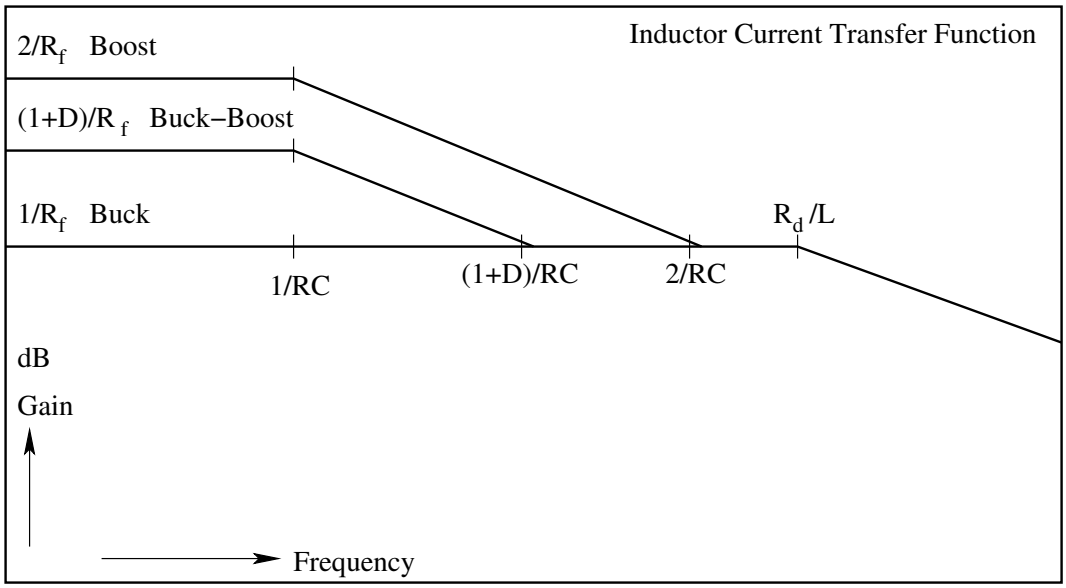

Figure 7.8: Inductor Current Control Transfer Function

output voltage) are shown in Figs. 8 & 9. The following conclusions may be drawn from the Bode plots.

- The dominant pole of the output transfer function is a function of R and C ($\omega_1 = 1/RC$).
- The output transfer function has a high frequency pole at ω_c. This high frequency pole is the same for all three types of converters, the value of which depends on the degree of compensation used. Its lower bound is about 1/6th the switching frequency ($f_c \geq f_s/6$).
- The boost and buck converters exhibit a rhp zero ω_z. (The same as found in duty ratio programmed control). Usually this rhp zero will be between the two frequencies f_1 and f_c.

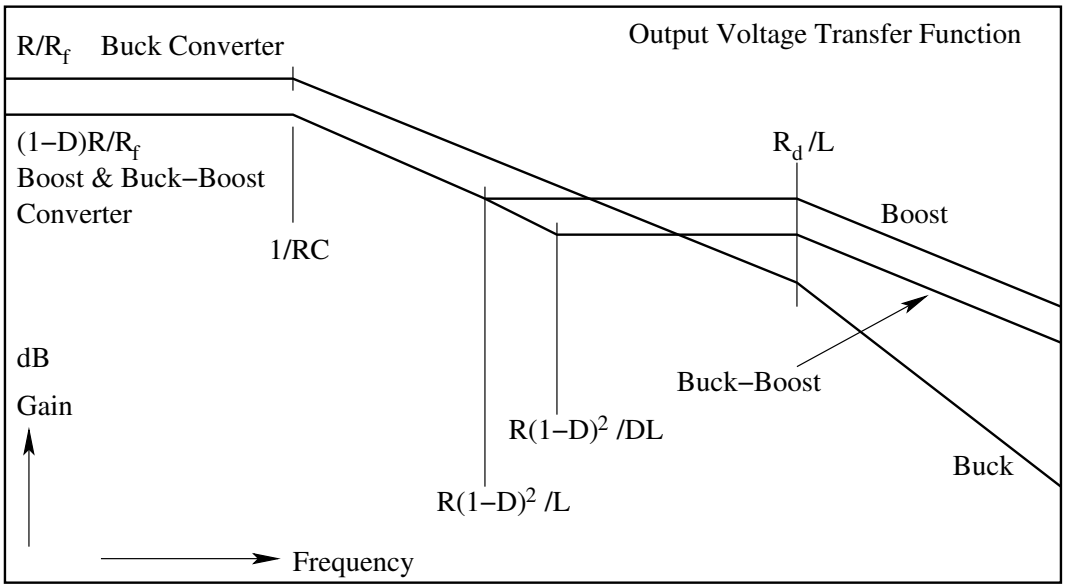

Figure 7.9: Ourput Voltage Control Transfer Function

- Since this frequency response of the converter is having a single slope in the frequency range of ω_1 and ω_z, the compensator design is considerably simple. However, it is to be noticed that ω_1, the dominant low-frequency pole is load dependent.

A commercially available current mode control IC is explained in the following data sheet.

Current mode controller

7.5 Problem Set

1. In current programmed converters, the artificial ramp is used to overcome the problem of sub harmonic instability. When the compensating ramp M_c is chosen to be equal to M_2, the compensation is taken to be best. Consider that M_c is chosen to be equal to 10% of M_2. Evaluate the range of ratio beyond which sub-harmonic instability will now occur. What will happen if M_c is chosen to be 20 % of M_2.

2. Fig. 2 shows a current controlled forward converter. The voltage controller organized as the outer loop is also shown in Fig. 2.

   V_g = 30V to 60 V ; V_o = 5 V ; L = 40 mH ; C = 1000 μF ;
   R_c = 0.02 Ω ; F_s = 50 kHz ; N_1 = 25 ; N_2 = 11 ; R = 1 Ω ;

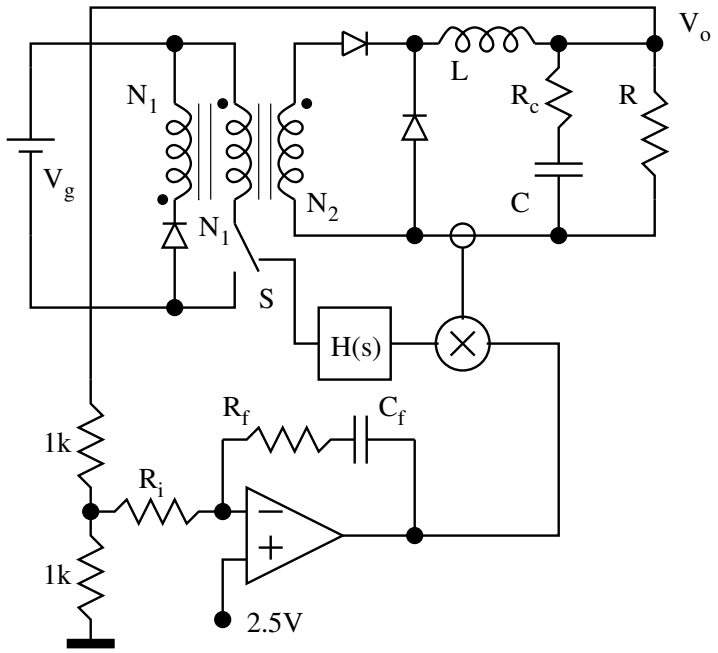

Fig. P 7.2: Current Controlled Forward Converter

(A) Evaluate the relationship between and i. Assume that the current controller is ideal. ($\epsilon = 0$)

(B) Evaluate the current control transfer function $G_i(s) = \dfrac{v_o(s)}{v_c(s)}$ (through the relation between I and v_o through the output filter circuit of the converter).

(C) Sketch the envelope of the transfer function $G_i(s)$ for the full variations in load R. Mark the salient features of transfer function.

(D) Evaluate the compensator design (R_f, C_f, R_i) so that the steady state accuracy is better than 1% and closed loop control bandwidth is better than 500 Hz.

Chapter 8

Soft Switching Converters

8.1 Introduction

In the recent past, switched mode power supplies (SMPS) that make use of resonant circuits for their operation, have emerged as an alternative to the more conventional types employing pulse width modulation (PWM). Among the important advantages claimed for this class of SMPS over the PWM type are the following.

1. Circuit operation is possible at much higher frequencies, giving scope for reducing the size of reactive components.
2. Because of smooth voltage and current waveforms, noise and interference are reduced.
3. Stress on the switching devices is also reduced because of smooth voltage and current waveforms; zero voltage and zero current switching is possible.
4. Parasitic circuit elements, such as transformer leakage inductance, can be taken into account as part of the circuit itself and so need not affect the circuit performance adversely.

The distinguishing feature of soft switched converters is that they switch ON and OFF at zero current or zero voltage. In zero current switching, the switch turns ON from a finite blocking voltage to zero ON state current and turns OFF at zero ON state current to a finite blocking voltage. The zero voltage switching is the dual of the zero current switching process. In either case the switching loss is substantially reduced. The zero current or zero voltage switching is achieved by switching close to the resonant frequency of the load (resonant load converter), or by addition of resonant elements to the switch (resonant switch converters) or by forcing a resonant transition during the switching process (resonant transition).

SMPS employing resonant converters are not without drawbacks. For example, the ratio of the total installed VA of the various components to the

output power - i.e. utilisation of the components - is generally poorer than with PWM type of SMPS. However, because of their many attractive operational features, resonant mode SMPS have taken up an appreciable share of the SMPS market [27, 35, 41].

8.2 Resonant Load Converters

In the following, the basic principle of operation of a resonant load type of SMPS is explained. The important features of circuit operation are pointed out. Relevant equations are developed for the analysis of the circuit. A simplified design procedure is outlined. Some alternative circuit arrangements are also briefly discussed.

8.2.1 Principle of Operation

Consider the circuit shown in Fig. 1. This diagram pertains to the transfer of power from a sinusoidal source of voltage V_g at frequency f ($f = \omega/2\pi$) to the load resistor R through a resonant circuit consisting of L and C. The output voltage V_o and the source current I_g of this circuit can be obtained from the following expressions.

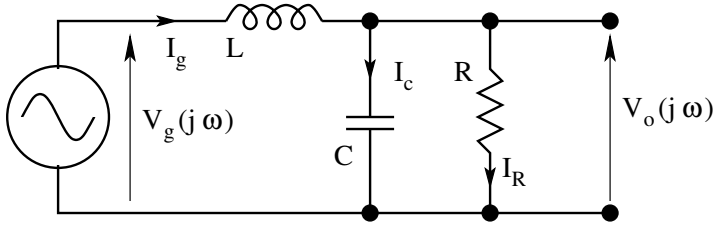

Figure 8.1: Resonant Power Processor

$$V_o = V_g \frac{1}{1 - \left(\frac{\omega}{\omega_o}\right)^2 + j\frac{\omega L}{R}} \tag{8.1}$$

$$I_g = V_g \frac{1 + j\omega CR}{R\left(1 - \left(\frac{\omega}{\omega_o}\right)^2 + j\frac{\omega L}{R}\right)} \tag{8.2}$$

where $\omega_o = 1/\sqrt{LC}$ is the resonant frequency of L and C. The magnitude response of the circuit at various frequencies can be plotted using Eq. [1]. Some typical characteristics are shown in Fig. 2. The curves have been drawn for different amplitudes of the source voltage V_g and different values of load resistance R. Superimposed on the frequency response curves is a dotted

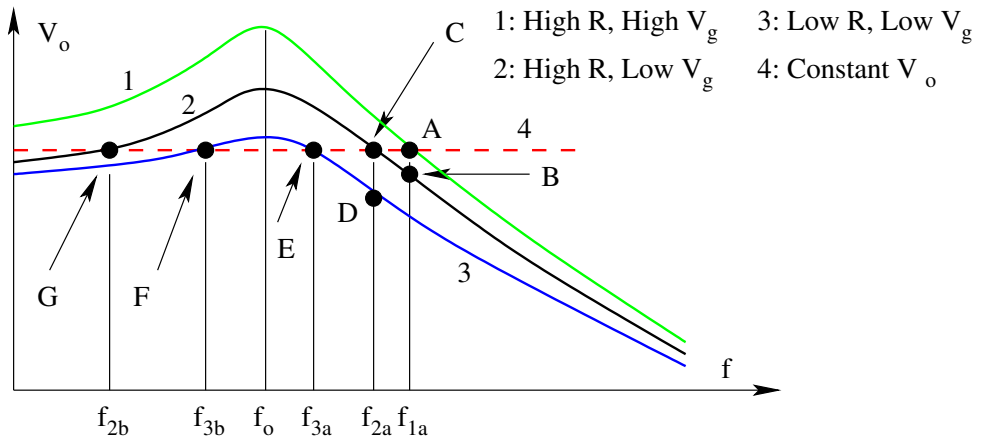

Figure 8.2: Gain Characteristics of the Resonant Circuit

horizontal line called the "constant V_o line". From Fig. 2, it becomes clear that it is possible to maintain a constant amplitude of the output voltage V_o in the face of variation in the source voltage V_g and the load resistance R - in other words regulate the output voltage V_o - provided the frequency of the source is changed correspondingly.

For example consider the portion of the frequency response characteristics which lie above the resonant frequency f_o. When the circuit is operating at a frequency of f_{1a}, with a high amplitude of V_g and a large value of R, i.e. light load, the output voltage is equal to the desired value V_o. This operating point is seen on the characteristics as the point (A). If now the amplitude of the source voltage decreases to a low value, the output voltage will have an amplitude corresponding to point (B), if the frequency is maintained at f_{1a}. Thus the output voltage amplitude decreases with decreasing amplitude of V_g at constant frequency. However, if now the frequency of the source is changed to f_{2a}, the operating point moves to (C) where the output voltage is again the desired value. Thus by changing the frequency, the output voltage can be regulated against source voltage variations.

Similarly, the output voltage can also be regulated against variations in loading i.e. changes in the value of R, by changing the source frequency. This can be understood by considering the operating points (C), (D), and (E).

It is also apparent from Fig. 2 that a similar process of regulation can be carried out by considering frequencies below resonant frequency, as borne out by considering the operating points (F) and (G) for example. However, it can be seen that the direction of change in the source frequency required to regulate the output voltage is different in the two cases. For frequencies above resonance, the source frequency has to be decreased i.e. move towards resonant frequency, in order to correct a tendency of the output voltage to decrease. On the other hand, for frequencies below resonance, the source frequency has

to be increased i.e again moved towards resonance, to correct any tendency of the output voltage to decrease. Also it can be seen that the range of variation in the frequency necessary to achieve output voltage regulation is larger below resonance than above resonance.

Further differences between operation above and below resonance can be appreciated by carrying out simple steady state analysis of the circuit of Fig. 1 and drawing the corresponding phasor diagrams. From Fig. 1,

$$I_R = \frac{V_o}{R} \tag{8.3}$$

$$I_c = j\omega C V_o \tag{8.4}$$

$$I_g = I_R + I_c = \frac{V_o}{R} + j\omega C V_o \tag{8.5}$$

$$V_g = V_o + j\omega L I_g \tag{8.6}$$

$$= V_o + j\omega L \left(\frac{V_o}{R} + j\omega C V_o\right) \tag{8.7}$$

$$= V_o \left(1 - \omega^2 LC\right) + j\frac{\omega L}{R} V_o \tag{8.8}$$

$$V_g = V_o \left(1 - \omega^2 LC\right) + j\frac{\omega L}{R} V_o \tag{8.9}$$

For operation above resonance, $\omega/\omega_o \geq 1$. For operation below resonance,

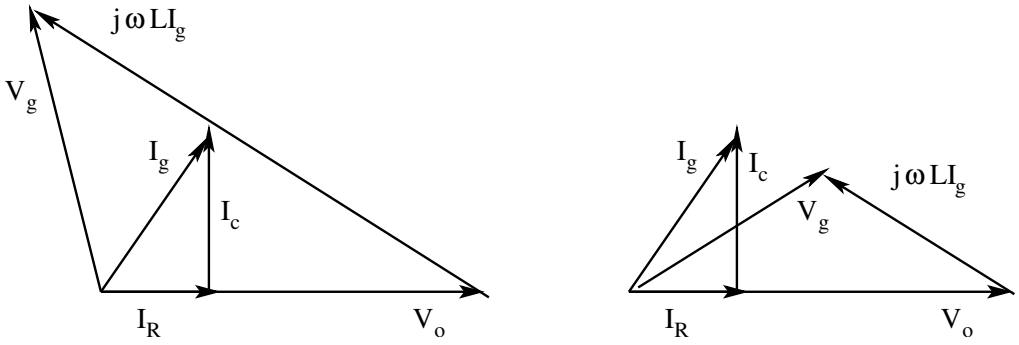

Figure 8.3: Sub-Resonance and Super-Resonance Operation

$\omega/\omega_o \leq 1$. The phasor diagrams corresponding to the two situations are shown in Fig. 3a (operation above resonance) and 3b (operation below resonance) respectively. The following points can be noticed from the phasor diagrams. For operation above resonance:

1. The source voltage V_g leads the output voltage V_o by more than 90°.
2. The source current I_g always lags the source voltage V_g.

For operation below resonance:

1. The source voltage V_g leads the output voltage V_o by less than 90°.
2. The source current I_g may lead or lag the source voltage V_g.
3. The phase relationship can be deduced by examining the imaginary part of the expression for I_g given in Eq. (2).

$$Im(I_g) = \omega C R^2 \left(1 - \left(\frac{\omega}{\omega_o}\right)^2\right) - \omega L \tag{8.10}$$

I_g will lead V_g if the imaginary part is greater than zero. i.e.

$$R^2 \left(1 - \left(\frac{\omega}{\omega_o}\right)^2\right) \geq \frac{L}{C} \tag{8.11}$$

8.2.2 SMPS Using Resonant Circuit

The relevance of Fig. 1 to switched mode power conversion can be readily appreciated by considering the block diagram of a general SMPS shown in Fig. 4. In conventional SMPS, the high frequency switching converter is

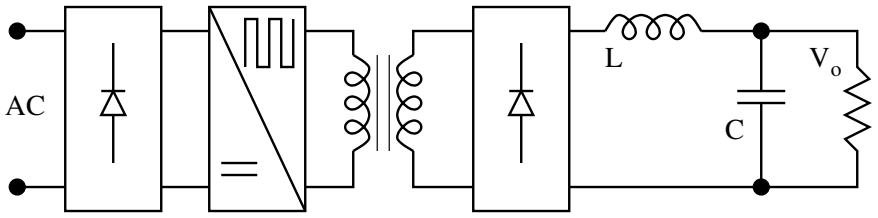

Figure 8.4: A Hard Switching SMPS

usually of the PWM type. Well known configurations are forward, flyback, and push-pull converters. Output voltage regulation is achieved by control of pulse-width, while the frequency is usually fixed. However in the light of the previous discussion, it can be realised that in place of the PWM converter, the configuration shown in Fig. 5 can be used. Voltage regulation can be achieved by frequency control of the sine wave.

In practical implementation, instead of a sine wave inverter, a simple square wave inverter is used, since the resonant circuit itself performs as a low pass filter, resulting in a capacitor voltage waveform that is a good approximation of a sine wave.

The circuit of a practical SMPS incorporating the concepts of sine wave resonant operation is shown in Fig. 6. A half-bridge MOSFET inverter is indicated in Fig. 6. MOSFETs are preferred to bipolar transistors for operation at frequencies of the order of 100 KHz. An important fact to be highlighted

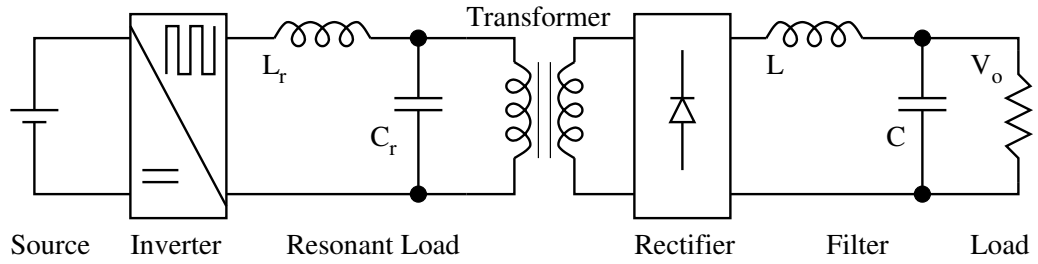

Figure 8.5: An SMPS Based on Resonant Circuit

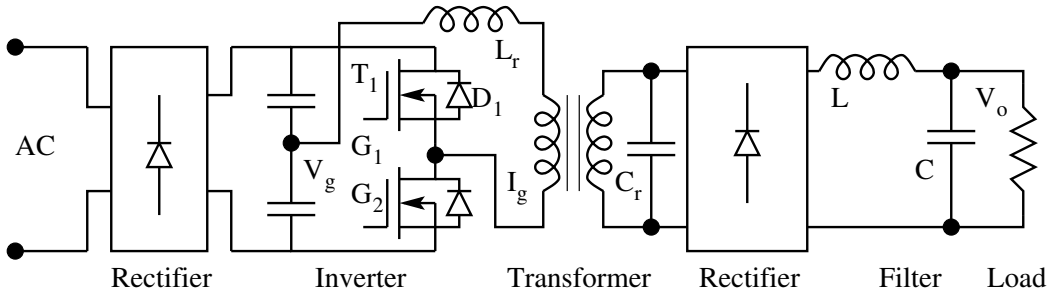

Figure 8.6: A Resonant Inverter Based SMPS

with respect the Fig. 6 is that the resonant capacitor C is shown on the secondary side of the transformer. This implies that the leakage inductance of the transformer is in series with the resonant inductor and can therefore be regarded as forming part of the resonant circuit. Therefore the transformer leakage inductance need not be a troublesome parasitic, causing power loss and voltage spikes, as is the case with PWM converters. This is a feature of resonant SMPS circuits that enhances the possibility of high frequency operation.

From the point of view of the inverter too, operation of the resonant circuit above and below the resonant frequency gives rise to important differences. As deduced earlier, operation of the circuit above resonance results in a lagging phase angle of current with respect to inverter voltage, whereas operation below resonance is more likely to result in a leading phase angle. Of course these deductions were based on the source voltage being purely sinusoidal, whereas the voltage produced by the inverter consists of harmonics, besides the fundamental. However, conclusions regarding the relative positions of the zero crossings of the inverter voltage and current are still valid. Therefore the waveforms of voltage across and current through the inverter switches can be drawn as shown in Fig. 7.

It can be seen from Fig. 7a that for circuit operation above resonance, the current drawn from the inverter lags the voltage. This means that whenever a transistor is switched on, load current actually flows in its antiparallel diode.

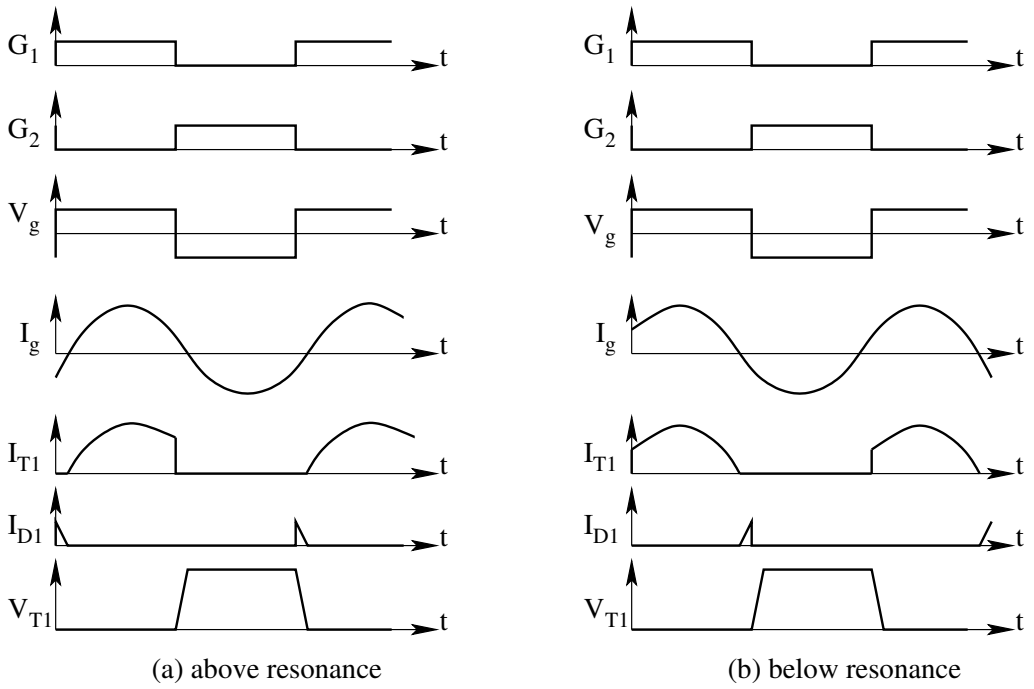

Figure 8.7: Salient Waveforms for Below and Above Resonance

It transfers to the transistor only at the zero crossing of the load current. Thus the snubber capacitor across the transistor can be discharged smoothly by the load current itself and the transistor voltage falls to zero well before the current starts building up. This is referred to as zero voltage switching. The sequence of events during transfer of current from the bottom to the top transistor is shown on Fig. 8. A similar sequence of events takes place during current transfer from the top device to the bottom device. It is clear that because of the zero voltage switching, the snubber gets discharged by the load current itself. The fall di/dt of current in the diodes is very small, as the load inductance is appreciable. Therefore there is no need to have di/dt limiting reactors. The MOSFETs do not have to discharge the snubber capacitors and so there is no need for a resistor to limit the discharge current in the snubber circuit. On the whole then, there is no energy loss in the snubber. A snubber of the form shown in Fig. 8, consisting of only a capacitor, is therefore referred to as a lossless snubber.

In contrast, for operation below resonance, the transistors have to carry the load current as soon as they are turned on and therefore they have to discharge the snubber too. Further since the diode currents are transferred sharply to the transistor, there is a need for di/dt limiting inductor. The energy in this inductor is transferred to the snubber capacitor and subsequently lost. Thus lossless snubbing is not possible in this case.

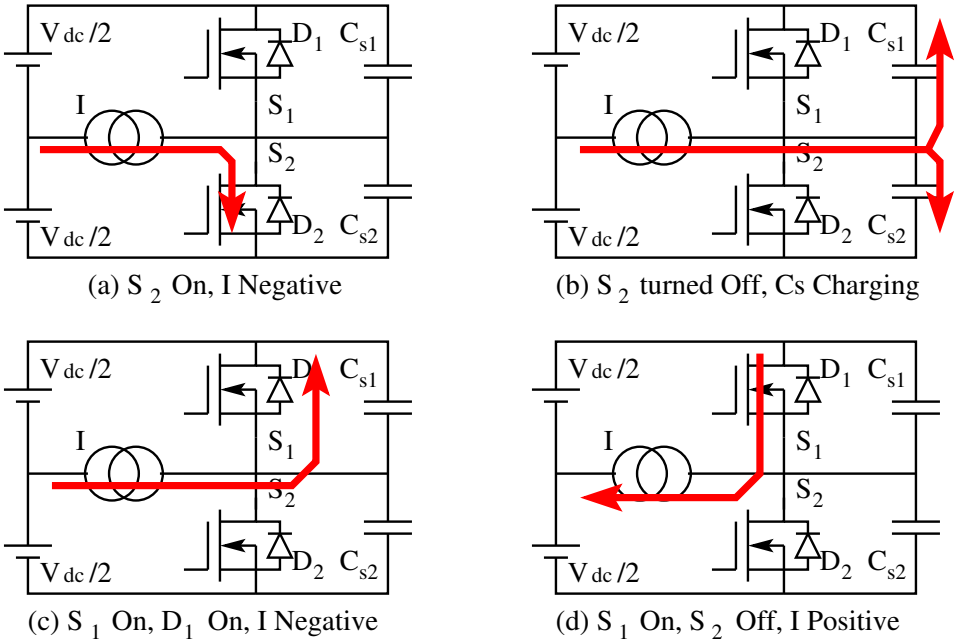

Figure 8.8: Switching Transition in the Resonant Load SMPS

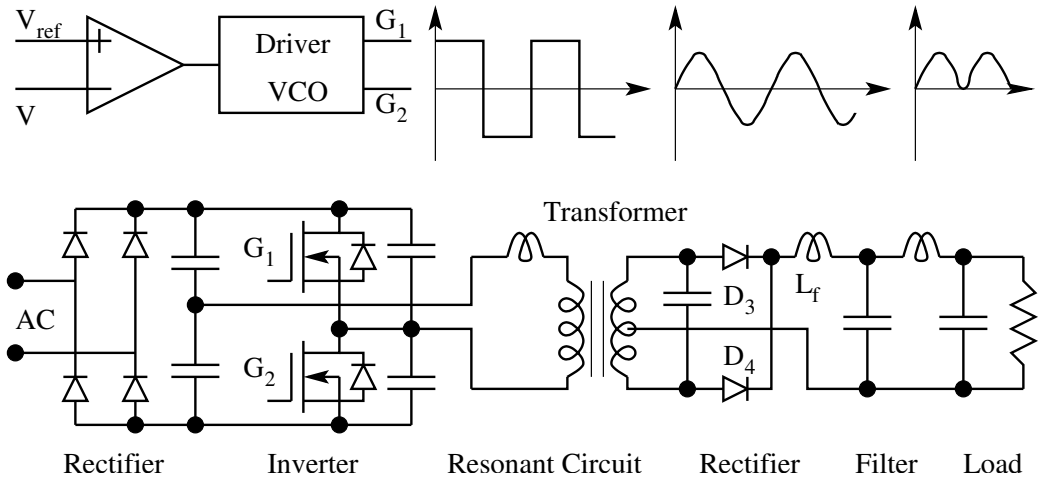

Figure 8.9: Full Power Circuit of a Resonant Load SMPS

It is clear from the above considerations that operation above resonance is preferred for SMPS operation at high frequencies of the order of 100 KHz. The power circuit of a resonant SMPS is indicated in Fig. 9, along with circuit waveforms and a schematic of the control circuit.

The main operating features are highlighted as follows.

1. By placing the resonating capacitor on the secondary side of the trans-

former, the leakage inductance of the transformer has been made part of the circuit. As a result, leakage inductance does not contribute to losses. High operating frequencies are therefore possible. This advantage is gained at the expense of increased current rating for the resonating C.

2. Because of circuit operation above resonance,

   (A) Snubbers are lossless, once again making high frequency operation possible.

   (B) Frequency variation required to regulate the output voltage is quite small.

3. Because of sinusoidal voltage and current waveforms, less interference is generated compared to PWM type of SMPS.

4. Since the output rectifiers D_3 and D_4 operate from sinusoidal voltage waveforms, ultra-fast recovery diodes are not needed. For example, even for 200 KHz operation, rectifiers with 50 nS recovery times have been reported to be adequate.

5. Because of higher operating frequencies and sinusoidal voltage waveforms, the size of the output filter is less than that for PWM converters.

6. Operation under output short circuit is possible, as current is limited by the resonating inductor.

8.2.3 Steady State Modeling of Resonant SMPS

As was pointed out earlier, the inverter of the resonant SMPS applies a variable frequency square wave to the resonant circuit, whereas the frequency response curves of Fig. 2 have been obtained assuming a sinusoidal source voltage V_g. To obtain somewhat more exact characteristics of the circuit, it is necessary to identify the conducting switch at any instant of time and write down the corresponding circuit differential equations. An approach towards the steady state analysis of the resonant SMPS is outlined below. The operating frequency of the resonant circuit being high, it can be reasonably assumed that over one cycle of the inverter operation, the current in the filter inductor L_f is constant. This loading of the resonant circuit can therefore be modelled as a constant current source across the resonating capacitor C, the direction of the current being decided by whether D_3 or D_4 is in conduction. D_3 will conduct if the capacitor voltage is positive, while D_4 will conduct if it is negative. The capacitor and the load can further be reflected to the primary side of the transformer, any leakage inductance being clubbed with the resonating inductor L_r. Based on these considerations the steady state waveforms of the circuit can be drawn over one cycle as shown in Fig. 10. The circuit basically operates in two modes, termed mode A and mode B. The equivalent circuits

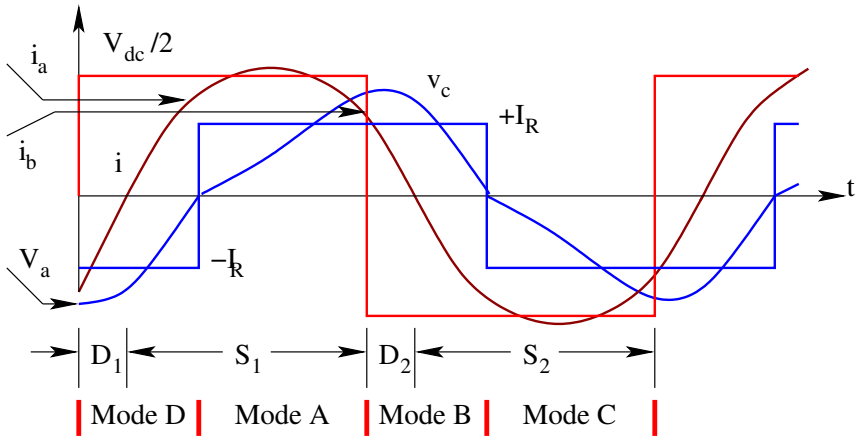

Figure 8.10: Steady State Inductor Current and Capacitor Voltage

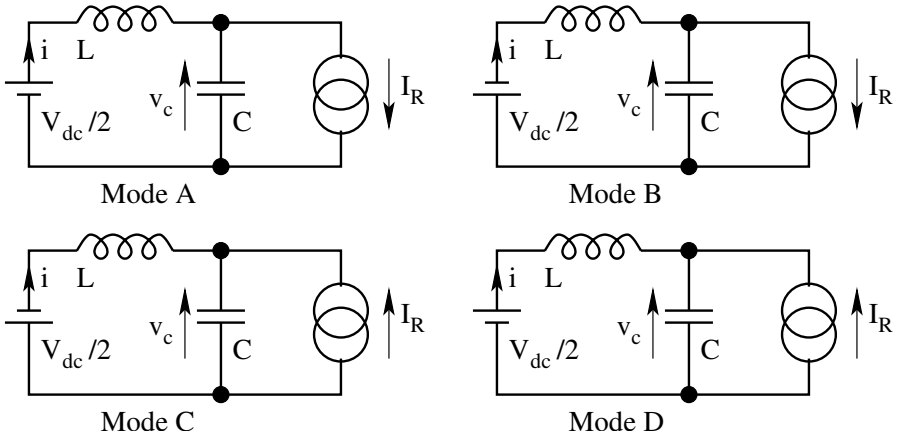

Figure 8.11: Equivalent Circuits in Mode A and Mode B

for these two modes are shown in Fig. 11. The circuit response in each of these modes can be obtained by solving the appropriate differential equation.

Mode A:

$$L\frac{di}{dt} + \frac{1}{C}\int_0^t (i - I_R)dt = \frac{V_{dc}}{2} \tag{8.12}$$

Solving this subject to $i(0) = i_a$, the response of inductor current i and capacitor voltage v_c may be obtained.

Mode B:

$$L\frac{di}{dt} + V_{co} + \frac{1}{C}\int_0^t (i - I_R)dt = -\frac{V_{dc}}{2} \tag{8.13}$$

Solving this subject to $i(0) = i_b$, and $V_{co} = V_a$, the response of inductor current i and capacitor voltage v_c may be obtained.

Mode C:

$$L\frac{di}{dt} + \frac{1}{C}\int_0^t (i + I_R)dt = \frac{V_{dc}}{2} \tag{8.14}$$

Solving this subject to $i(0) = -i_a$, the response of inductor current i and capacitor voltage v_c may be obtained.

Mode D:

$$L\frac{di}{dt} + V_{co} + \frac{1}{C}\int_0^t (i + I_R)dt = -\frac{V_{dc}}{2} \tag{8.15}$$

Solving this subject to $i(0) = -i_b$, and $V_{co} = -V_a$, the response of inductor current i and capacitor voltage v_c may be obtained.

It is to be noted once again that V_a, i_a, and i_b are the initial values of capacitor voltage and inductor current at the discontinuities.

Using Eqs (12) to (15) and the waveforms of Fig. 10, it is possible to obtain the steady state operating point of the circuit by noting that the values of i and v_c at the beginning and end of the inverter half cycle must be equal in magnitude and opposite in polarity. From the resulting solution of the circuit, it is possible to calculate the various quantities of interest such as the peak and rms values of i, the rms and average currents through the MOSFETs and diodes etc.

8.2.4 Approximate Design Procedure

By using the information obtained on the basis of the above analysis, it is possible to design the resonant SMPS. However, to arrive at a reasonable first estimate of component sizes, ratings etc., a somewhat simple analysis and design procedure would be more convenient. In the following, a simple design method based on sinusoidal steady state analysis of the resonant circuit, neglecting harmonics in the inverter output voltage is discussed.

From the principle of operation of the resonant circuit, it is clear that as the loading becomes heavier or the source voltage reduces, the operating frequency has to move closer to resonance. Therefore, for worst case design, it can be assumed that at the heaviest load and lowest source voltage, the circuit is operating at the resonant frequency f_o. At all other conditions it is operating above resonance. The general AC equivalent circuit of the converter is shown in Fig. 12.

In this circuit, the resistance R includes the load on the dc side of the output rectifier and any other losses such as the transformer losses etc. The resonating inductor is shown on the secondary side, although in the actual circuit it will be connected on the primary side and must be taken to include

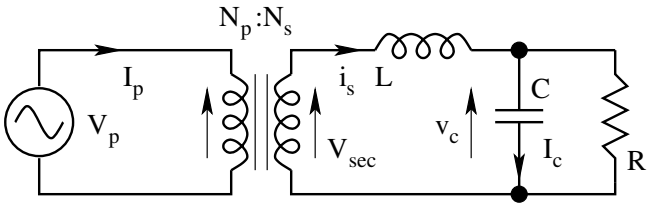

Figure 8.12: Approximate AC Equivalent Circuit

the leakage inductance of the transformer also. V_{ac} is the equivalent rms ac output voltage of the ac equivalent circuit. V_p represents the fundamental component of the inverter output voltage. At resonance, using Eq. (1), we get

$$V_{ac} = V_{sec}\left|\frac{1}{j\omega_o L/R}\right| \tag{8.16}$$

$$V_{sec} = \frac{V_{ac}}{R} j\omega_o L \tag{8.17}$$

$$V_{sec} = I_R j\omega_o L \tag{8.18}$$

$$|V_{sec}| = I_R j\omega_o L \tag{8.19}$$

The value of I_R used in Eq. (19) should be the heaviest load current that is to be designed for. The design steps can now be summarised.

Given:

The equivalent ac output voltage: V_o
The resonant frequency: f_o
The maximum load current: I_R
The Fundamental component of input voltage: V_p

Step 1

Chose a capacitor value: C.

Capacitor Current:

$$|I_c| = \omega_o C V_o \tag{8.20}$$

Secondary Current:

$$|I_s| = \sqrt{(I_c^2 + I_R^2)} \tag{8.21}$$

Step 2

Inductor Value: L.
Inductance:

$$L = \frac{1}{C\omega_o^2} \tag{8.22}$$

Step 3

Secondary Voltage: V_{sec}.
Secondary Voltage:

$$|V_{sec}| = \omega_o L I_R \tag{8.23}$$

Step 4

Transformer Ratio: N_p/N_s
Transformer Ratio:

$$\frac{N_p}{N_s} = \frac{V_p}{V_{sec}} \tag{8.24}$$

Step 5

Primary Current: I_p
Primary Current:

$$|I_p| = I_s \frac{N_s}{N_p} \tag{8.25}$$

This gives us all the information necessary for deciding on the ratings of the various components. To illustrate the process, the following design example may be considered.

8.2.5 Design Example

Design a resonant SMPS to deliver 5 A, 20 V (100 W) regulated output, operating from single phase ac mains of 230 V ±10%. The operating frequency is to be around 100 kHz.
The required dc output voltage: 5 V

Peak value of full wave rectified ac voltage: $5\pi/2 = 7.85\ V$

Allowing for the drop across the output diode to be 1.5 V, the peak value of the sinewave across the resonating capacitor : $2(7.85 + 1.5) = 18.7\ V$

Rms value of Vac : $18.7/\sqrt{2} = 13.2\ V$

Since operation above 100 kHz is required : $f_o = 100\ kHz$

$$\omega_o = 628318 \text{ rad/sec}$$

Maximum load with centre tapped secondary : $I_R = \frac{20}{2}\frac{4}{\pi\sqrt{2}}$

$$I_R = 9\ A$$

Minimum primary voltage assuming a bridge rectifier at the input with 230 V ac input and a half bridge inverter :

$$V_p = 0.9\ 230\ \sqrt{2}\frac{4}{2\pi\sqrt{2}}$$

$$V_p = 132\ V$$

Using the above values of V_o, f_o, I_R, and V_p, design steps 1 to 5 can be iterated starting with different values for the capacitor C.

For Example:

Step 1:

Choose $C = 1\mu F$

$$I_c = 2\ \pi\ (100000)(1)(10^{-6})13.2\ =\ 8.3\ A$$

$$I_s = \sqrt{8.3^2 + 9^2}\ =\ 12.2\ A$$

Step 2:

Inductance referred to the secondary:

$$L = \frac{1}{(2\pi)^2(100000)^2(1)(10^{-6})} =\ 2.5\ \mu H$$

Inductance referred to the primary:

$$L = 2.5\ (9.3)^2\ =\ 216\ \mu H$$

Step 3:

Secondary Voltage:

$$V_{sec} = (2\pi)(100000)\,(2.5\ 10^{-6})\ 9\ =\ 14.2\ V \text{ rms}$$

Step 4:

Transformer turns ratio:

$$\frac{N_p}{N_s} = \frac{132}{14.2} \;=\; 9.3$$

Step 5:

Primary Current:

$$I_p = \frac{12.2}{9.3} \;=\; 1.3\ A$$

From the above the voltage and current ratings of the MOSFETs can be decided. In order to get some appreciation of the capacitor value, five different designs are summarised in Table 1. Study of the Table 1 shows that the VA

Table 8.1: Design of Resonant Load SMPS

									VA Ratings			
Sl No.	C μF	I_c A	I_s A	L_s μH	V_{sec} V	$N_p : N_s$	I_p A	L_p μH	L J	C J	T J	Total J
1	0.22	1.8	9.2	11.5	65	2.03	4.5	47	611	24	598	1,223
2	0.47	3.9	9.8	5.4	30.4	4.3	2.3	101	335	51	304	690
3	1	8.3	12.2	2.5	14.1	9.3	1.3	216	269	109	207	585
4	2.2	18.2	20.3	1.2	6.8	19.4	1.1	451	287	240	139	666
5	4.7	39	40	0.5	3	43.4	0.9	1,017	540	514	121	1,175

of the inductor dominates the total VA requirement of reactor components. Further, as the capacitor value is increased, there is an optimum value up to which the inductor VA and the total VA keep falling. Further increase in the value of the capacitor results in an increase in the total VA requirements. Moreover, even considering the design with the lowest VA requirement among those shown, it is seen that the total VA is more than five times the power output of the SMPS. This is characteristic of resonant circuits, the ratio of installed VA of output power being high, in the range of 2.5 to 3.

The above design is of course based on an approximate analysis, but is useful to obtain initial values for the components and their ratings. These figure can subsequently be subjected to a more careful analysis. Also, the VA figures in Table 1 do not include the output filter components.

8.3 Resonant Switch Converters

Switched mode power supplies employing pulse width modulation (PWM) have generally been operated at frequencies of the order of 50 KHz. While it has been recognised that operation at high frequencies offers the possibility of reduced size and weight, PWM converters are by nature not amenable to operation at very high frequencies of the order of 1 MHz. This is because of the fact that when the switch in a PWM converter is going from the ON state to the OFF state or vice versa, both the voltage across and the current through the switch undergo variation. As a result at every switching the device traverses the active region in its output characteristics, with accompanying losses. These losses, being switching losses, increase directly with operating frequency and thus limit the frequency of operation of PWM converter. Further, inevitable stray circuit elements, such as transformer leakage inductances, device output capacitance etc. cannot be made to play a useful part in circuit operation, and cause undesirable effects such as voltage and current spikes.

If operating frequencies in the MHz region are to be attempted in SMPS, which would certainly seem to be a desirable thing, it is clear that the first requirement is a better switching locus for the main power switch, so that switching losses are minimised. Two approaches to achieve this goal have emerged, known as zero current switching (ZCS) and zero voltage switching (ZVS). These can be broadly defined as follows.

Zero current switching: In this approach, it is ensured that both at turn-on and turn-off, the current through the switching device remains at zero and does not change suddenly.

Zero voltage switching: In this approach, it is ensured that both at turn-on and turn-off, the voltage across the switching device remains at zero and does not change suddenly.

8.3.1 Switch Realisation

As is clear from the above definition, to achieve zero current switching, the switching device has to be immediately followed or preceded by an inductor, so that current through the switch cannot change suddenly. Similarly, to achieve zero voltage switching, the switching device should be connected in parallel with a capacitor, so that the voltage across the switch cannot change suddenly. Figure 13 shows two switch realisations which achieve ZCS and ZVS respectively.

In these switches, the basic PWM switch consisting of a transistor (or MOSFET) and its feedback diode has been surrounded by a suitable LC network to achieve ZCS/ZVS. Although several variations are possible on these realisations, in the following the switch of Fig. 13 will only be considered. The L and C elements in these switches are designed to constitute a resonant circuit. By this means the current through (or the voltage across) the switch is made

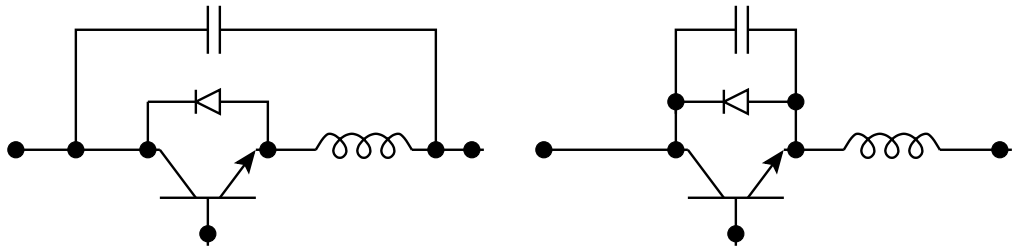

Figure 8.13: Zero Current & Zero Voltage Switching

to vary in a smooth sinusoidal fashion. Families of SMPS converters can be realised by replacing the PWM switch in conventional SMPS topologies such as buck, boost etc. by the switch configuration shown in Fig. 13. Such SMPS topologies have come to be known as quasi-resonant converters. In the following, the well known buck converter is considered and its operation with ZCS/ZVS is explained in order to bring out the essential features of the new topologies.

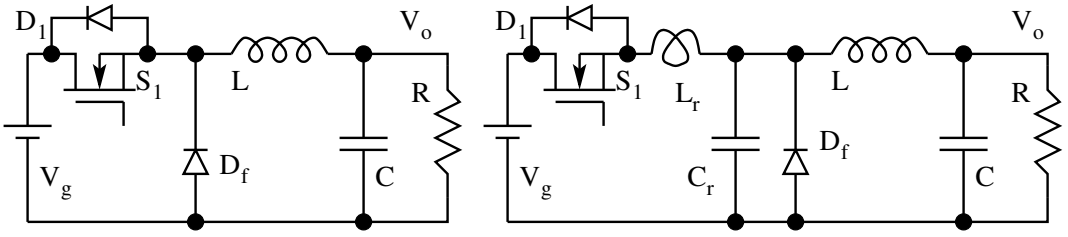

Figure 8.14: Hard Switching & ZVS Buck Converter

8.3.2 Buck Converter with Zero Current Switching

Figure 14 shows the PWM buck converter and its ZCS counterpart. The operation of the PWM version is well known. Operation is at fixed frequency, with the duty ratio being the control variable. In the following the operation of the ZCS version is explained.

8.3.3 Operation of the Circuit

Assume that, in the circuit in Fig. 14, to start with the output current I_o is freewheeling through the diode D_f and that the switch S_1 is OFF. The equivalent circuit under these conditions is shown below in Fig. 15a.

At t = 0, the switch S_1 is turned ON. The equivalent circuit under these conditions is shown below in Fig. 15b. The resonant capacitor C_r voltage

continues to be at zero (since D_f is still ON). The current in the resonating inductor L rises linearly following the equation

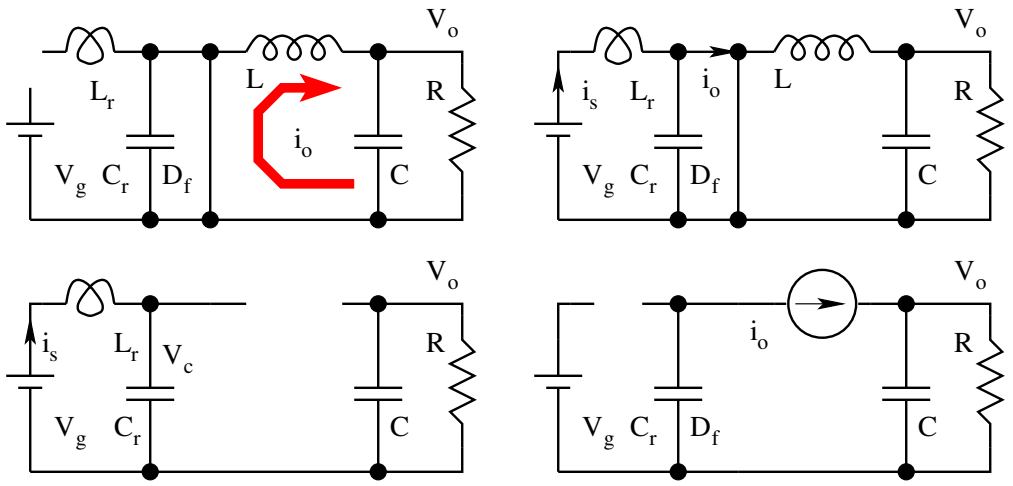

Figure 8.15: Equivalent Circuits of ZVS Buck Converter

$$L_r \frac{di_s}{dt} = V_g \tag{8.26}$$

$$i_s = \frac{V_g\ t}{L_r} \tag{8.27}$$

The circuit operates in this mode until the current i_s becomes equal to the load current I_o and the diode D_f gets reverse biased. This will happen after an interval T_1 given by

$$T_1 = \frac{L_r I_o}{V_g} \tag{8.28}$$

At the end of T_1, D_f stops conducting. The capacitor C discharges through S_1 and L_r in a resonant manner. The equivalent circuit under these conditions is shown in Fig. 15c. Because of the large filter inductor L, the current I_o can be assumed to be constant. The circuit equations are as follows.

$$L_r \frac{di_s}{dt} = V_g - v_c \tag{8.29}$$

$$C_r \frac{dv_c}{dt} = i_s - I_o \tag{8.30}$$

$$V_g = L_r \frac{di_s}{dt} + v_c(0) + \frac{1}{C_r}\int_0^t (i_s - I_o)\ dt \tag{8.31}$$

The initial conditions are: $i_s(0) = I_o$; $v_c(0) = 0$; the solution is

$$i_s(t) = I_o + V_g\sqrt{\frac{C_r}{L_r}} Sin\ \omega_o(t) \tag{8.32}$$

$$\omega_o = \sqrt{\frac{1}{L_r C_r}} \tag{8.33}$$

The capacitor voltage is given by

$$v_c(t) = V_g \ (1 - Cos \ (\omega_o t)) \tag{8.34}$$

In the above equations the origin for time is taken as the beginning of this mode. i.e. the instant at which D_f stops conducting. In order to achieve ZCS, the current $i_s(t)$ given by Eq. [32] must proceed to zero. It can be seen that the necessary condition for ZCS is that

$$I_o \ \leq \ V_g \sqrt{\frac{C_r}{L_r}} \tag{8.35}$$

We may define a dimensionless parameter $\sigma \ = \ \frac{I_o \sqrt{L_r}}{V_g C_r}$. Then for satisfactory quasi-resonant operation, $\sigma \ > \ 1$. If the above condition is satisfied, the current through the switch will be negative for some duration (after the time when the switch current passes through zero).

$$\omega_o \ T_2 = \pi + Sin^{-1}\sigma \tag{8.36}$$

$$\omega_o \ T_3 = 2\pi - Sin^{-1}\sigma \tag{8.37}$$

$$i_s(t) = I_o \left(1 + \frac{1}{\sigma} Sin \ (\omega_o t)\right) \tag{8.38}$$

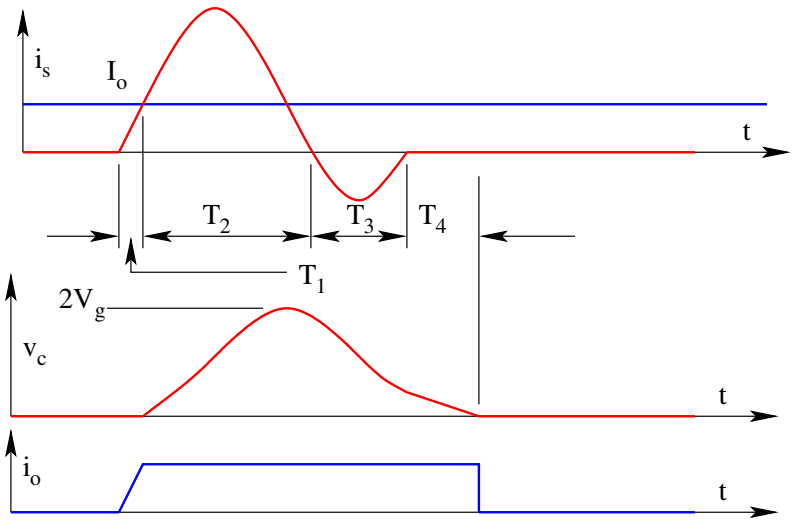

Figure 8.16: Waveforms in the Fullwave ZVS Buck Converter

The wave forms of the current $i_s(t)$, $I_o(t)$, and the voltage $v_c(t)$ during this mode of circuit operation are all shown in Fig. 16. During the time when the

current is negative, it flows through the diode D_1. During this time, if the gating signal to the switch is removed, it can turn-off at zero voltage and with very little loss.

$$v_c(T_3) = V_g \ (1 - Cos \ (\omega_o T_3)) \tag{8.39}$$

At t = T_3, both D_1 and S_1 are OFF. The equivalent circuit is shown in Fig. 15d. The voltage $v_c(t)$ is now given by

$$v_c(t) = v_c(T_3) - \frac{I_o \ t}{C_r} \tag{8.40}$$

This mode comes to an end when $v_c(t)$ reaches zero, at time $t = T_4$ as shown in Fig. 16.

$$T_4 = v_c(T_3)\frac{C_r}{I_o} \tag{8.41}$$

The circuit reverts back to the mode described in Fig. 15a with the load current freewheeling in D_f and remains in this mode until S_1 is turned ON again. From the above explanation, it becomes clear that the duration for which the switch S_1 is gated ON is rigidly determined by the resonant period of the LC components. However, the interval between two consecutive turn ONs of S_1 can be varied. Therefore the circuit operates in "constant ON time, variable frequency mode".

8.3.4 Conversion Ratio of the Converter

With reference to Figs 15 and 16, we see that the average input current I_g is the average of the current $i_o(t)$ over one switching cycle.

$$I_g = \frac{\left(I_o\frac{T_1}{2} + I_o T_3 + I_o T_4\right)}{T_s} \tag{8.42}$$

$$I_g = I_o\frac{\left(\frac{T_1}{2} + T_3 + T_4\right)}{T_s} \tag{8.43}$$

Since the converter is lossless, $\frac{V_o}{I_g} = \frac{I_g}{I_o}$,

$$M_f = \frac{V_o}{V_g} = f_s\left(\frac{T_1}{2} + T_3 + T_4\right) \tag{8.44}$$

From Eq. [28], $\omega_o T_1 = \sigma$;

From Eq. [12], $\omega_o T_3 = 2\pi - Sin^{-1}\sigma$;

and from Eqs [139] and [16], $\omega_o T_4 = \frac{1 - \sqrt{(1-\sigma^2)}}{\sigma}$;

$$M_f = G_f(\sigma)\frac{f_s}{f_o} \tag{8.45}$$

$$G_f(\sigma) = \frac{\left(\frac{\sigma}{2} + 2\pi - Sin^{-1}\sigma + \frac{\left(1-\sqrt{1-\sigma^2}\right)}{\sigma}\right)}{2\pi} \tag{8.46}$$

The following Table gives the value of $G_f(s)$ for different values of σ.

Table 8.2: Conversion Factor for Half and Full Wave ZCS Buck Converter

σ	0.0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1.0
$G_f(\sigma)$	1.00	0.99	0.99	0.99	0.99	0.99	0.99	0.99	0.99	0.99	-
$G_h(\sigma)$	-	3.70	2.12	1.61	1.36	1.22	1.13	1.07	1.03	1.01	1.00

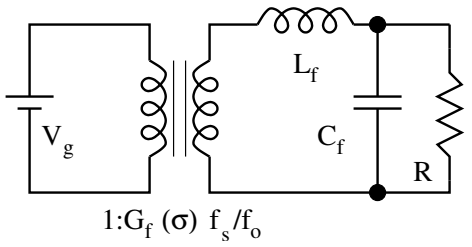

Figure 8.17: Equivalent Circuit of Full Wave ZVS Buck Converter

In the practical range of 0 to 1 for σ, the function $G_f(s)$ is practically constant and is equal to 1. Therefore the conversion factor of the converter may be taken as f_s/f_o. The quasi-resonant converter therefore may be represented by the equivalent circuit shown in Fig. 17. The step-down feature of the buck topology is obvious from the conversion factor. The dynamic model of the converter may be readily obtained by following the circuit averaging technique explained in Chapter 5.

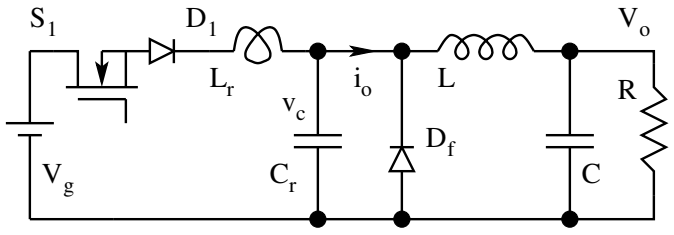

Figure 8.18: Halfwave ZVS Buck Converter

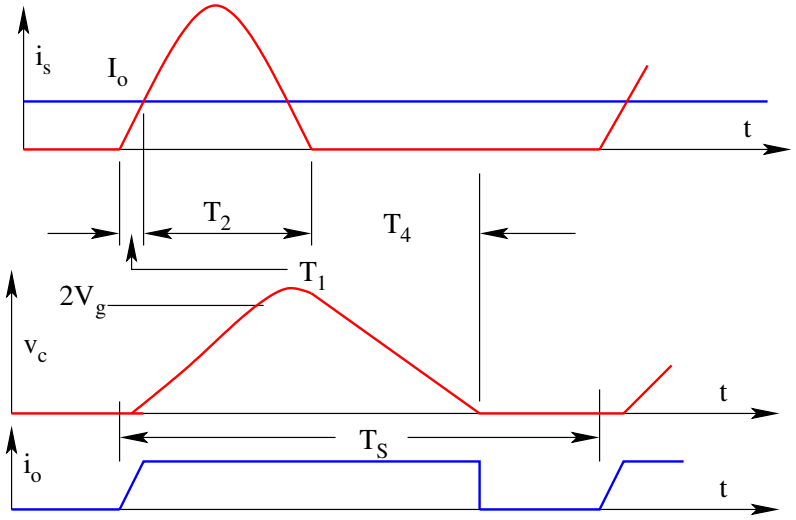

Figure 8.19: Waveforms in a Halfwave ZVS Buck Converter

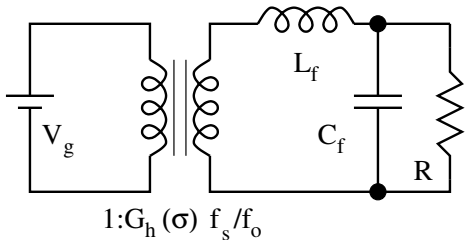

Figure 8.20: Equivalent Circuit of Halfwave ZVS Buck Converter

8.3.5 Halfwave Operation of the Converter

We may operate the above converter in a different mode of operation called the halfwave operation. The circuit topology for halfwave operation is shown in Fig. 18. The operating waveforms are shown in Fig. 19. The equivalent circuit is shown in Fig. 20. The device current stops at $\omega_o T_2$, on account of the series diode with the switch. The conversion factor for the converter is given by

$$M_f = G_h(\sigma)\frac{f_s}{f_o} \tag{8.47}$$

$$G_h(\sigma) = \frac{\left(\frac{\sigma}{2} + \pi + Sin^{-1}\sigma + \frac{\left(1-\sqrt{1+\sigma^2}\right)}{\sigma}\right)}{2\pi} \tag{8.48}$$

It may be seen from the Table that $G_h(s)$ is a strong function of the operating point σ, unlike the case of fullwave operation, and so is suitable for only

converters where the circuit operating point does not change appreciably. The dynamic model of the converter may be derived from the equivalent circuit given in Fig. 20. Notice that the dynamic model will be messy because the gain $G_h(s)$ is a function of V_g and I_o as well besides f_s.

The main features of the ZCS SMPS can be listed as follows.

1. Device turn-on and turn-off happen at zero current theoretically. However, in the above description, the output capacitance of the switch S_1 has not been considered. This capacitance discharges into the switch at turn-on, and the inductance is not able to limit this discharge current. Therefore all the energy in the device output capacitance is lost in the device, and at very high frequencies in the MHz range, the turn-on losses can be appreciable. This is one factor which limits the frequency range of operation of the ZCS converter.

2. While the device voltage rating is only the battery voltage V_g, the peak repetitive current rating has to be more than twice the output current I_o.

3. Zero current switching is possible only if the load current Io does not exceed the value $V_g(C_r/L_r)$.

4. The sequence of events in each cycle is :

   (A) charging of inductor at constant voltage.

   (B) resonant circuit operation.

   (C) charging of capacitor at constant current.

   (D) load current freewheeling through the freewheeling diode.

8.3.6 Boost Converter with Zero Voltage Switching

Figures 21a and 21b show the PWM converter and its ZVS counterpart operating in the halfwave mode.

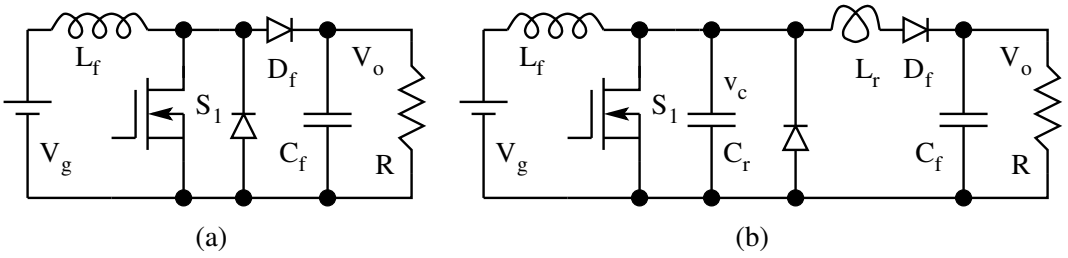

Figure 8.21: Hard Switched and Soft Switched Boost Converter

Operation of the Circuit:

Assume that to start with the switch S_1 is ON and carrying the inductor current I_g. The equivalent circuit is shown in Fig. 22a. At t = 0, S_1 is turned OFF. Because of the presence of C_r, the voltage across S_1 cannot increase instantaneously. The inductor current I_g is diverted to the capacitor C_r. The equivalent circuit is shown in Fig. 22b. The capacitor voltage is described by

$$v_c(t) = \frac{I_g}{C_r}\, t \tag{8.49}$$

The capacitor charges linearly until $v_c = V_o$ at time t = T_1 given by

$$T_1 = \frac{C_r V_o}{I_g} \tag{8.50}$$

At this instant, the free wheeling diode D_f becomes forward biased. The

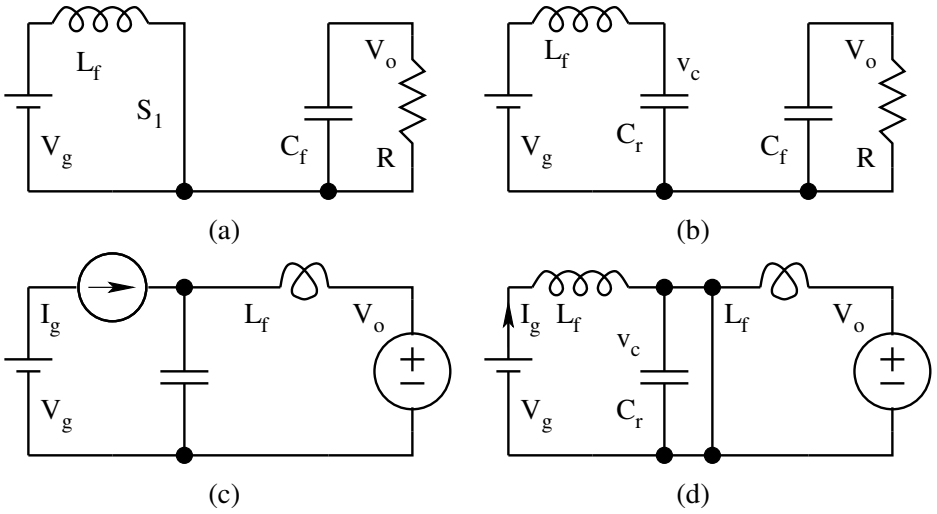

Figure 8.22: Sub-Intervals in ZVS Boost Converter

circuit enters into a resonant mode of operation. The equivalent circuit is as shown in Fig. 22c. The circuit behaviour is described by

$$v_c = V_o + L_r \frac{di_l}{dt} \tag{8.51}$$

$$I_g = i_l + C_r \frac{dv_c}{dt} \tag{8.52}$$

$$0 = C_r \frac{d^2 v_c}{dt^2} + \frac{v_c - V_o}{L_r} \tag{8.53}$$

$$v_c(0) = 0 \; ; \; \left| \frac{dv_c}{dt} \right|_{t=0} = \; I_g \tag{8.54}$$

$$v_c(t) = V_o + I_g\sqrt{\frac{L_r}{C_r}}Sin(\omega_o t) \quad \left[\omega_o = \frac{1}{2\pi\sqrt{L_r C_r}}\right] \tag{8.55}$$

$$i_l(t) = I_g\left(1 - Cos(\omega_o t)\right) \tag{8.56}$$

To achieve zero voltage switching, the capacitor voltage has to go down to zero following resonance. Alternatively, the dimensionless parameter σ $\left(\sigma = \frac{V_o\sqrt{C_r}}{I_g\sqrt{L_r}}\right)$ has to be less than 1.

$$V_o \leq I_g\sqrt{\frac{L_r}{C_r}}\ ;\ \sigma = \frac{V_o}{I_g}\sqrt{\frac{L_r}{C_r}} \leq 1 \tag{8.57}$$

The time T_2 when the capacitor voltage reaches zero following resonance is obtained from,

$$\omega_o(T_2) = \pi + Sin^{-1}(\sigma) \tag{8.58}$$

$$i_l(T_2) = I_g\left(1 - Cos(\omega_o T_2)\right) \tag{8.59}$$

At t = T_2, the capacitor voltage reaches zero, and the diode across the switch gets forward biased. Subsequently the current in the resonant inductor linearly falls to zero. The equivalent circuit is shown in Fig. 22d. Current i_l is given by

$$i_l(t) = i_l(T_2) - \frac{V_o}{L_r}t \tag{8.60}$$

Current i_l becomes zero at T_3, given by

$$T_3 = i_l(T_2)\frac{L_r}{V_o} \tag{8.61}$$

It is to be noted that during this mode of operation, the voltage across S_1 is zero as D_1 is conducting. If the gating signal is applied to S_1 now, it will turn-on at zero voltage. At T_3, diode D_f gets reverse biased and the circuit reverts back to the initial mode given in Fig. 22a.

From the above it is clear that for ZVS operation, the duration for which the switch is OFF is decided rigidly by the period of resonance of the LC components. The interval between consecutive turn-offs of S_1 can be varied, keeping the OFF time constant, to achieve output voltage regulation. Therefore the circuit operates in the "constant OFF time variable frequency mode"

One important aspect to be noted is that S_1 should be turned ON again before the current is turns positive following resonance if ZVS is to be achieved, as otherwise the capacitor will once again charge in the positive direction. However S_1 cannot be turned on before $v_c(t)$ becomes zero either (Fig. 25). Therefore deciding the instant of turn-on of S1 becomes critical. This problem may be overcome by using the fullwave version of the circuit given in Fig. 23.

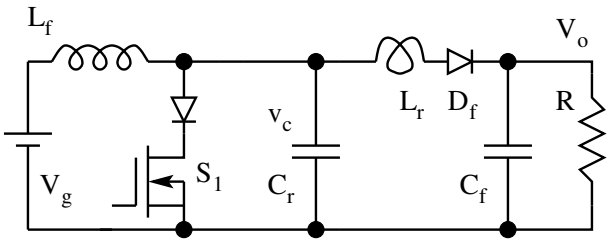

Figure 8.23: Full Wave ZVS Boost Converter

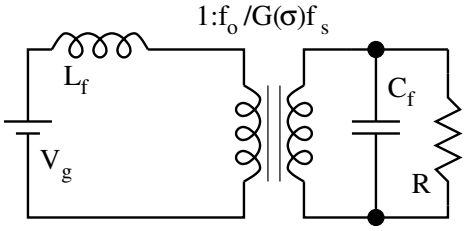

Figure 8.24: Equivalent Circuit of the ZVS Converter

Conversion Factor

Just as we did for the buck ZCS converter, considering that the converter is lossless, the conversion factor $\frac{V_o}{V_g}$ is evaluated.

$$M_h = \frac{V_o}{V_g} = \frac{1}{G_h(\sigma) f_s / f_o} \tag{8.62}$$

$$G_h(\sigma) = \frac{\left(\frac{\sigma}{2} + \pi + Sin^{-1}\sigma + \frac{\left(1 - \sqrt{1+\sigma^2}\right)}{\sigma}\right)}{2\pi} \tag{8.63}$$

The fullwave version of the boost quasi-resonant ZVS circuit is shown in Fig. 23. The equivalent circuit of the converter is given in Fig. 24. The circuit waveforms are given in Figs 25 and 26. The conversion factor for the fullwave version is

$$M_f = \frac{V_o}{V_g} = \frac{1}{G_f(\sigma) f_s / f_o} \tag{8.64}$$

$$G_f(\sigma) = \frac{\left(\frac{\sigma}{2} + 2\pi - Sin^{-1}\sigma + \frac{\left(1 + \sqrt{1+\sigma^2}\right)}{\sigma}\right)}{2\pi} \tag{8.65}$$

The main features of the ZVS buck converter can therefore be summarised as follows.

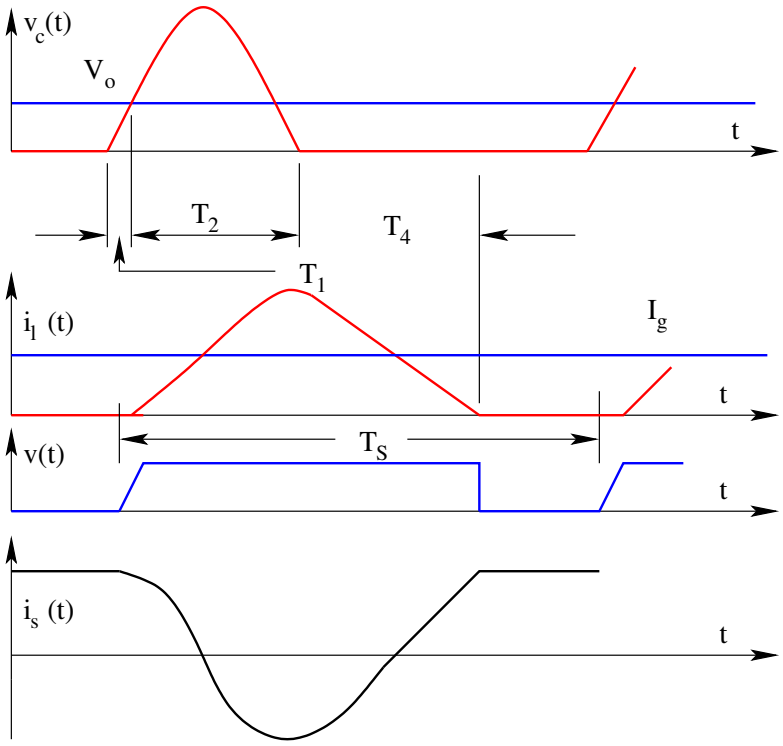

Figure 8.25: Circuit Waveforms of the Halfwave ZVS Converter

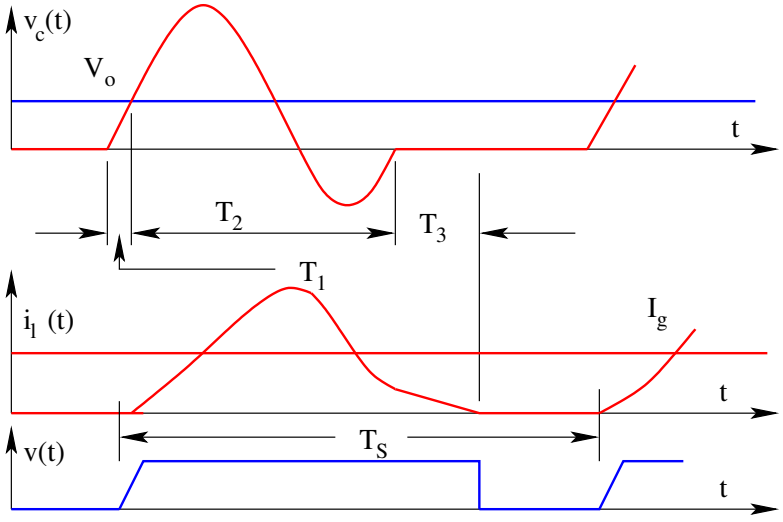

Figure 8.26: Circuit Waveforms of the Fullwave ZVS Converter

1. Device turn-on and turn-off happen at zero voltage. The ZVS technique is capable of being applied at much higher frequencies than ZCS. Device

output capacitance can be taken as part of the resonating capacitor C. Also, stray circuit inductances can be taken to form part of L_r, thus extending the frequency of operation.

2. While device current rating equals the output current I_o, the device voltage rating has to be greater than twice the battery voltage V_g.
3. Zero voltage switching is possible only if the load current is greater than $V_g\sqrt{\frac{C_r}{L_r}}$.
4. The sequence of events in each cycle is:
   (A) charging of the capacitor at constant current
   (B) resonant circuit operation
   (C) charging of the inductor at constant voltage
   (D) load current flowing through switch S_1.

It can be seen from the above that at the expense of increased voltage/current ratings for the switch and additional L and C components, switching losses are reduced to a large extent in quasi-resonant converters. The ZCS and ZVS switch configuration can in general be applied to any of the conventional PWM converter circuits, resulting in families of quasi-resonant converters. Of the two techniques to reduce switching losses, zero voltage switching has less switching losses and can therefore be applied at higher frequencies. It is also possible to make use of some of the stray circuit components such as device capacitances and wiring and leakage inductances as part of the resonant circuit.

8.4 Resonant Transition Phase Modulated Converters

Resonant transition converters were proposed more recently. They combine the low switching loss characteristics of the resonant converters and the low conduction loss and constant frequency characteristics of the PWM converters. The phase modulated full bridge converter (PMC), presented in the following section, belongs to this class of converters and offers ZVS characteristics. Except for resonant transition, it is identical to the square wave PWM full bridge topology. The design principles for the two schemes have many things in common. ZVS in PMC is obtained relying mainly on the parasitic components like the magnetising and leakage inductances of the power transformer and the output capacitance of the MOSFET switch. These features make PMC the preferred topology for high-voltage and high-frequency applications.

8.4.1 Basic Principle of Operation

In any double-ended converter, like the push-pull, half-bridge etc., it is possible to design for zero-voltage switching, if the duty-ratio is kept fixed at 50%. This

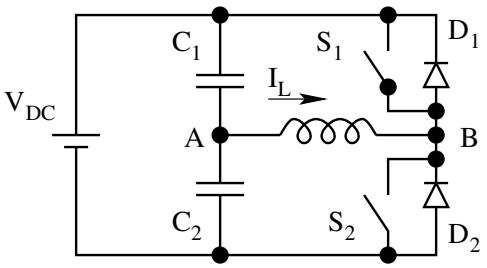

Figure 8.27: Half Bridge Converter

basic principle may be brought out by considering the half-bridge converter shown in Fig. 27. Consider S_2 conducting initially, resulting in the current I_L. As S_2 is switched off, the inductive nature of the load forces I_L to continue to flow in the same direction, but now completing the path through D_1 and C_1 . Since D_1 is conducting, the voltage across the switch S_1 is zero. Hence, turning on S_1 now, results in ZVS. The duration for which D_1 conducts depends of the nature of the load and the energy stored in it. Hence to reliably turn on S_1 with zero volts across it, it is necessary that it is switched on after S_2 is switched off and while D_1 is conducting. Similarly S_2 should be turned on after S_1 is turned off and D_2 is conducting. In a symmetrical half-bridge converter, this implies operating with the fixed duty ratio of 50%.

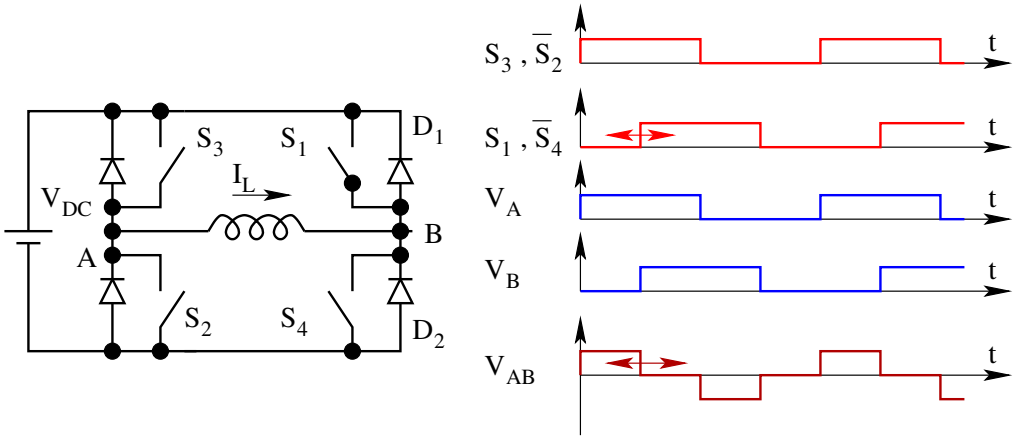

Figure 8.28: Resonant Transition Converter

With the duty ratio fixed at 50%, output regulation is not possible. Therefore, alternate methods have to be employed to achieve regulation. For the full-bridge topology, phase modulation, explained with the help of Fig. 28, is one such alternative. Figure 28 shows the simplified schematic of the phase-modulated full-bridge converter. Each of the four devices (S_1 to S_4) is operated at 50% duty-ratio. Hence the waveforms at points A and B are square-waves

with 50% duty-ratio as shown. Phase modulation simply refers to varying the phase-difference between these two square-waves, to achieve output control. Phase-difference of 180° corresponds to the maximum output voltage. As the phase-difference is reduced, the output reduces proportionately. Figure 28 shows the output for a phase-difference of about 90°. The sequence of operation in a complete cycle is explained in the next section.

8.4.2 Analysis of a complete cycle of operation

Figure 29 shows the schematic of PMC used for analysis and simulation. As may be seen, the circuit includes the parasitic elements like the output capacitance (C_1, C_2, C_3, and C_4)of the MOSFET and the magnetising (L_m) and leakage inductances (L_{LK}) of the transformer. Zero voltage switching demands that, before a MOSFET is switched on, its output capacitance be completely discharged. This discharge is accomplished by the energy stored in the magnetising and the leakage inductances. Therefore, these parameters are crucial from the ZVS viewpoint and have to be considered in the analysis.

For the purpose of analysis, a complete cycle of operation is divided into

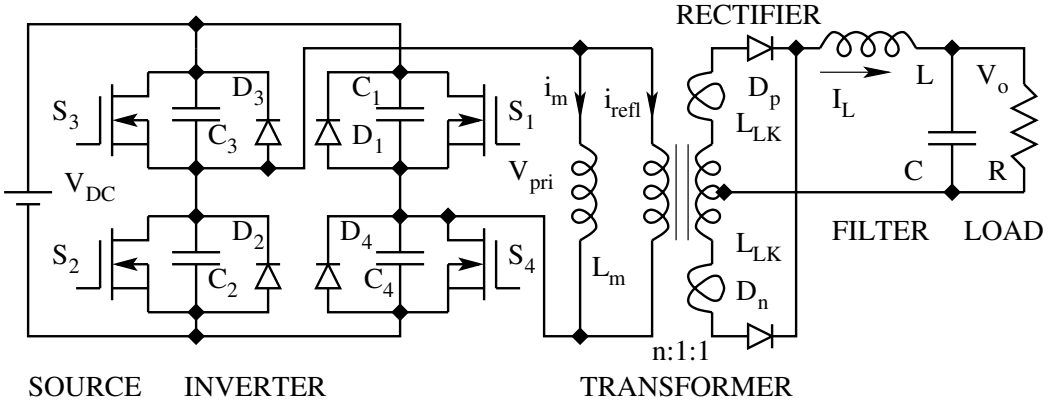

Figure 8.29: Schematic of a Resonant Transition Converter

eight distinct intervals for the inverter and four intervals for the secondary side rectifiers. The inverter and rectifier intervals are interdependent. The transformer primary currents are determined by the secondary side diode currents and the diode currents in turn depend on the magnitude and polarity of the inverter voltages. However, for ease of analysis they are considered separately. The inverter intervals are determined by the switching sequence of the devices. Figure 30 shows the inverter in interval 1, showing the devices conducting, and the current path. During this interval the diagonal switches S_3 and S_4 conduct, transferring power to the load. This interval ends when

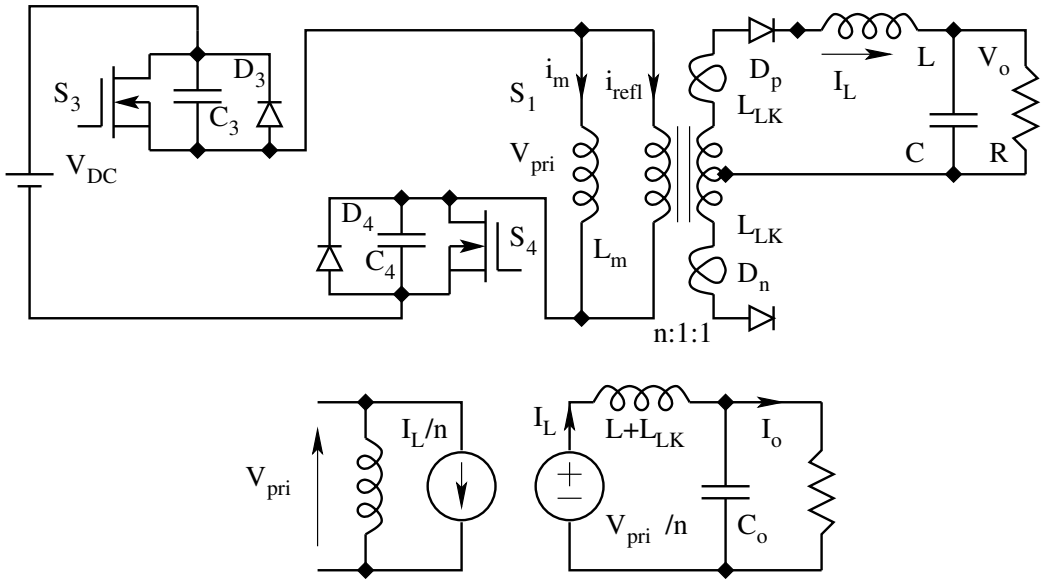

Figure 8.30: Equivalent Circuit of Resonant Transition Converter

S_4 is switched off. The governing equations for the inverter are,

$$L_m \frac{d}{dt} i_m = V_{pri} \tag{8.66}$$

$$i_{pri} = i_m + i_{refl} \tag{8.67}$$

$$i_{refl} = (i_{Dp} - i_{Dn})/n \tag{8.68}$$

The above three equations are general and are valid in all the intervals. The equations valid in interval 1 alone are,

$$V_{C1} = V_{C2} = V_{DC} \tag{8.69}$$

$$V_{C3} = V_{C4} = 0 \tag{8.70}$$

$$V_{pri} = V_{DC} \tag{8.71}$$

The second interval starts when S_4 is switched off. The primary current which was initially flowing through S_4 , now begins to flow through C_4 and C_1 as shown in Fig. 31. From the equivalent circuit shown in Fig. 31, the governing equations valid for this interval can be derived as below.

$$\frac{d}{dt} V_{C4} = \frac{i_{pri}}{2C} \; ; (C = C_1 = C_2 = C_3 = C_4) \tag{8.72}$$

$$V_{pri} = V_{C1} = (V_{DC} - V_{C4}) \tag{8.73}$$

The interval 2 ends when S_1 is switched on. The equivalent circuit for the other inverter intervals can be established by similar analysis and the corresponding

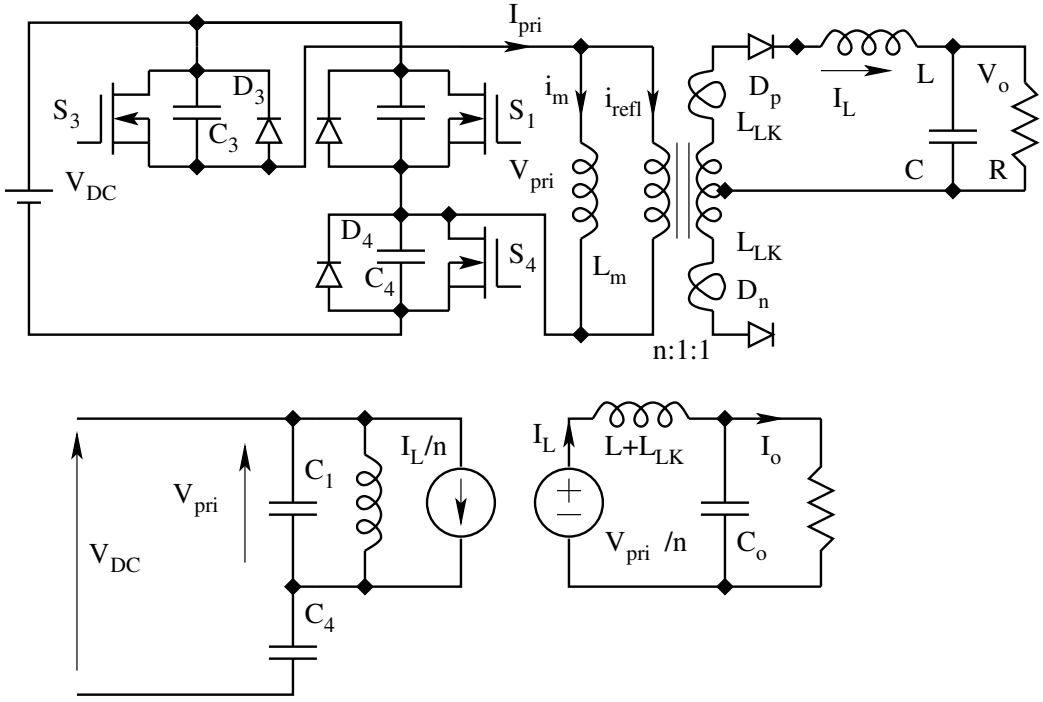

Figure 8.31: Equivalent Circuit of Resonant Transition Converter

Table 8.3: Sequence and Governing Equations of the Inverter Intervals

U	ON devices	From	to	V_{C1}	V_{C2}	V_{C3}	V_{C4}	V_{pri}
1	S_3, S_4	S_3 on	S_4 off	V_{DC}	V_{DC}	0	0	V_{DC}
2	S_3, C_4 C_1	S_4 off	S_1 on	$V_{DC} - V_{C4}$	V_{DC}	0	$\frac{dV}{dt} = \frac{i_{pri}}{2C}$	V_{C1}
3	S_3, D_1	S_1 on	S_3 off	0	V_{DC}	0	V_{DC}	0
4	D_1, C_3 C_2	S_3 off	S_2 on	0	$V_{DC} - V_{C3}$	$\frac{dV}{dt} = \frac{i_{pri}}{2C}$	V_{DC}	$-V_{C3}$
5	S_1, S_2	S_2 on	S_1 off	0	0	V_{DC}	V_{DC}	$-V_{DC}$
6	S_2, C_1 C_4	S_1 off	S_4 on	$\frac{dV}{dt} = \frac{i_{pri}}{2C}$	0	V_{DC}	$V_{DC} - V_{C1}$	$-V_{C4}$
7	S_2, D_4	S_4 on	S_2 off	V_{DC}	0	V_{DC}	0	0
8	S_4, C_2 C_3	S_2 off	S_3 on	V_{DC}	$\frac{dV}{dt} = \frac{i_{pri}}{2C}$	$V_{DC} - V_{C2}$	0	$-V_{C2}$

equations derived. Table 3 lists the start and end of each interval, and the equations valid in them.

The rectifier intervals are determined mainly by the transformer voltages. In the two inverter intervals (1 and 2), discussed above in detail, the transformer voltage remains positive. This period corresponds to the first rectifier interval (Table 4) in which diode D_p conducts. The next interval is reached

Table 8.4: Sequence and Governing Equations of the Rectifier Intervals

U	1	2	3	4
Devices	D_p	D_p, D_n	D_n	D_p, D_n
From	$i_{Dn} \leq 0$	$V_{sec} \leq \frac{L_{Lk}}{2}\frac{d}{dt}i_{Dp}$	$i_{Dp} \leq 0$	$V_{sec} \geq \frac{-L_{Lk}}{2}\frac{d}{dt}i_{Dn}$
To	$V_{sec} \leq \frac{L_{Lk}}{2}\frac{d}{dt}i_{Dp}$	$i_{Dp} \leq 0$	$V_{sec} \geq \frac{-L_{Lk}}{2}\frac{d}{dt}i_{Dn}$	$i_{Dn} \leq 0$
i_{Dp}	i_L	$i_L - i_{Dn}$	0	$\frac{di}{dt} = \frac{V_{sec}}{L_{Lk}}$
i_{Dn}	0	$\frac{di}{dt} = -\frac{V_{sec}}{L_{Lk}}$	i_L	$i_L - i_{Dp}$
V_{in}	V_{sec}	0	$-V_{sec}$	0
L^*	$L + L_{Lk}$	L	$L + L_{Lk}$	L

only when the transformer voltage changes polarity and gets forward biased. From Fig. 31, the condition for D_n to be forward biased, can be derived as

$$-V_{sec} \geq V_{sec} - L_{Lk}\frac{d}{dt}i_{Dp} \tag{8.74}$$

During this interval 2, known as the overlap interval, both D_p as well as D_n conduct, resulting in zero voltage across the output filter. The current through D_p decreases at the rate given by,

$$\frac{d}{dt}i_{Dp} = \frac{V_{sec}}{L_{Lk}} \tag{8.75}$$

and when it reaches zero, the next interval begins where D_n alone conducts. The equations valid in each of the four rectifier intervals are listed in Table 4. The next section outlines the design strategy for achieving ZVS.

8.4.3 Design considerations to achieve ZVS

From the analysis of the PMC, it is important to note that there are two types of transitions. One is from the power transfer mode to the freewheeling mode (inverter intervals 2 and 6) and the other from the freewheeling to the power transfer mode (intervals 4 and 8). From the ZVS viewpoint, these two transitions are quite different. In the transition from power transfer to freewheeling mode, referred to as the right-leg transition, the reflected load current is always in the proper direction to discharge the capacitance of the MOSFET to be turned on. Hence the load current aids the magnetising current in achieving ZVS. In the other transition, referred to as the left-leg transition, the reflected

load current begins to reverse direction, the rate of reversal being determined by the leakage inductance. Once the load current reverses direction, it opposes the magnetising current in the discharge of the MOSFET capacitance. Hence the left-leg transition is more critical from the ZVS standpoint. The design equations are therefore, derived to achieve ZVS in this transition, which automatically ensures ZVS for the other transition too.

Apart from the magnetising and leakage inductances, the other parameter which affects ZVS, is the dead time $[T_{delay}]$ allowed between the turn-off of a MOSFET and the subsequent turn-on of the other MOSFET in the same arm. All these parameters along with their qualitative effects on ZVS, are given in Table 5.

Table 8.5: Parameters affecting ZVS and their qualitative effects

Variable	Positive effect	negative effect
Magnetising current	Aids ZVS.	Higher current stress and conduction loss.
Leakage inductance	Aids ZVS, by reducing the rate of reversal of primary current in the intervals 4 and 8.	Reduces the maximum effective duty ratio; hence poor VA utilisation and more conduction loss. Results in higher ringing and dissipation in the secondary rectifiers.
T_{Delay}	Large T_{Delay} aids ZVS at light loads and affects adversely at high loads.	Large T_{Delay} reduces the effective duty ratio and is particularly undesirable at very high switching frequencies.
Capacitance across the MOSFET - C_{DS}	Large C_{DS} aids in lossless turn-off	Large C_{DS} demands more energy to be stored in the transformer inductances, to be fully discharged, hence bad for ZVS.

From the equations valid for the fourth inverter interval (left-leg transition which is the crucial one for ZVS) the following expression can be derived, for the voltage V_{C2} across the MOSFET to be turned on.

$$V_{C2} = V_{DC} - (i_m + i_{refl})\sqrt{\frac{L_{eq}}{2C}}\ sin\ \omega t \tag{8.76}$$

where,

$$\omega = \frac{1}{\sqrt{2CL_{eq}}}$$

$L_{eq} = L^*_{Lk}||L_m$; (L^*_{Lk} – leakage inductance referred to the primary)

The above expression gives the following two conditions to achieve ZVS at any given load.

$$(i_m + i_{refl})\sqrt{\frac{L_{eq}}{2C}} \geq V_{DC} \tag{8.77}$$

$$T_{Delay} = \frac{\pi}{2}\sqrt{2CL_{eq}} \tag{8.78}$$

The first condition ensures that the peak of the sinusoidal component of Eq. (76) is atleast equal to V_{DC}, so that V_{C2} eventually reaches zero. The second condition ensures that the MOSFET is switched on when V_{C2} is zero. Hence the design strategy is to,

1. Select T_{delay} considering the switching frequency and the MOSFET characteristics.
2. Calculate the value of L_{Lk} from Eq. (78), with the above value of T_{Delay}.
3. With the above value of L_{Lk}, calculate from Eq. (77), the peak magnetising current required at any load down to which ZVS is required.

The full system may be numerically simulated with the help of equations listed in Tables 3 and 4, and using the above values for delay time, magnetising current and leakage inductance as initial estimates. From repeated simulation runs, more satisfactory design values for all the parameters may be found.

8.4.4 Development Examples

The following specifications refer to two PMC rated for 560W and 30W respectively developed at the Indian Institute of Science. The various tech-

Table 8.6: Parameters affecting ZVS and their qualitative effects

	Model 1	Model 2
Input	150 – 270 V ac, 50 Hz	30 – 52 V dc
Output Voltage	28 V	5 V
Maximum Output Current	20 A	6 A
Output Regulation	0.1 %	0.1 %
Output Ripple (peak to peak)	0.5 %	0.5 %
Switching Frequency	250 kHz	500 kHz
Efficiency	82 %	84 %
Power Density	5 W/cubic inch	7.5 W/cubic inch

nologies which are evolving in the area of soft switching converters, are the resonant load, resonant switch and the resonant transition converters. The

first two were briefly reviewed and the third was covered in detail. With its ZVS characteristics and constant-frequency control, the phase-modulated full-bridge converter is well suited for high-voltage and high-power applications. Results obtained on a 560W/250kHz off line converter, and a 30W/500kHz dc to dc converter are presented to substantiate this claim.

The advantages of PMC are more striking in applications where the range of input variation is not too wide. One such important application area is in high-power converters with front end powerfactor control [PFC] scheme.

The following links give the data sheets on a few commercially available ICs suitable for soft switching converters.

Phase modulated converter controller

Quasi-resonant converter controllers

8.5 Resonant Switching Converters with Active Clamp

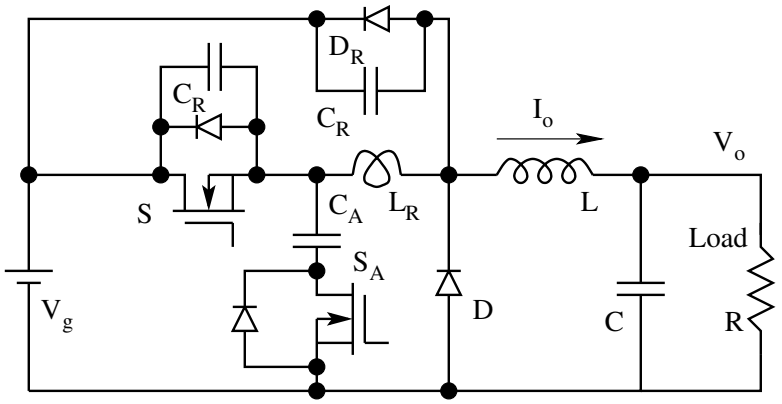

Figure 8.32: Hard Switching and Active Clamped ZVS Buck Converter

Another family of ZVS and ZCS converters proposed recently is classified as resonant converters with active clamp. These converters have the advantage of constant frequency PWM control, soft commutation and low voltage stress on account of clamping action, and simple dynamics. The concept is applicable to a variety of circuit topologies. This section will present the principle of operation and control of such converters along with a method of analysis of this family of converters. Figure 32 shows the resonant switching buck converter with active clamp. The switching device S, D, L, C, and R form the Buck Converter. The active clamp converter has several additional circuit elements. The active clamp ZVS circuit is obtained by applying the following rules.

1. C_R in parallel with the main switch S.

2. L_R in series with the main switch S.
3. C_R and D_R in parallel with S and L_R.
4. Clamp capacitor C_A and clamp switch S_A from the mid-point of switch S and L_R to a clamp point. Any fixed potential can serve as a clamp point.

8.5.1 Analysis of Active Clamp ZVS Buck Converter

The ZVS buck converter with active clamp, illustrated for analysis, is presented along with the idealised wavefors. The operation of the circuit follows sequentially several sub-circuits. Figure 33 shows the state of the converter prior to time $t = 0$. The output circuit is idealised as a current sink of magnitude I_o. The load current is free-wheeling through the free-wheeling diode D. The clamp circuit is carrying current in the path C_A, S_A, D, and L_R. The current in the resonant inductor L_R is negative ($-I^*$). The capacitor C_R across the source node and the free-wheeling diode node is charged to V_g. The main device S is off.

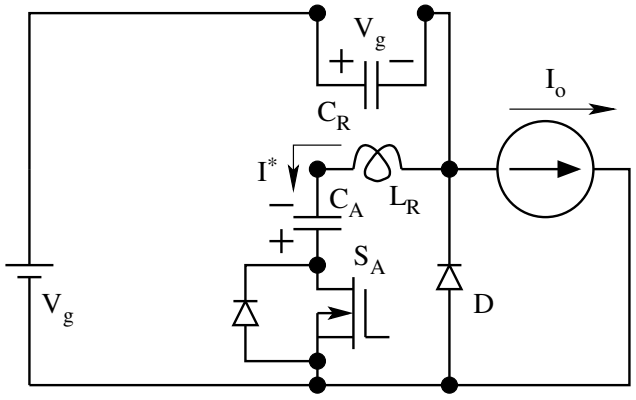

Figure 8.33: The Equivalent Circuit of the Converter prior to $t = 0$

Interval T1

Interval 1 immediately following $t = 0$ has a duration T_1. This interval is initiated when the switch S_A is switched off. Instantly the current from S_A is transferred to the switch S. This current flows through the body diode of the main switch S. During the interval T_1, both D and S are on. At the end of interval T_1, the current in S builds up and reaches I_o. At this instant, the free-wheeling diode goes off. The equivalent circuit in this interval is given in Fig. 34. The circuit equation governing this interval is

$$\frac{di}{dt} = \frac{V_g}{L_R} \tag{8.79}$$

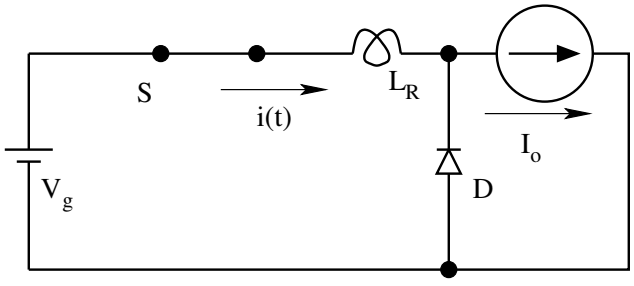

Figure 8.34: The Equivalent Circuit of the Converter in Interval T_1

The initial condition on the current is $i(0) = -I^*$; The switch current (inductor L_R current) $i(t)$ in interval T_1 is given by

$$i(t) = -I^* + \frac{V_g}{L_R} t \tag{8.80}$$

$$i(T_1) = I_o \tag{8.81}$$

$$T_1 = \frac{I + I^*}{V_g} L_R \tag{8.82}$$

We define a normalised current I_N. This will be useful in establishing the performance parameters of the converter later. Normalised current is defined in terms of pole current I_o, throw voltage V_g, and the switching period T_s.

$$I_N = \frac{L_R I_o}{V_g T_s} \tag{8.83}$$

Interval T2

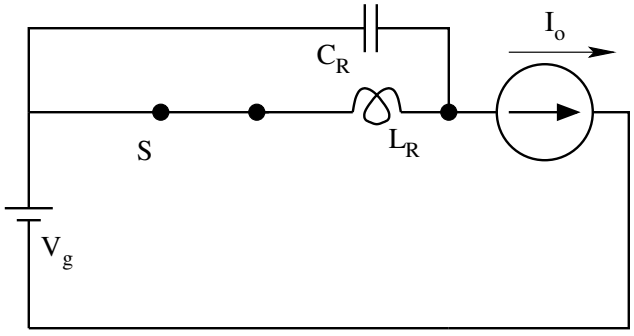

Figure 8.35: The Equivalent Circuit of the Converter in Interval T_2

Interval 2 follows immediately the interval T_1. The equivalent circuit in this interval is given in Fig. 35. This interval is initiated when the free-wheeling

diode D goes off. The initial current on the resonant inductor L_R is I_o. The initial voltage on the resonant capacitor C_R is V_g. During this interval, the capacitor loses its voltage from V_g to 0. At the end of this interval, the diode across C_R starts conducting. The resonant inductor current $i(t)$, the resonant capacitor voltage $v(t)$ during this interval, the resonant capacitor voltage at the end of this interval $v(T_2)$, and the duration of this interval T_2 are all given by the following equations.

$$i(t) \;=\; I_o \;+\; V_g \sqrt{\frac{C_R}{L_R}}\; sin\; \frac{t}{\sqrt{L_R C_R}} \tag{8.84}$$

$$v(t) = V_g\; cos\; \frac{t}{\sqrt{L_R C_R}} \tag{8.85}$$

$$v(T_2) \;=\; 0 \tag{8.86}$$

$$T_2 \;= \frac{\pi}{2}\; \sqrt{L_R C_R} \tag{8.87}$$

Interval T3

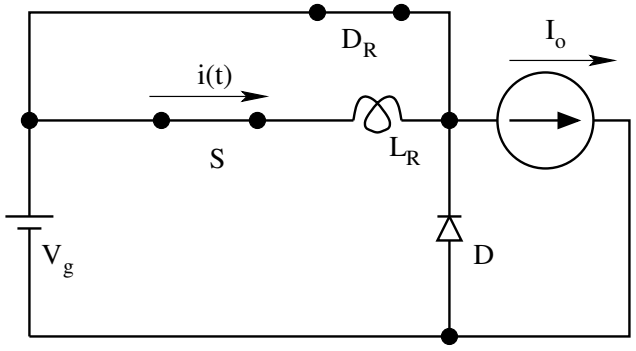

Figure 8.36: The Equivalent Circuit of the Converter in Interval T_3

Figure 36 shows the equivalent circuit of the converter during the interval T_3. During this interval the initial current in the resonant inductor L_R is $I_o \;+\; V_g \sqrt{\frac{C_R}{L_R}}$.

$$L_R \frac{di}{dt} \;=\; 0 \tag{8.88}$$

$$i(t) \;=\; I_o \;+\; V_g \sqrt{\frac{C_R}{L_R}} \tag{8.89}$$

$$T_1 \;+\; T_2 \;+\; T_3 \;=\; DT_s \tag{8.90}$$

This interval ends at the end of the on time DT_s. The inductor current during this interval stays constant as given in Eq. [89]. At the end of this interval the switch S is turned off.

Interval T4

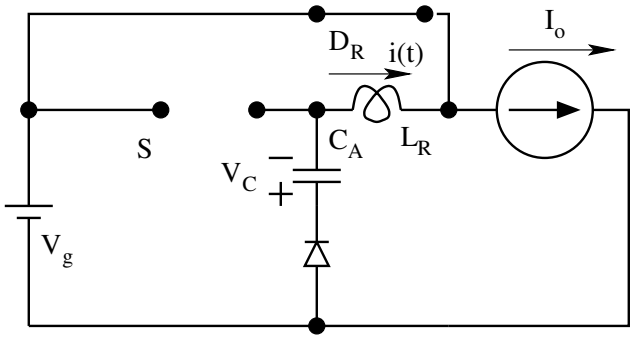

Figure 8.37: The Equivalent Circuit of the Converter in Interval T_4

Figure 37 shows the equivalent circuit of the converter in the interval T_4. The initial condition on the inductor current is $i(0) = I_o + V_g \sqrt{\frac{C_R}{L_R}}$. The clamp capacitor voltage is V_C. Define $V_C = \beta V_g$. The governing equation of the resonant inductor current is

$$L_R \frac{di}{dt} = -(V_g + V_C) \tag{8.91}$$

The inductor current $i(t)$ in this inteerval is given by

$$i(t) = I_o + V_g \sqrt{\frac{C_R}{L_R}} - \frac{V_g + V_C}{L_R} t \tag{8.92}$$

This interval T_4 gets over when $i(t)$ drops to I_o.

$$i(T_4) = I_o \tag{8.93}$$

The interval T_4 is as follows.

$$T_4 = \frac{V_g}{V_g + V_C} L_R \sqrt{\frac{C_R}{L_R}} = \frac{1}{1+\beta} \frac{1}{2\pi f_r} ; \; f_r = \frac{1}{2\pi\sqrt{L_R C_R}} \tag{8.94}$$

D_R goes off at the end of T_4.

Interval T5

The equivalent circuit of the converter in interval T_5 is given in Fig. 38. V_g, V_C, L_R, C_R form a resonant loop. The initial inductor (L_R) current is (I_o).

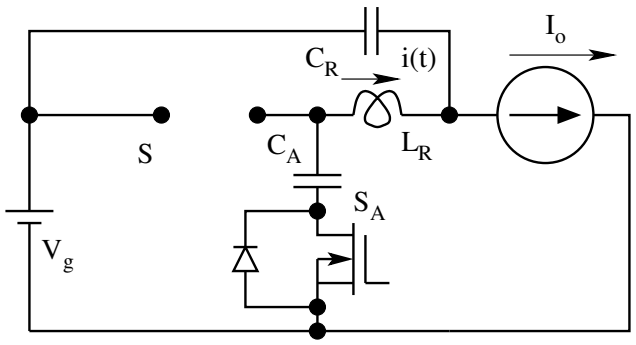

Figure 8.38: The Equivalent Circuit of the Converter in Interval T_5

The initial capacitor C_R voltage is 0. The inductor (L_R) current $i(t)$, and the capacitor (C_R) voltage $v(t)$ are as follows.

$$i(t) \;=\; I_o \;-\; (V_g + V_C)\,\sqrt{\frac{C_R}{L_R}}\;sin\frac{t}{\sqrt{L_R C_R}} \tag{8.95}$$

$$v(t) \;=\; (V_g + V_C)\left[\;1 \;-\; cos\frac{t}{\sqrt{L_R C_R}}\right] \tag{8.96}$$

The end of this interval is when the capacitor voltage $v(t)$ reached V_g.

$$T_5 \;=\; \sqrt{L_R C_R}\;cos^{-1}\frac{\beta}{1+\beta} \tag{8.97}$$

The inductor current $I(T_5)$ is given by

$$I(T_5) \;=\; I_o \;-\; V_g(1+\beta)\sqrt{\frac{C_R}{L_R}} \tag{8.98}$$

At the end of interval T_5, the capacitor is charged to V_g, and the free-wheeling diode starts conducting.

Interval T6

The equivalent circuit of the converter in interval T_6 is shown in Fig. 39. During this interval, the inductor (L_R) current at the start is $I(T_5)$. The governing equations of the inductor current are given by

$$L_R\frac{di}{dt} \;=\; -\,V_C \tag{8.99}$$

$$i(t) \;=\; I(T_5) \;-\; \frac{V_C}{L_R}\,t \tag{8.100}$$

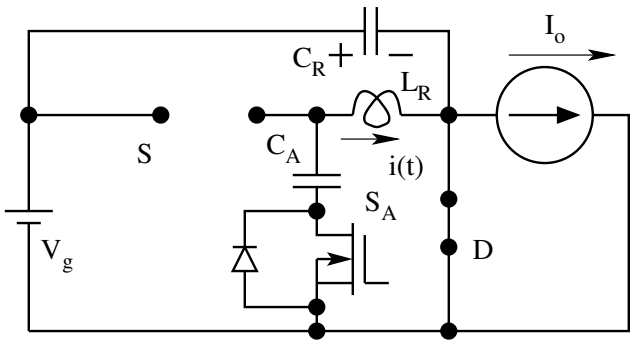

Figure 8.39: The Equivalent Circuit of the Converter in Interval T_6

This interval ends after T_6 when the switching period T_s ends. At the end of interval T_6, the inductor current ramps down to $kI(T_5)$. Immediatly following T_6, the next interval starts, which is the same as the first interval T_1.

$$kI(T_5) \;=\; -I^* \tag{8.101}$$

Resonant Inductor Current Waveform

Figure 40 shows the steady state current of the resonant inductor L_R. Notice the six sub-periods T_1 to T_6 explained above.

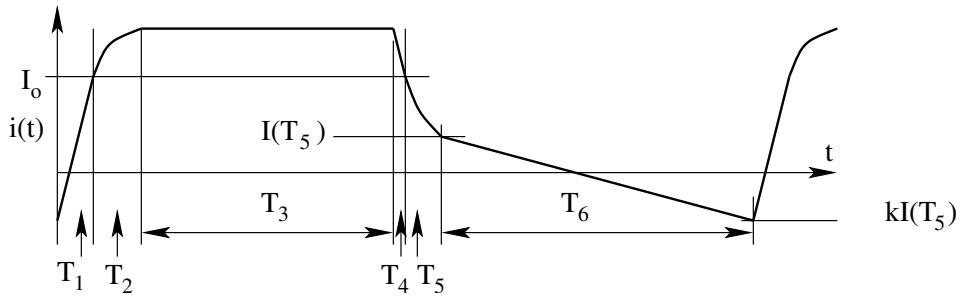

Figure 8.40: Steady State Periodic Current in Resonant Inductor L_R

Clamp Capacitor Current Waveform

Figure 41 shows the steady state current of the clamp capacitor C_A. The sub-periods of relevance are T_4 to T_6 explained above.

Evaluation of β and k

The steady state performance of the converter is dependent on the clamp capacitor voltage or indirectly β. Under steady-state, the clamp capacitor

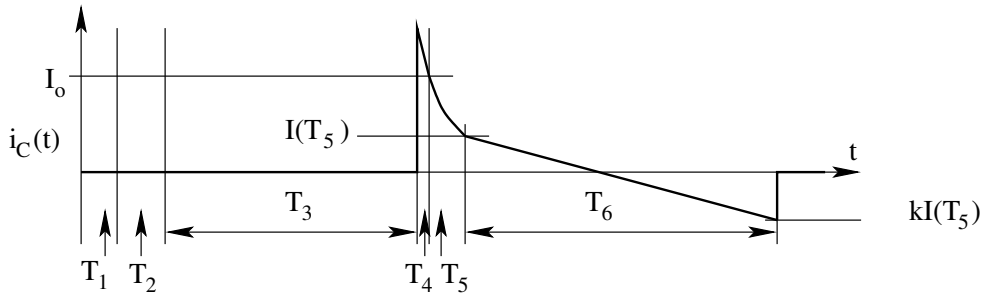

Figure 8.41: Steady State Periodic Current in Clamp Capacitor C_A

voltage is constant. Therefore the average clamp capacitor current over a period has to be zero. This is done by evaluating the quantity of charge transferred to the capacitor in one period.

$$Q(T_4) \; + \; Q(T_5) \; + \; Q(T_6) \; = \; 0 \tag{8.102}$$

$$Q(T_4) \; = \; I_o T_4 \; + \; \frac{V_g C_R}{2(1+\beta)} \tag{8.103}$$

$$Q(T_5) \; = \; I_o T_5 \; - \; V_g C_R \tag{8.104}$$

$$Q(T_6) \; = \; \frac{I(T_5) T_6 (1-k)}{2} \tag{8.105}$$

From the above, k can be related to the other variables as follows.

$$k-1 \; = \; 2 \left[\frac{I\left((1-D)T_s - T_6\right) \; - \; \dfrac{V_g C_R (1+2\beta)}{2(1+\beta)}}{I(T_5) T_6} \right] \tag{8.106}$$

β is related to the other variables from the current slope in interval T_6.

$$\frac{V_C}{L_R} \; = \; \frac{(k+1) I(T_5)}{T_6} \tag{8.107}$$

By substituting for $I(T_5)$ from Eq. [98], β is evaluated as follows.

$$\beta \; = \; A \left(I_N \; - \; \frac{f_S}{2\pi f_R} \right) \; ; \; A \; = \frac{\dfrac{(k+1)T_s}{T_6}}{\left(1 + \dfrac{(k+1)T_s}{T_6} \dfrac{f_S}{2\pi f_R} \right)} \tag{8.108}$$

Design Methodology

Stsrting with an initial value of V_C, and $kI(T_5)$, one may compute sequentially through the six intervals to obtain a steady state solution. A spreadsheet design may conveniently be used. The first guess for the initial current $kI(T_5)$

and V_C may be entered and re-entered from the computed values till convergence is obtained. The number of iterations in most cases is not more than 3. The design constraints are the following.

1. $f_R >> f_S$. The resonant frequency of the circuit elements L_R and C_R is chosen much greater than the switching frequency.
2. $V\sqrt{\frac{C_R}{L_R}} > I_{min}$

8.5.2 Steady State Conversion Ratio

The conversion ratio $M = \frac{V_o}{V_g}$ can be evaluated by averaging the pole voltage over a full cycle. The pole voltage for the buck converter is shown in Fig. 42. Under the assumption that the resonant frequency is much higher than the

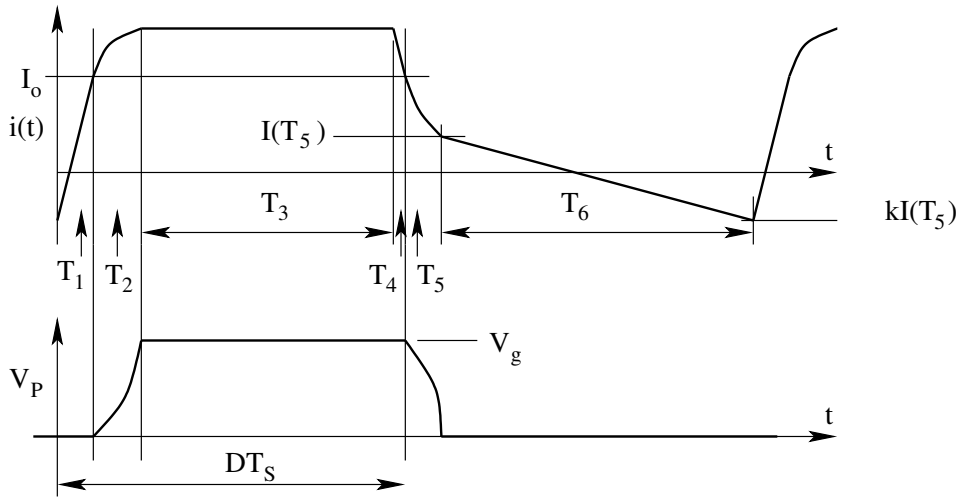

Figure 8.42: Steady State Pole Voltage of the Active Clamp Buck Converter

switching frequency, the conversion ratio for the buck converter is

$$M = \frac{V_o}{V_g} = D - (1+k)I_N \tag{8.109}$$

8.5.3 Equivalent Circuit

The conversion ratio (V_o/V_g) for active-clamp buck converter may be simplified as follows.

$$\frac{V_o}{V_g} = D - I_N(1+k) = D - \frac{L_R I_o(1+k)}{V_g T_s} \tag{8.110}$$

$$V_o = DV_g - \frac{L_R(1+k)}{T_s} I_o \tag{8.111}$$

Equation [111] may be represented by the equivalent circuit shown in Fig. 43.

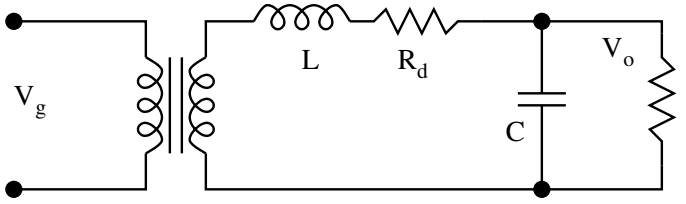

Figure 8.43: Equivalent Circuit of Active Clamp Buck Converter

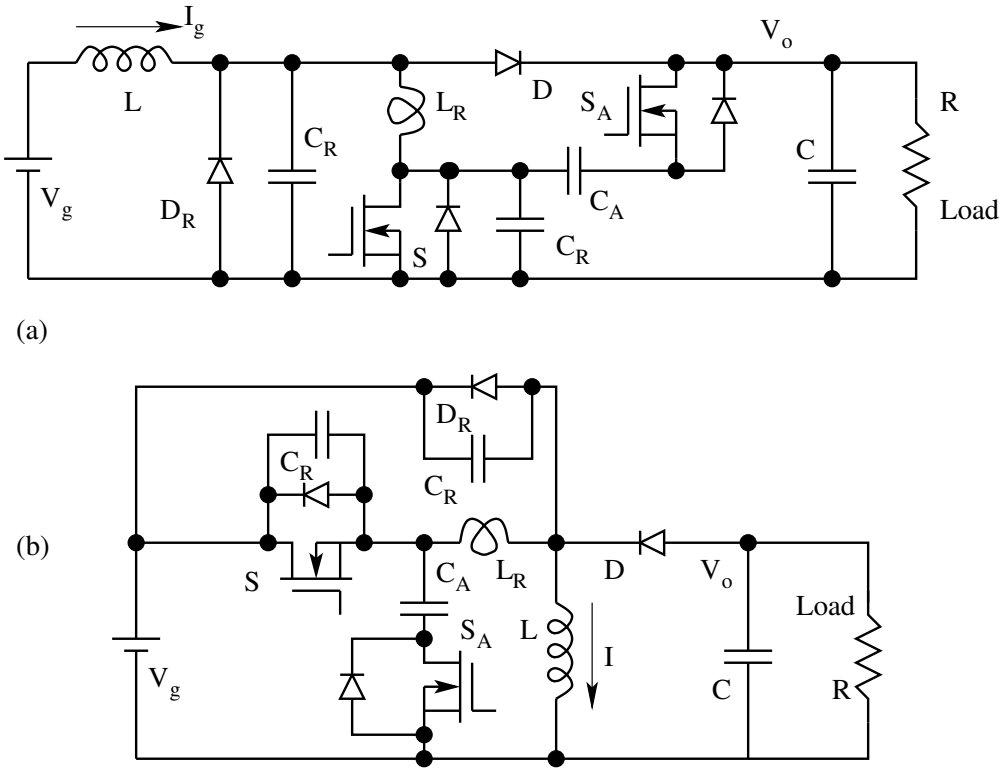

Figure 8.44: Active Clamp (a) Boost and (b) Buck-Boost Converters

Figures 44 shows the active-clamp versions of the (a) non-isolated boost and (b) non-isolated buck-boost converters. The equivalent circuits of the various active clamp converters are shown in Fig. 45. Table 7 gives the equivalent circuit parameters.

ZVS converters with active clamp retain the simple features of the hard switched counterparts. In addition, ZVS converters with active clamp exhibit loss-less damping in their dynamic performance. As a result closed loop compensators for this family of converters are easier to design. More details including the dynamic model and transfer functions of the ZVS converters

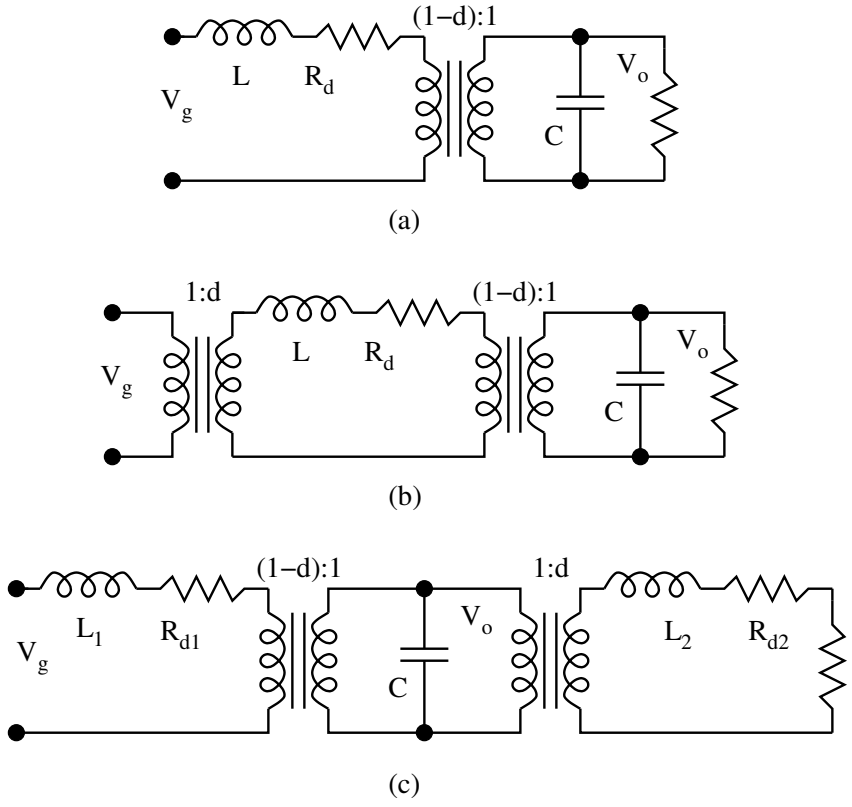

Figure 8.45: Equivalent Circuits of Different Active Clamp Converters

Table 8.7: Equivalent Circuit Parameter for the Different Converters

Converter	V	I	R_d	M
Buck	V_g	I_o	$\frac{(1+k)L_R}{T_s}$	$D-(1+k)I_N$
Boost	V_o	I_g	$\frac{(1+k)L_R}{T_s}$	$\frac{1}{(1-D)+(1+k)I_N}$
Buck-Boost	V_g+V_o	I_L	$\frac{(1+k)L_R}{T_s}$	$\frac{D-(1+k)I_N}{(1-D)+(1+k)I_N}$
Cuk	V_g+V_o	I_g+I_o	$\frac{(1+k)L_R}{(1-D)T_s}$ $\frac{(1+k)L_R}{DT_s}$	$\frac{D-(1+k)I_N}{(1-D)+(1+k)I_N}$

with active clamp are given in the following link.
(Unified Model for Converters with Active Clamp)

8.6 Problem Set

1. Draw the halfwave and fullwave versions of the quasi-resonant ZCS and ZVS circuits for the three basic non-isolated converter topologies.

2. For each of these circuits, write down the conversion factors (V_o/V_g) as a function of σ and (f_s/f_o). You may be able to do this without deriving the gain mathematically, but by recognising the nature of the result from what has been obtained for the two converters in the text. For each of these converters write down the expressions for the dimensionless parameter σ and state the condition such that resonant operation is possible.

3. The expression for $G_h(s)$ is given in Eq. (48). Evaluate the functions $dG_h(s)/dt$ as sums of partial derivatives with respect to the different variables. Explain in what way this result is significant in obtaining the small signal model of the converter. You may demonstrate your answer through the example shown in Fig. 20.

4. Figure P4 shows a buck converter designed to operate at 20 kHz at a duty ratio of D = 0.43, with an inductor current ripple of 0.2 A and a voltage ripple of 120 mV. It is desired to convert the circuit into a zero current switching quasi-resonant converter operating at around 200 kHz.

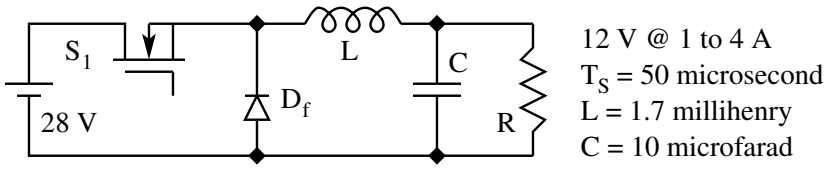

Fig. P 8.4: Hard Switched Buck Converter

   (A) Will you select halfwave or fullwave operation?

   (B) Show the circuit topology including the resonant components.

   (C) What will be the approximate resonant frequency? Design the value of the resonant components.

   (D) To obtain the same output inductor current ripple and output voltage ripple, what will be the new value of L and C? (Make suitable simplifying assumptions).

5. Figure 5 shows the active clamped zero voltage switching boost converter. The switch S_1 and D are the main switches. The resonant elements are

L_R and C_R. The switches, S_2, D_2, and C form the active clamp circuit. Figure 9 also shows the periodic current $i(L_R)$ through the resonant inductor L_R. Several sub-intervals are also shown.

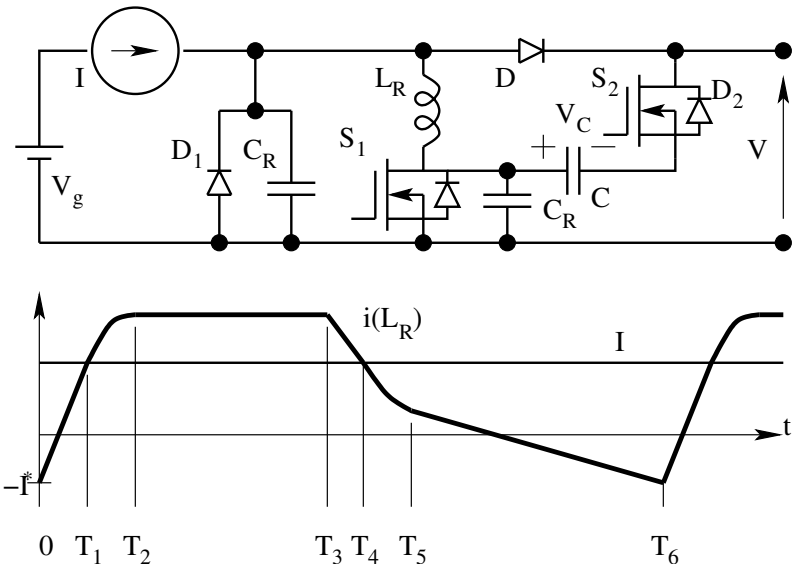

Fig. P 8.5: Active Clamped ZVS Boost Converter

(A) Sketch the equivalent circuit determining the inductor current in each of the intervals 0 to T_1, T_1 to T_2, T_2 to T_3, T_3 to T_4, T_4 to T_5, and T_5 to T_6.

(B) Write down the equations relating the rate of change of inductor current $di(L_R)/dt$ in the intervals 0 to T_1, T_2 to T_3, and T_5 to T_6

Chapter 9

Unity Power Factor Rectifiers

This chapter introduces a family of off-line power supplies which draw unity power factor sinusoidal current from the ac mains. Figure 1 shows the front end of off-line rectifiers with capacitive and inductive filter respectively. Fig-

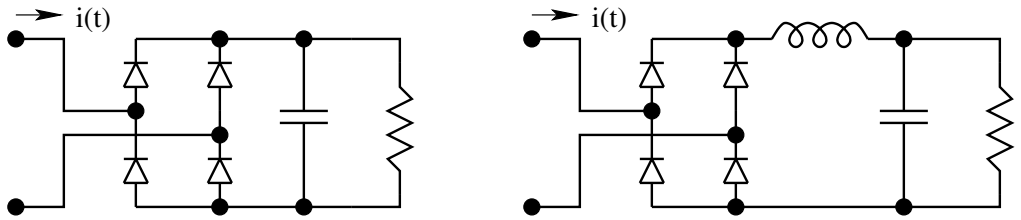

Figure 9.1: Off-line Rectifiers with Capacitive or Inductive Filter

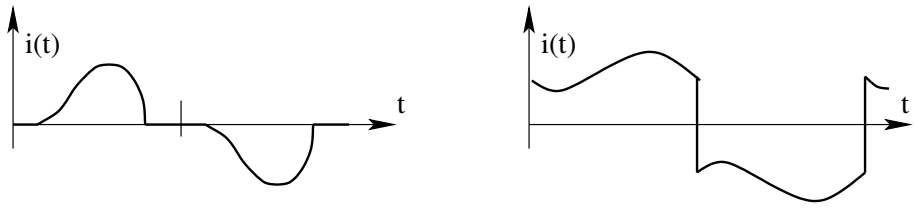

Figure 9.2: Input Current in Off-line Rectifiers in Fig. 1

ure 2 shows the input current in such front-end rectifiers. Poor power factor, High crest factor, and harmonic distorion are the undesirable features typical of these converters. It is seen that the inpur current in such rectifiers is non-sinusoidal with substantial harmonic content. The current concern on power quality in distribution end addresses this issue. Accordingly several recommendations and specifications are being laid down to ensure sinusoidal input current in off-line power supplies. IEC 555 and IEEE 519 are some of these recommendations.

9.1 Power Circuit of UPF Rectifiers

Almost all UPF rectifiers adopt the boost converter as the active power stage. Figure 3 shows the power stage of such a circuit. The switch S is controlled at

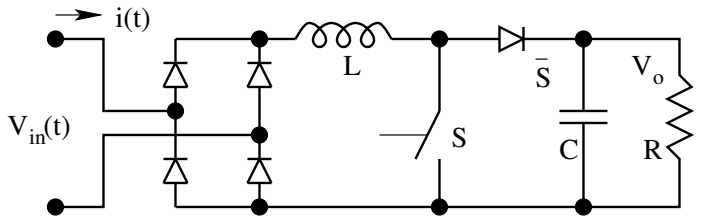

Figure 9.3: Power Stage of a UPF Off-line Rectifier

high switching frequency with pulse width modulation (PWM). The constraint on the output voltage for proper control is as follows.

$$V_o \;=\; max\,[V_{in}(t)] \tag{9.1}$$

9.1.1 Universal Input

The current trend is to design the off-line converters suitable for universal input. Universal input covers 110 V ac, 60 Hz, as well as 230 V ac, 50 Hz. Such converters are made suitable for ac inputs ranging from 90V ac to 270 V ac. In such a case, the dc output voltage is designed to be higher than the peak of the highest input voltage. A typical and popular output voltage is 400 V dc.

9.2 Average Current Mode Control

The switch modulation in such a case is made such that the average current flowing through the inductor L is a rectified sinusoid. The rectified sinusoidal current reference is derived from the rectified voltage of the input diode rectifier. The concept is illustrated in Fig. 4. The current control is obtained with a current controller shown as $H_i(s)$. It is usual to employ a simple PI controller for this purpose. It is usual that the output voltage is required to be regulated. Therefore it is customary that an outer voltage controller is employed around the current controller as shown in Fig. 5. The block shown as $H_v(s)$ is the voltage controller. The voltage controller output is multiplied with the rectified sinusoid to obtain the desired I_{ref}. The voltage controller is also usually a PI controller.

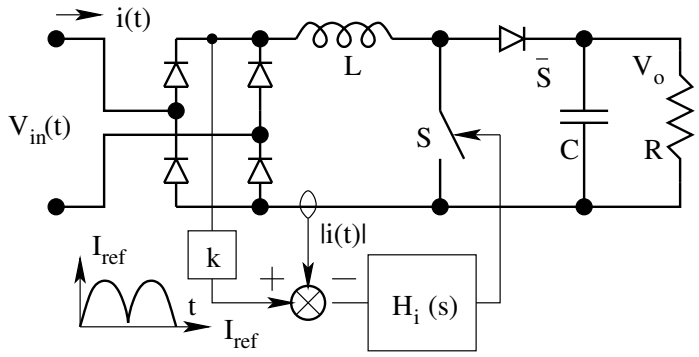

Figure 9.4: Average Current Controlled Rectifier

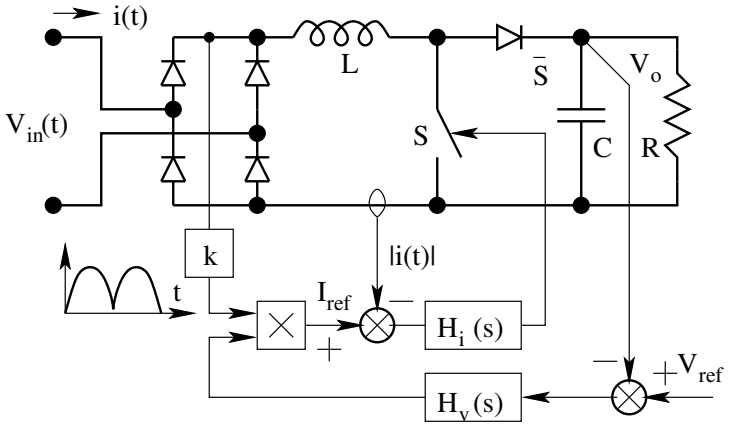

Figure 9.5: Voltage Regulated UPF Rectifier

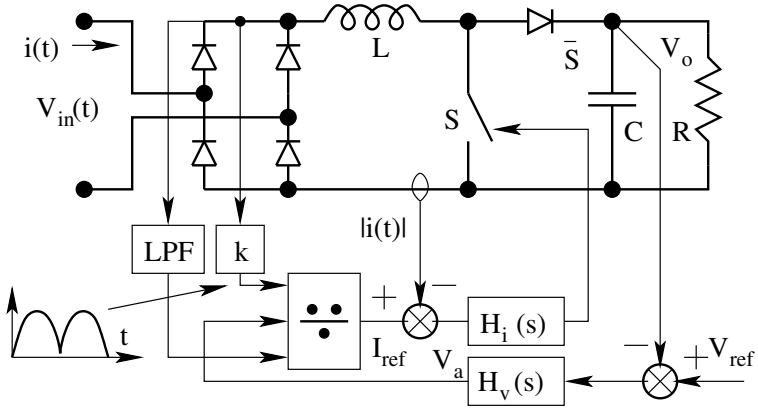

Figure 9.6: Voltage Regulated UPF Rectifier with Voltage Feedforward

9.2.1 Voltage Feedforward Controller

Several IC manufacturers have proprietory chips useful for the UPF rectifier application. Figure 6 shows the conceptual block diagram of a popular IC (UC3854). Notice that the current reference is evaluated as follows.

$$I_{ref} \;=\; \frac{k\;|v(t)|\;V_a}{V_{in}(rms)} \tag{9.2}$$

The application note of the IC may be referred (UC3854 Application)for details. The control circuit is quite complex. On account of the low pass filter employed for feed-forward, absolute value circuit and multiplier/divider used for current reference generation, there are several non-linearities in the circuit. The harmonic distortion performance therefore involves strong trade-offs.

9.3 Resistor Emulator UPF Rectifiers

A whole family of control methods has emerged in the recent past which overcomes the earlier state-of-the-art. The power circuit employed is the same. The concept is illustrated in the following. The power circuit of the rectifier is shown in Fig. 7. The switch S is modulated to have a duty cycle $d(t)$ which

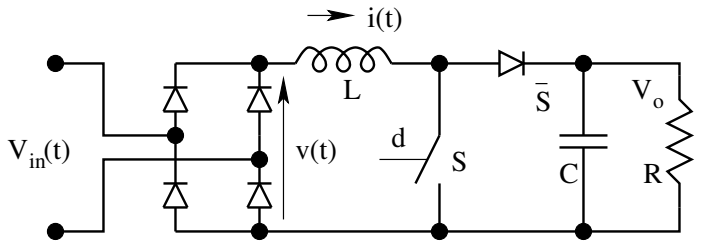

Figure 9.7: Concepts behind Resistor Emulator Control

is a function of time. The circuit characteristics ($v(t)$ vs $i(t)$) is governed by the following equation.

$$i(t) \;=\; f_1\left[v(t), V_o, d(t)\right] \tag{9.3}$$

In order to obtain UPF operation, the converter characteristics has to match that of a resistor. This control objective may be expressed as follows.

$$i(t) \;=\; \frac{v(t)}{R_e} \tag{9.4}$$

where R_e is the circuit emulated resistance. Suitable approximation is employed with Eq. [3] & [4], to obtain the following control characteristics.

$$d(t) \;=\; f\left[i(t), V_o, R_e\right] \tag{9.5}$$

There are several different realisations of the concept. Some of them are illustrated in the following.

9.3.1 Non-linear Carrier Control

The following relationship is the converter characteristics.

$$i_g(t) = \frac{v_g(t)}{R_e} \tag{9.6}$$

$$i_g(av) = \frac{v_g(av)}{R_e} \tag{9.7}$$

$$i_g(av) = \frac{V_o(1-d)}{R_e} \tag{9.8}$$

Considering the switch current $i_s(av) = d\ i_g(av)$, we get

$$d\ i_g(av) = \frac{V_o d(1-d)}{R_e} \tag{9.9}$$

In order to obtain a suitable method of modulation, d may be replaced by $\frac{t}{T_s}$,

$$\int_0^{dT_s} i_s(t)dt = \frac{V_o}{R_e}\ \frac{t}{T_s}\ \left(\ 1\ -\ \frac{t}{T_s}\right) \tag{9.10}$$

Figure 8 shows a modulation method to evaluate the duty ratio to satisfy Eq.

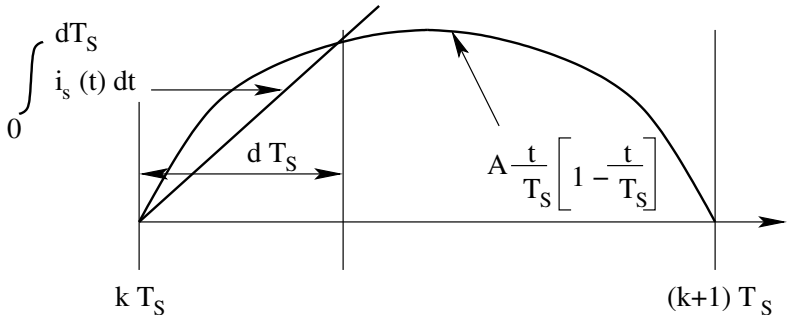

Figure 9.8: Non-linear Carrier Based Control

[10]. This method of obtaining upf operation of the boost converter is named the non-linear carrier control based resistor emulation.

9.3.2 Scalar Controlled Resistor Emulator

Consider the converter characteristics given by the following equation.

$$i_g(t) = \frac{v_g(t)}{R_e} \tag{9.11}$$

$$i_g(av) = \frac{v_g(av)}{R_e} \tag{9.12}$$

$$i_g(av) \;=\; \frac{V_o(1-d)}{R_e} \tag{9.13}$$

In order to obtain a suitable method of modulation, d may be replaced by $\frac{t}{T_s}$,

$$i_g(av) \;=\; \frac{V_o}{R_e}\left(\,1\;-\;\frac{t}{T_s}\right) \tag{9.14}$$

Figure 9 shows a modulation method to evaluate the duty ratio to satisfy Eq. [14]. This method of obtaining upf operation of the boost converter is named the scalar controlled resistor emulation. This method is suitable for polyphase rectifiers as well. Additional features of scalar control is given (Scalar Controlled Resistor Emulator) in this link. A predictive switching modulator for current mode control of high power factor boost rectifier is available (Linear Predictive Resistor Emulator) at this link.

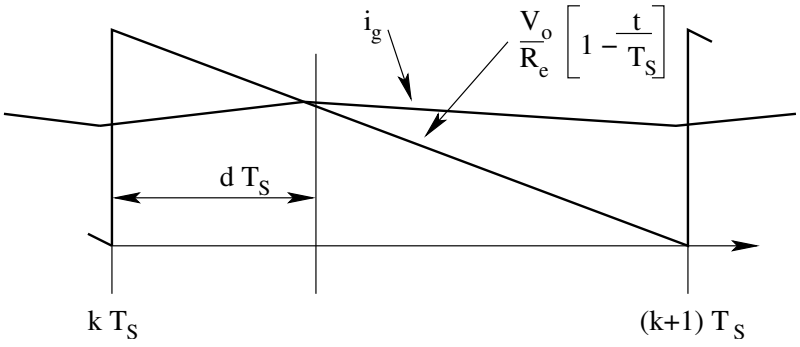

Figure 9.9: Scalar Controlled Resistor Emulation

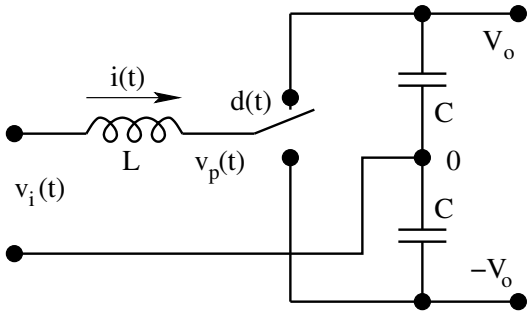

Figure 9.10: Power Circuit of a Single Phase Rectifier

9.3.3 Single Phase and Polyphase Rectifier

The power circuit of the single phase upf rectifier is shown in Fig. 10. Notice that the neutral of the ac input is connected to the centre-tap of the output

dc.

$$v_p(t) \;=\; \frac{V_o}{2}\, d(t) \;-\; \frac{V_o}{2}\,[1-d(t)] \;=\; \frac{V_o}{2}\,[1-2d(t)] \tag{9.15}$$

$$v_i(t) \;=\; i(t)\; R_e \;\approx\; v_p(t) \;=\; \frac{V_o}{2}\,[1-2d(t)] \tag{9.16}$$

$$i(t) \;=\; \frac{V_o}{2\; R_e}\,[1-2d(t)] \tag{9.17}$$

d may be replaced by $\dfrac{t}{T_s}$, in order to obtain a suitable method of modulation.

$$i(t) \;=\; \frac{V_o}{2\; R_e}\,[1-2\frac{t}{T_s}] \tag{9.18}$$

Equation [18] may be graphically put in the form of a carrier based modulation scheme as shown in Fig. 11. Scalar control applied to single phase upf

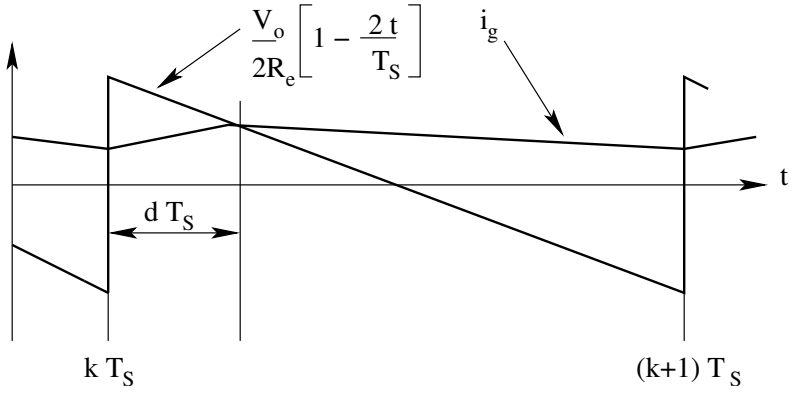

Figure 9.11: Scalar Control Carrier Scheme for Single Phase UPF Rectifier

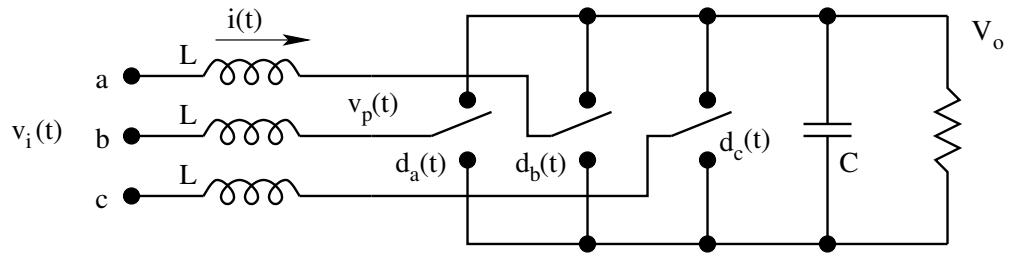

Figure 9.12: Power Circuit of a Three Phase Rectifier

rectification is given (Scalar Controlled Resistor Emulator) in this link. Figure 12 shows a scalar controlled three phase rectifier. Notice that the neutral connection is not needed since the three currents add up to zero.

9.4 Problem Set

1. Figure 1 shows a unity power factor rectifier. The source is 230V, 50 Hz ac. The output voltage is bipolar dc with $V_{dc} = 400$ V. The input inductor L has a value of 5 millihenry. The switching frequency is considerably high so that the source current is 10 A (rms) at 50 Hz, with negligible harmonic content. The control of the switch is done such that

$$d = \frac{1}{2} - \frac{kI_{ac}}{2V_{dc}} \quad (0 < d < 1)$$

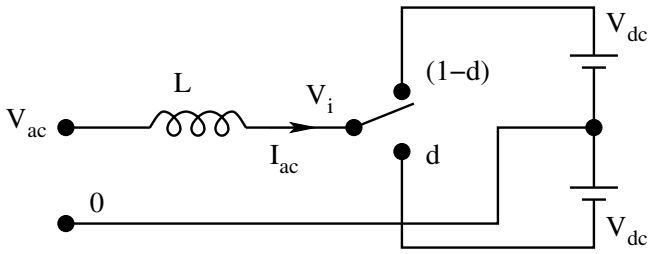

Fig. P 9.1: Unity Power Factor Rectifier

(A) Prove that $I_{ac} = V_i/k$, where V_i is the fundamental component of the voltage at the pole of the switch.

(B) Sketch the phasor diagram of V_{ac}, V_i, and I_{ac}.

(C) For the given operating condition evaluate k.

(D) Evaluate the minimum (d_{min}) and maximum (d_{max}) value of duty ratio in a cycle of the fundamental.

Appendix A

Review of Control Theory

A.1 Introduction

In Power Electronic Systems, besides power electronic devices, circuits and converters, the other major area of importance is the control. In the chapters covering the various converters, the operation and modeling of different converters were covered. For achieving the desirable working objectives, the converters are invariably controlled in closed loop. Classical and modern control theory is applied towards this objective. The dynamic transfer functions of the various power converters are the starting point in the design of closed loop controllers. In this Chapter, we will review the basics of control theory to the extent it is applicable for our objective of closed loop control of power converters.

A.1.1 System

The block f shown in Fig. A.1 qualifies as a system, if it responds (produces an output function y) in an understandable and predictable manner for all input functions u. System f links the input and output in an understandable and predictable manner. The system may be defined through a mathematical function operating on the input $u(t)$, to provide the output $y(t)$. Or the system may be defined through a reference table listing all possible inputs and the respective outputs.

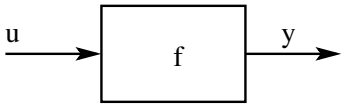

Figure A.1: A System

$$y = f(u) \tag{A.1}$$

A.1.2 Dynamic System

In a dynamic system, we require more information than just the input u and the system function f in order to determine the response y. In a dynamic system, for every input, there is a family of possible outputs. Therefore, for any input, in order to obtain the unique output (one unique member of the set of all possible outputs for the input), additional information is required. This extra information is defined as the "state of the system". The dynamic property defined as the "state" arises out of dynamic elements present in the system. Physically dynamic elements are those that are capable of storing information in certain ways. Examples of dynamic elements are,

1. Switches or flip-flops in digital electrical systems. Switches or flip-flops store digital information (ON/OFF, TRUE/FALSE, 1/0).
2. Capacitors or inductors in analog electrical systems. Capacitors store electrostatic energy. Inductors store electromagnetic energy.

The defining equations of dynamic systems are either differential or difference equations. Nondynamic systems are usually defined by algebraic equations. In dynamic systems, the functional relationship between input u and output y are linked through the state x of the system.

$$y = f(u, x) \tag{A.2}$$

A.1.3 Linear Dynamic System

A linear dynamic system is a dynamic system that satisfies the property of linearity - i.e superposition and homogeneity. These properties may be mathematically expressed as follows

- Homogeneity:

$$For\ f(u_1) = y_1 \quad \Rightarrow \quad f(au_1) = a\ y_1 \tag{A.3}$$

- Superposition:

$$For\ f(u_1) = y_1 \quad \& \quad f(u_2) = y_2 \quad \Rightarrow \quad f(u_1 + u_2) = y_1 + y_2 \tag{A.4}$$

The above properties may be combined into a single mathematical expression as follows.

$$f(au_1 + bu_2) = af(u_1) + bf(u_2) \tag{A.5}$$

A.1.4 A Simple Linear System

Consider the circuit shown in Fig. A.2

$$y = v_o = \frac{R_2}{R_1 + R_2} v_i = au \tag{A.6}$$

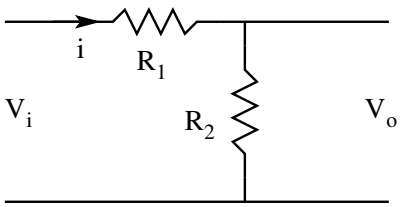

Figure A.2: A Simple Linear System

- The system is defined through an algebraic equation; it is a nondynamic system.
- The input/output relationship satisfies the property of linearity.
- For any system input v_i, the only property of the system that is required to be known is a, in order to determine the output uniquely.
- The system function in this case is an arithmetic multiplication by the attenuation constant a.

A.1.5 A Simple Linear Dynamic System

Consider the circuit shown in Fig.A.3

$$u \;=\; v_i \;;\; y \;=\; v_0 \tag{A.7}$$

Applying kirchoff's law, we get

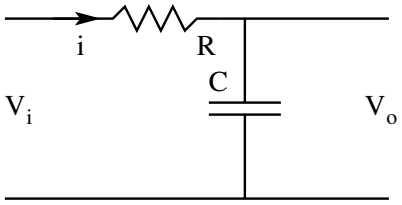

Figure A.3: A Simple Linear Dynamic System

$$v_i = v_o + iR \tag{A.8}$$

$$i = C\frac{dv_o}{dt} \tag{A.9}$$

$$v_i = v_o + RC\frac{dv_o}{dt} \tag{A.10}$$

- The system equation is a differential equation; it is a dynamic system.

- The system satisfies properties of linearity. (Notice Linear Differential Equation)
- The response for a step input of magnitude is obtained by solving the above first order linear differential equation.

$$v_o(t) = v_i\left(1 - e^{-\frac{t}{RC}}\right) + Ae^{-\frac{t}{RC}} \tag{A.11}$$

According to the above, the solution is not unique on account of the presence of the arbitrary constant A in the solution. To uniquely determine $v_o(t)$, the value of A must be determined. To determine A, v_o at t = 0 (initial condition) or at any finite time (boundary condition) is required to be known. For example, if $v_o(0) = V$, then

$$v_o(t) = v_i\left(1 - e^{-\frac{t}{RC}}\right) + Ve^{-\frac{t}{RC}} \tag{A.12}$$

- The voltage on the capacitor at t = 0 is the information that was used to uniquely determine the system response. Thus v_o qualifies as the state of the system.
- The state of the system in this example is the voltage on the capacitor. Notice that $v_o(t)$ determines the energy stored in the system at start. The dynamic nature of the system is related to the capacity of the element C to store energy (information).

In a similar way inductors store information through storage of magnetic energy. In general, the number of states in a system is equal to the number of independent energy storage elements in the system.

A.2 Laplace Transformation

Consider again the same circuit shown in Fig. A.3

$$v_i = v_o + RC\frac{dv_o}{dt} \tag{A.13}$$

- Solution of differential equations is more difficult than solution of algebraic equations.
- We therefore resort to transforming the linear differential equation into an algebraic system of equations.

Consider $v(t)$, and the pair of functions $v(t)$ & $V(s)$.

$$v(t) \quad \Rightarrow \quad V(s) \tag{A.14}$$

The definition of the Laplace transform of a function of time is as follows.

V(s) = Laplace transform of v(t)

$$V(s) = \int_0^\infty e^{-st}\ v(t)\ dt \tag{A.15}$$

The variable s in the Laplace transform is the transformed variable. Its physical significance is seen later. When we apply the Laplace transform to the system Eq.(A.13), the transformed equation is

$$\int_0^\infty\ v_i(t)e^{st}dt = \int_0^\infty\ v_o(t)e^{st}dt + RC\int_0^\infty\ e^{st}dv_o(t) \tag{A.16}$$

$$V_i(s) = V_o(s) + RCL\left(\frac{dv_o}{dt}\right) \tag{A.17}$$

$$V_i(s) = V_o(s) + RC\ sV_o(s) - RCv_o(0) \tag{A.18}$$

- The above equation describes the same system in the transformed variable s.
- In the new transformed system, the defining equation is algebraic.
- The system "state" automatically pops out in the process.

A.2.1 Transfer Function

For a moment, suppose that the initial condition is zero. The system starts from zero initial energy.

$$V_i(s) = V_o(s) + RC\ sV_o(s) = (1 + sCR)V_o(s) \tag{A.19}$$

$$V_o(s) = \frac{1}{1 + sCR}\ V_i(s) \tag{A.20}$$

$$G(s) = \frac{V_o(s)}{V_i(s)} = \frac{1}{1 + sCR} \tag{A.21}$$

Transfer function of a linear dynamic system is defined as the ratio of the Laplace transform of the output of the system to the Laplace transform of the corresponding input to the system under zero initial conditions.

- Transfer function is an input/output relationship. It does not tell us about all that is happening in the system. It relates the output to the input.
- Transfer function description is valid only for linear systems. Laplace transformation is a linear transformation, and the advantages of Laplace transform accrue only for linear systems.

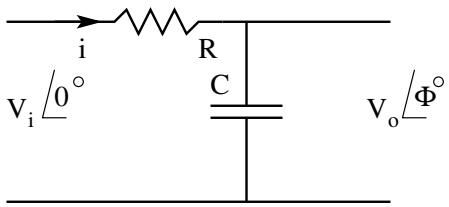

Figure A.4: A Dynamic Circuit Excited by a Sinusoidal Source

A.2.2 Physical Interpretation of the Transfer Function

Consider the same circuit excited by a sinusoidal source as shown in Fig. A.4. The input excitation is $V_i Sin(\omega t)$(angular frequency = ω rad/sec). In phasor notation $v_i = V_i \angle 0^\circ$. The system being linear, the output function will also be sinusoidal with the same angular frequency and a phase angle of

$$v_o = V_o \angle \phi^\circ \tag{A.22}$$

Under steady state, the impedance of R & C are R and $1/j\omega C$ respectively.

$$v_o = \frac{\frac{1}{j\omega C}}{1 + \frac{1}{j\omega C}} v_i \tag{A.23}$$

$$V_o \angle \Phi^\circ = \frac{1}{1 + j\omega CR} V_i \angle 0^\circ \tag{A.24}$$

When V_i, ω, C, R are all known, V_o and Φ may be computed.

$$\left|\frac{V_o}{V_i}\right| = \left|\frac{1}{1 + j\omega CR}\right| = |G(s)|_{s=j\omega} \tag{A.25}$$

$$\Phi = Phase\ of\ \frac{1}{1 + j\omega CR} = \angle G(s)_{s=j\omega} \tag{A.26}$$

Physically, the transfer function evaluated at any ($s = j\omega$) frequency gives the complex gain (magnitude gain & Phase Gain) of the system for that particular excitation frequency. For this reason, the transfer function is termed as the frequency domain description of the system.

A.2.3 Bode Plots

The transfer function evaluated at $s = j\omega$ gives the steady state complex gain of the system at that frequency. Bode Plot depicts this information for all frequencies, in a graphical plot. The steps in constructing the Bode plot are

1. The magnitude gain and phase gain are evaluated at different frequencies from the given transfer function.

2. The magnitude gain is converted into units of dB.
3. The phase gain is computed in degrees.
4. The Bode plot is plotted in two parts - the magnitude plot & the phase plot.

Magnitude Plot is plotted between $log_{10}(f)\ in\ Hz$ on the x-axis and the gain in dB ($20\ log_{10}(|G(j\omega)|)$ on the y-axis. Phase plot is plotted between $log_{10}(f)\ in\ Hz$ on the x-axis and the phase gain in degrees on the y-axis. In practice, the Bode plots are made using simple asymptotic approximations as illustrated in the following sections.

A.2.4 Some Terminologies on Transfer Function

Consider a dynamic system represented by

$$a_2\frac{d^2v_i}{dt^2} + a_1\frac{dv_i}{dt} + a_0v_i = b_3\frac{d^3v_0}{dt^3} + b_2\frac{d^2v_o}{dt^2} + b_1\frac{dv_o}{dt} + b_0v_o \tag{A.27}$$

Transforming to s domain, we get

$$V_i(s)(a_2s^2 + a_1s + a_o) = V_o(s)(b_3s^3 + b_2s^2 + b_1s + b_o) \tag{A.28}$$

$$G(s) = \frac{V_o(s)}{V_i(s)} = \frac{a_2s^2 + a_1s + a_o}{b_3s^3 + b_2s^2 + b_1s + b_o} \tag{A.29}$$

- G(s) is the transfer function of the system.
- System is linear. G(s) will be a ratio of polynomials in s.
- $$G(s) = \frac{N(s)}{D(s)} \tag{A.30}$$
- For physical systems, the order of the numerator will always be less than or equal to the order of the denominator. The reason is that all physical systems have inertia and cannot respond to excitation at infinitely high frequency.
- The coefficients appearing in the numerator and denominator are real for physical systems.
- The numerator and denominator may be factorised

$$G(s) = \frac{(1 + s/\omega_{z1})(1 + s/\omega_{z2})(1 + s/\omega_{z3})\dots}{(1 + s/\omega_{p1})(1 + s/\omega_{p2})(1 + s/\omega_{p3})\dots} \tag{A.31}$$

- The roots ω_{z1}, ω_{p1}, etc are real or complex. When complex, these roots occur in conjugate pairs, since the co-efficient of N(s) and D(s) are real.

- ω_{z1}, ω_{z2} etc (values of s for which G(s) = 0) are called the zeroes of the transfer function.
- ω_{p1}, ω_{p2} etc (values of s for which G(s) = ∞) are called the poles of the transfer function.
- Complex poles or zeroes, when occur, are in conjugate pairs. Then they may be combined into a single second order pair of poles and zeroes. Consider

$$\omega_{z1} = \sigma + j\omega \ \& \ \omega_{z2} = \sigma - j\omega \tag{A.32}$$

$$\left(1 + \frac{s}{\sigma + j\omega}\right)\left(1 + \frac{s}{\sigma - j\omega}\right) = 1 + \frac{s}{Q\omega_z} + \frac{s^2}{\omega_z^2} \tag{A.33}$$

$$\omega_z^2 = \sigma^2 + \omega^2 \ ; \ Q\omega_z = \frac{\sigma^2 + \omega^2}{2\sigma} \tag{A.34}$$

- The transfer function may be written as a ratio of polynomials in s. The numerator and the denominator are products of first order (real poles or zeroes) or second order (complex poles or zeroes) terms.

$$G(s) = K \, \frac{\left(1 + \frac{s}{\omega_{z1}}\right)\left(1 + \frac{s}{Q\omega_{zo}} + \frac{s^2}{\omega_{zo}^2}\right)\ldots}{\left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{Q\omega_{po}} + \frac{s^2}{\omega_{po}^2}\right)\ldots} \tag{A.35}$$

- Gain in dB is (20 $log_{10}|G(j\omega)|$. By defining gain in dB as a logarithmic function, the total gain is the sum of the gains due to zeroes and poles.
- Phase gain = Phase of $G(j\omega)$. The total phase gain is the sum of the phase gains due to poles and zeroes.
- The most important consequence of defining the gain in dB and phase in degrees is that the overall gain (dB) and the overall phase may be obtained by simply adding the gains of individual zeroes and poles. The types of poles and zeroes are also limited to first and second order. Further a pole may be considered as an inverted zero. Therefore, if we know the bode plots for first and second order terms, any higher order transfer function may be considered as a superposition of simple terms.

A.2.5 Asymptotic Bode Plots

We consider plotting approximate asymptotic Bode plots.

Simple Pole:

$$G(s) = \frac{1}{1 + \frac{s}{\omega_p}} \tag{A.36}$$

Magnitude Gain:

$$G(j\omega) = 20\ log_{10}\left|\frac{1}{1+j\frac{\omega}{\omega_p}}\right| \tag{A.37}$$

$$= 20\ log_{10}\sqrt{\frac{1}{1+\frac{\omega^2}{\omega_p^2}}} \tag{A.38}$$

The function given in Eq.(38) is as such inconvenient. We break it into two regions and apply appropriate approximations.

$$1+\frac{\omega^2}{\omega_p^2}\ \approx\ 1\ for\ \frac{\omega^2}{\omega_p^2}\ <<\ 1 \Rightarrow\ \frac{\omega}{\omega_p}\ \leq\ 1 \tag{A.39}$$

$$1+\frac{\omega^2}{\omega_p^2}\ \approx\ \frac{\omega^2}{\omega_p^2}\ for\ \frac{\omega^2}{\omega_p^2}\ >>\ 1 \Rightarrow\ \frac{\omega}{\omega_p}\ \geq\ 1 \tag{A.40}$$

The aymptotic plots are given by the following expressions.

Table A.1: Frequency Vs Gain

Angular Frequency ω/ω_p	Actual Gain dB	Approximate Gain dB	Error dB
0.1	-0.04	0	0.04
0.2	-0.17	0	0.17
0.5	-1.0	0	1.0
1	-3.0	0	3.0
2	-7.0	-6.0	1.0
5	-14.15	-14	0.17
10	-20.04	-20.0	0.04

$$G(j\omega) = \begin{cases} 20\ log_{10}(1)\ =\ 0\ for\ \ \frac{\omega}{\omega_p}\ \leq\ 1 \\ 20\ log_{10}(\frac{\omega}{\omega_p})\ \ for\ \ \frac{\omega}{\omega_p} \geq\ 1 \end{cases} \tag{A.41}$$

$$G(j\omega) = \begin{cases} =\ 0\ dB\ for\ \ \frac{\omega}{\omega_p}\ \leq\ 1 \\ =\ 20\ (dB/decade)\ Slope\ for\ \ \frac{\omega}{\omega_p} \geq\ 1 \end{cases} \tag{A.42}$$

The error caused by this approximation in gain is as given in Table.1

- The maximum error introduced by the approximation is 3dB.
- The gain is 0 dB for $\omega \leq \omega_p$.
- The gain monotonically falls at the rate of 20 dB/decade of frequency change in the region $\omega \geq \omega_p$.

Phase Gain

$$\phi(j\omega) = tan^{-1}\left(\frac{\omega}{\omega_p}\right) \tag{A.43}$$

Just as we did for magnitude gain, the range of frequency is split into different regions.

$$\phi(j\omega) = \begin{cases} tan^{-1}0 \quad = 0 \ for \quad \frac{\omega}{\omega_p} << 1 \Rightarrow \quad \frac{\omega}{\omega_p} < 0.1 \\ tan^{-1}\infty \quad = -90^\circ \ for \quad \frac{\omega}{\omega_p} >> 1 \Rightarrow \quad \frac{\omega}{\omega_p} > 10 \end{cases} \tag{A.44}$$

$$\phi(j\omega) = \begin{cases} 0^\circ \ for \quad \omega \leq 0.1\omega_p \\ 45^\circ/decade \quad 0.1\omega_p \leq \omega \leq 10\omega_p \\ -90^\circ \ for \quad \omega \geq 10\omega_p \end{cases} \tag{A.45}$$

In the intermediate region ($0.1\omega_p \leq \omega \leq 10\omega_p$), the phase is taken as a linear

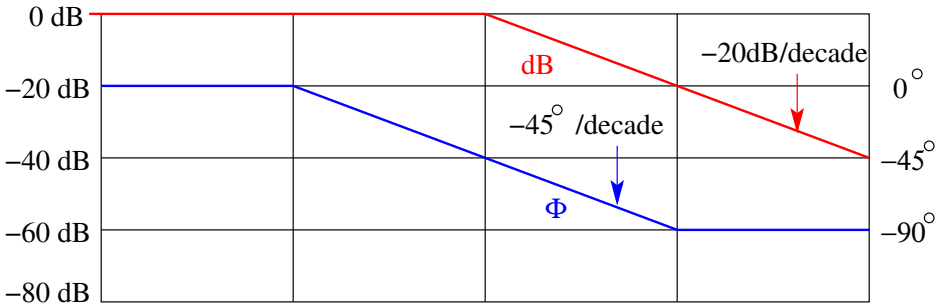

Figure A.5: Asymptotic Bode Plot of a Simple Pole

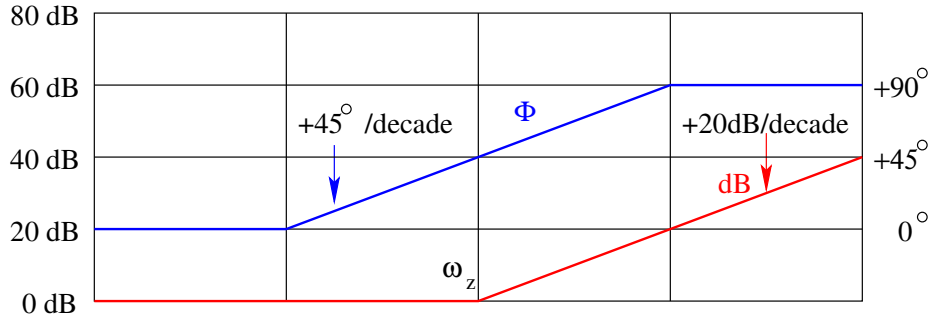

Figure A.6: Asymptotic Bode Plot of a Simple Zero

relationship with . The error in the approximation is bounded within as given in Table 2. The asymptotic Bode plots for a simple pole and zero are shown in Figs 5 and 6. The asymptotic Bode plot for a simple zero is the inverted version of that of a simple pole.

Table A.2: Frequency Vs Phase

Angular Frequency ω/ω_p	Actual Phase degree	Approximate Phase degree	Error degree
0.05	-3	0	3
0.1	-6	0	6
0.5	-27	-31	4
1	-45	-45	0
2	-63	-59	-4
10	-84	-90	-6
20	-87	-90	-3

Second Order Pole

Consider the second order pole given by the following function

$$G(s) = 1 + \frac{s}{Q\omega_o} + \frac{s^2}{\omega_o^2} \tag{A.46}$$

Magnitude Gain

Again we consider in three regions

$$G(j\omega) = \begin{cases} 0\ dB\ for \quad \dfrac{\omega}{\omega_p} << 1 \\ 20\ log_{10}Q\ dB\ for \quad \dfrac{\omega}{\omega_p} = 1 \\ -40\ log_{10}\dfrac{\omega}{\omega_p}\ dB\ for \quad \dfrac{\omega}{\omega_p} >> 1 \end{cases} \tag{A.47}$$

- For $\omega << \omega_o$, the gain is 0 dB.
- For $\omega = \omega_o$, the gain is 20 $log_{10}Q$.
- For $\omega >> \omega_o$, the gain monotonically falls at the rate of -40dB/decade of frequency increments.

Phase Gain

$$\phi(j\omega) = \begin{cases} 0^\circ\ for \quad \omega \leq \omega_1 \\ -90^\circ \quad \omega = \omega_o \\ -180^\circ\ for \quad \omega \geq \omega_2 \end{cases} \tag{A.48}$$

The phase angle is approximated as a straight line between ω_1 and ω_2 varying from 0° at ω_1 and -180° at ω_2, where

$$\omega_1 = \frac{\omega_o}{5^{(1/2Q)}}\ ; \qquad \omega_2 = \omega_o\ 5^{(1/2Q)} \tag{A.49}$$

The asymptotic bode plots for a quadratic pole-pair are shown in Fig. 7.

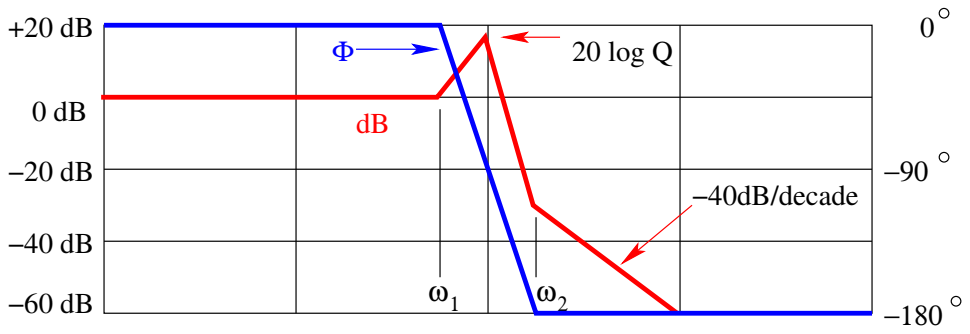

Figure A.7: Asymptotic Bode Plot of a Quadratic Pole-Pair

A.3 Principles of Closed Loop Control of Linear Systems

In the open loop system shown in Fig. 8, the output y is a function of the input u and the system parameters. In frequency domain description, G(s) is the system to be controlled. G(s) is a function of the parameters of the system. The parameters of the system are usually not completely known, and even when completely known are dependent on operating point and can vary over a wide range. Ideally when we wish to control the system, we desire

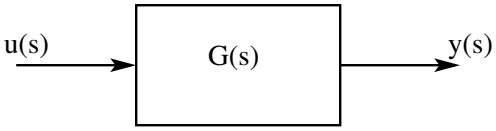

Figure A.8: A Simple Open-Loop System

that the output is fully under our control and independent of the parameters of the system or the operating point - or independent of the uncertainties of the system parameters. Such an ideal situation is not obtainable in the open loop control shown above. Closed loop control achieves this objective to a considerable extent. The objective of closed loop control is to make the overall system behaviour less sensitive to the system parameters. Consider the closed loop system shown in Fig. 9. Suppose that G(s) even though not completely known, is very large.

$$G(s) = \infty \quad \Rightarrow \epsilon = \frac{Y}{G} \approx 0 \tag{A.50}$$

$$\epsilon = U - HY \approx 0 \quad \Rightarrow Y = \frac{1}{H}U \tag{A.51}$$

The output Y is the ideal gain (1/H) times the input U. H(s) is the feedback controller under the control of the designer. Therefore the gain of the ideal

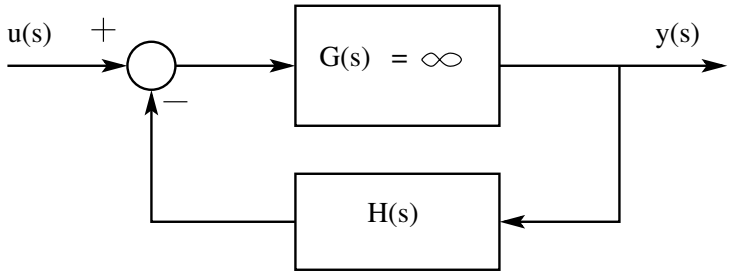

Figure A.9: Ideal Closed Loop System

closed loop system is totally independent of the system parameters.

A.3.1 Effect of the Non ideal G(s)

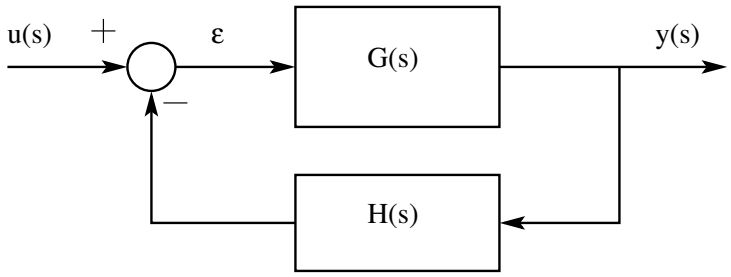

Figure A.10: A Real Closed Loop System

In practice G(s) is not ∞. Considering this nonideality as shown in Fig. 10, we see that

$$Y = G\,\epsilon = G(U - HY) \quad \Rightarrow \quad Y = \frac{G}{1+GH}U \tag{A.52}$$

$$Y = \frac{1}{H}\frac{GH}{1+GH} \tag{A.53}$$

The nonideality in G(s) introduces a correction factor in the actual closed loop performance compared to the ideal performance. As the correction factor approaches unity, we approach the ideal situation. Define T = GH (called the loop gain). The correction factor C is

$$C = \frac{T}{1+T} \tag{A.54}$$

The correction factor C is a function of T and only T. With this, Eq. [53], may be rewritten as

$$Y = \frac{1}{H}C \tag{A.55}$$

- The correction factor is 1 when T is large ($T >> 1$).
- The correction factor is T when T is small ($T << 1$).
- The factor (1+T) appearing in the denominator of C is responsible for stability.
- When $|T| < 1$, the denominator is always non-zero. The system is always stable. This property is referred to as " Small gain Theorem"
- When $|T| = 1$, the denominator may approach zero and lead to instability.
- For guaranteed stability of linear systems, the phase angle of the loop gain T must be greater than $-180°$, for $|T|$ above 1. The gain magnitude of loop gain $|T|$ must be less than 1, for phase angle Φ less than $-180°$.
- Phase Margin: The amount by which Φ is above $-180°$, when $|T|$ is equal to 1.
- Gain Margin: The amount by which $|T|$ is below unity, when Φ is $-180°$.
- The ideas reviewed in this section are used in the section on closed loop controllers to develop simple rules for the design of closed loop controllers.

Appendix B

Extra Element Theorem

B.1 Concept of Double Injection and Extra Element Theorem

Consider the two input two output system shown in Fig. 1. The input to output relations are given by Eqn. (1) and Eqn. (2).

Figure B.1: A Two Input Two Output System

$$u_{o1} = A_1\ u_{i1}\ +\ A_2\ u_{i2} \tag{B.1}$$

$$u_{o2} = B_1\ u_{i1}\ +\ B_2\ u_{i2} \tag{B.2}$$

$$A_1 = \left[\frac{u_{o1}}{u_{i1}}\right]_{u_{i2}=0} \qquad A_2 = \left[\frac{u_{o1}}{u_{i2}}\right]_{u_{i1}=0} \tag{B.3}$$

$$B_1 = \left[\frac{u_{o2}}{u_{i1}}\right]_{u_{i2}=0} \qquad B_2 = \left[\frac{u_{o2}}{u_{i2}}\right]_{u_{i1}=0} \tag{B.4}$$

Consider the case now when both the inputs u_{i1} and u_{i2} are present but u_{o1} is zero. This is called null-output condition. Physically this can be visualised as both inputs u_{i1} and u_{i2} being simultaneously adjusted to make output u_{o1} to become zero.

$$0 = u_{o1} = A_1\ u_{i1}\ +\ A_2\ u_{i2} \Rightarrow\ u_{i1} = \frac{A_2}{A_1} u_{i2} \tag{B.5}$$

$$u_{o2} = B_1\ u_{i1}\ +\ B_2\ u_{i2} \Rightarrow\ u_{o2} = \frac{A_1 B_2 - A_2 B_1}{A_1} u_{i2} \tag{B.6}$$

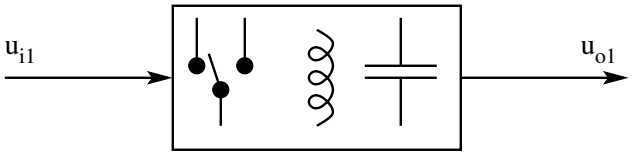

Figure B.2: A Switched Mode Power Converter

We now define two driving point functions Z_d and Z_n. Z_d is the driving point function of port 2 for zero input at port 1. Z_n is the driving point function of port 2 for null output at port 1. These are given by the following expressions.

$$Z_d = \left[\frac{u_{o2}}{u_{i2}}\right]_{u_{i1}=0} = B_2 \tag{B.7}$$

$$Z_n = \left[\frac{u_{o2}}{u_{i2}}\right]_{u_{o1}=0} = \frac{A_1B_2 - A_2B_1}{A_1} \tag{B.8}$$

Consider now a single input single output system (the power converter) as

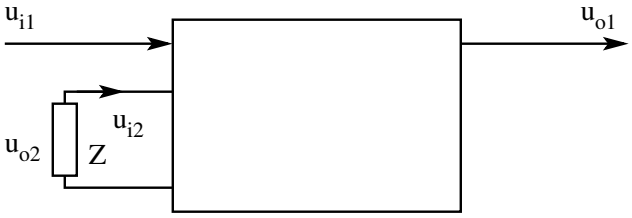

Figure B.3: Re-definition of the System

shown in Fig. 2. Define one of the elements in the network as an extra element Z as shown in Fig. 3. The current through the element Z is defined as the input u_{i2} and the voltage across Z is defined as the output u_{o2}. The system defining equations are

$$u_{o1} = A_1\ u_{i1}\ +\ A_2\ u_{i2} \tag{B.9}$$

$$u_{o2} = B_1\ u_{i1}\ +\ B_2\ u_{i2} \tag{B.10}$$

$$u_{i2} = -\frac{u_{o2}}{Z} \tag{B.11}$$

$$u_{o2} = B_1\ u_{i1}\ -\ B_2\ \frac{u_{o2}}{Z}\ \Rightarrow\ u_{o2}\left[1\ +\ \frac{B_2}{Z}\right] = B_1\ u_{i1} \tag{B.12}$$

$$u_{o2} = u_{i1}\frac{B_1}{\left[1\ +\ \dfrac{B_2}{Z}\right]} \tag{B.13}$$

$$u_{o1} = A_1\ u_{i1}\ -\ A_2\ \frac{u_{o2}}{Z}\ =\ A_1\ u_{i1}\ -\frac{A_2B_1}{B_2+Z}\ u_{i1} \tag{B.14}$$

$$u_{o1} \;=\; u_{i1}\frac{A_1\left[1+\dfrac{A_1B_2-A_2B_1}{A_1Z}\right]}{1+\dfrac{B_2}{Z}} \;=\; u_{i1}\;A_1\frac{\left[1+\dfrac{Z_n}{Z}\right]}{\left[1+\dfrac{Z_d}{Z}\right]} \tag{B.15}$$

$$\left[\frac{u_{o1}}{u_{i1}}\right]_Z \;=\; A_1\frac{\left[1+\dfrac{Z_n}{Z}\right]}{\left[1+\dfrac{Z_d}{Z}\right]} \;=\; \left[\frac{u_{o1}}{u_{i1}}\right]_{Z=\infty}\frac{\left[1+\dfrac{Z_n}{Z}\right]}{\left[1+\dfrac{Z_d}{Z}\right]} \tag{B.16}$$

$$\left[A\right]_{Z=Z} \;=\; \left[A\right]_{Z=\infty}\;\frac{\left[1+\dfrac{Z_n}{Z}\right]}{\left[1+\dfrac{Z_d}{Z}\right]} \tag{B.17}$$

Equation 17 is the statement of the extra element theorem. Any network function A in the presence of the element Z is expressed in terms of the network fuction A in the absence of the function ($Z = \infty$) and a correction factor consisting of a bilinear function of Z. The correction factor is a function of the extra element introduced Z and two driving point functions Z_d and Z_n at the point of introduction of the extra element. These two driving point impedances are as defined in Eq. [7] and [8].

There is an alternate formulation of the same problem. Define the voltage of the element Z as u_{i2} and the current through the element as u_{o2} as shown in Fig. 4. This is a dual formulation of the extra element theorem.

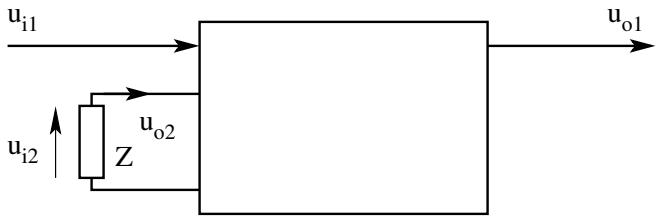

Figure B.4: Alternate Formulation of the System

$$u_{o1} = A_1\;u_{i1} \;+\; A_2\;u_{i2} \tag{B.18}$$

$$u_{o2} = B_1\;u_{i1} \;+\; B_2\;u_{i2} \tag{B.19}$$

$$u_{o2} = -\frac{u_{i2}}{Z} \tag{B.20}$$

$$u_{o1} = A_1\;u_{i1} \;-\; A_2\;Z\;u_{o2} \tag{B.21}$$

$$u_{o2} = B_1\;u_{i1} \;-\; B_2\;Zu_{o2} \;\Rightarrow\; u_{o2} \;=\; u_{i1}\;\frac{B_1}{\left[1+B_2Z\right]} \tag{B.22}$$

$$u_{o1} = A_1\ u_{i1}\ -\ A_2\ u_{o2}Z\ =\ A_1\ u_{i1}\ -\frac{A_2 Z B_1}{1+B_2 Z}\ u_{i1} \tag{B.23}$$

$$u_{o1}\ =\ u_{i1}\frac{A_1\left[1+\dfrac{[A_1B_2-A_2B_1]Z}{A_1}\right]}{1+B_2Z} \tag{B.24}$$

$$\left[\frac{u_{o1}}{u_{i1}}\right]_{(Z=Z)}\ =\ \left[\frac{u_{o1}}{u_{i1}}\right]_{(u_{i2=0})}\frac{\left[1+\dfrac{Z}{Z_n}\right]}{\left[1+\dfrac{Z}{Z_d}\right]} \tag{B.25}$$

$$\left[A\right]_{(Z=Z)}\ =\ \left[A\right]_{(Z=0)}\frac{\left[1+\dfrac{Z}{Z_n}\right]}{\left[1+\dfrac{Z}{Z_d}\right]}\ =\ \left[A\right]_{(Z=\infty)}\frac{\left[1+\dfrac{Z_n}{Z}\right]}{\left[1+\dfrac{Z_d}{Z}\right]} \tag{B.26}$$

From the above dual relationship, it is also seen that,

$$\left[A\right]_{(Z=0)} = \left[A\right]_{(Z=\infty)}\frac{Z_n}{Z_d} \tag{B.27}$$

B.2 Some Application Examples

B.2.1 Transfer Function

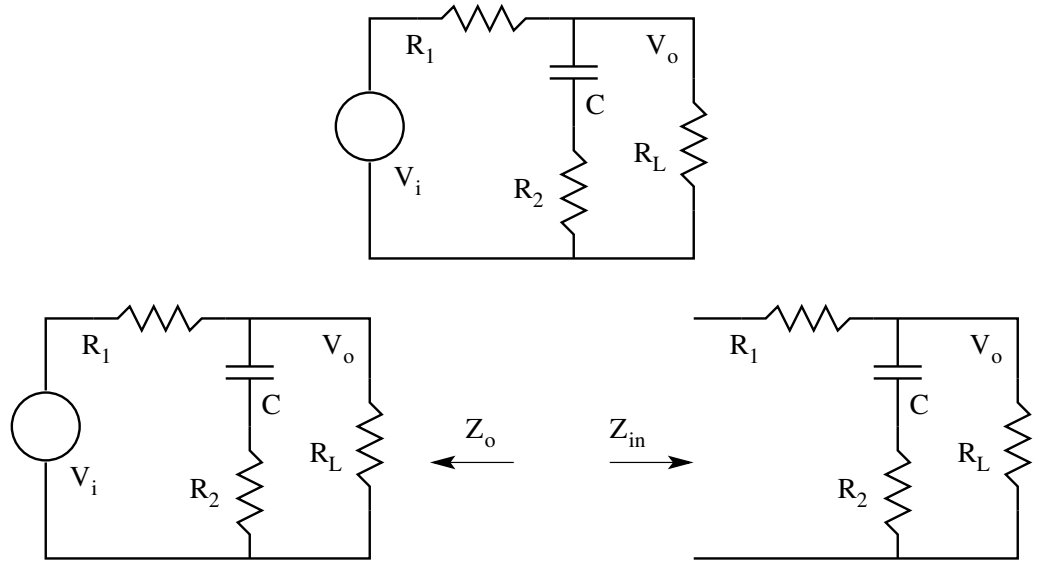

Figure B.5: A Simple Circuit Example

Consider the circuit shown in Fig. 5. By conventional method one can find the transfer function to be

$$A = \frac{V_o}{V_{in}} = \frac{R_L}{R_1 + R_L} \frac{1 + sCR_2}{1 + sC\left(R_2 + \left(R_1||R_L\right)\right)} \tag{B.28}$$

We may apply the extra element theorem for $Z = 1/sC$.

$$\left[A\right]_{Z=Z} = \left[A\right]_{Z=\infty} \frac{1 + sCZ_n}{1 + sCZ_d} \tag{B.29}$$

$$\left[A\right]_{Z=\infty} = \frac{R_L}{R_1 + R_L} \tag{B.30}$$

$$Z_d = \left[\frac{u_{o2}}{u_{i2}}\right]_{u_{i1} = V_{in} = 0} = \frac{R_L}{R_1 + R_L} \tag{B.31}$$

$$Z_n = \left[\frac{u_{o2}}{u_{i2}}\right]_{u_{o1} = V_o = Null} = R_2 \tag{B.32}$$

$$A = \frac{R_L}{R_1 + R_L} \frac{1 + sCR_2}{1 + sC\left(R_2 + \left(R_1||R_L\right)\right)} \tag{B.33}$$

B.2.2 Output Impedance

$Z = \frac{1}{sC}$ $u_{o1} = V_o$ $u_{i1} = i_o$

$$\left[Z_o\right]_{Z=\infty} = R_L||R_1 \tag{B.34}$$

Z_d = Driving Point Impedance with $(i_o = 0) = R_L + R_1$

Z_n = Driving Point Impedance with $(V_o = Null) = R_2$

$$Z_o = R_L||R_1 \frac{1 + sCR_2}{1 + sC\left(R_2 + \left(R_1||R_L\right)\right)} \tag{B.35}$$

B.2.3 Input Impedance

$Z = \frac{1}{sC}$ $u_{o1} = V_i$ $u_{i1} = i_1$

$$\left[Z_{in}\right]_{Z=\infty} = R_1 + R_L \tag{B.36}$$

$$Z_d \ = DrivingPointImpedancewith(i_o = 0) = R_2 + R_L$$

$$Z_n \ = DrivingPointImpedancewith(V_o = Null) = R_2 + (R_1||R_L)$$

$$Z_{in} \ = \ (R_1 + R_L)\ \frac{1 + sC\Big(R2 + (R_1||R_L)\Big)}{1 + sC(R_2 + R_L)} \tag{B.37}$$

B.2.4 Transistor Amplifier

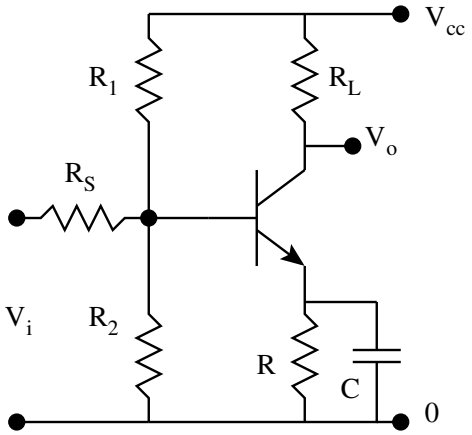

Figure B.6: A Transistor Amplifier

The equivalent circuit of the amplifier is shown in Fig. 7. Notice that the equivalent circuit is in the absence of C in the circuit. Extra element theorem is applied to correct for the presence of C. Figures 8 and 9 show the evaluation of the driving point impedances Z_d and Z_n.

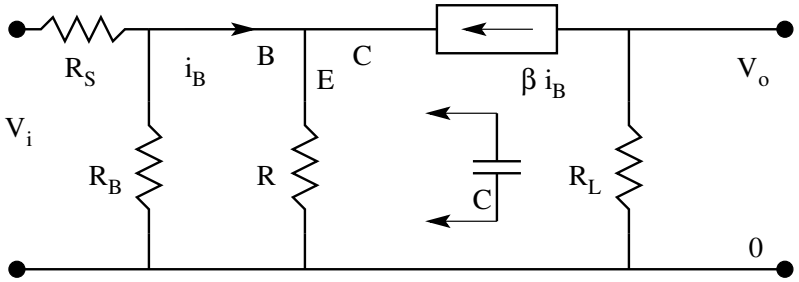

Figure B.7: Equivalent Circuit in the Absence of C

$$R_B \ = \ R_1||R_2 \tag{B.38}$$

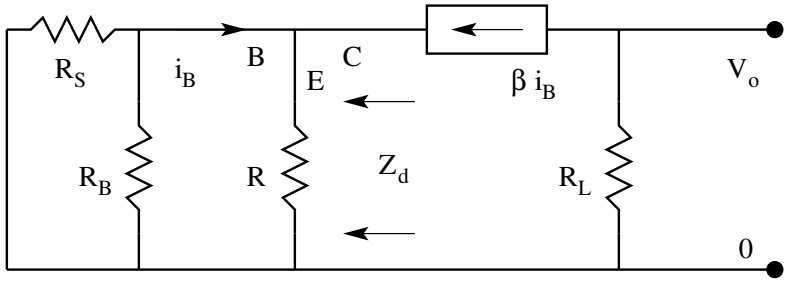

Figure B.8: Evaluation of Z_d

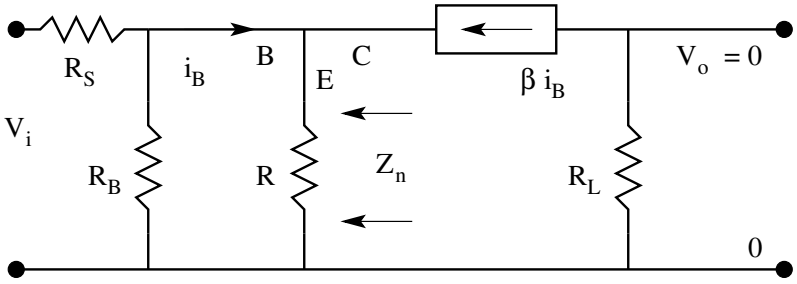

Figure B.9: Evaluation of Z_n

$$\left[A\right]_{Z=\infty} = \frac{R_B}{R_S + R_B} \frac{-\beta R_L}{R(\beta+1) + (R_S||R_B)} \tag{B.39}$$

$$\left[A\right]_{Z=Z} = \left[A\right]_{Z=\infty} = \frac{1 + sCZ_n}{1 + sCZd} \tag{B.40}$$

Z_d = Driving Point Impedance with $(V_i = 0) = R||\frac{R_S||R_B}{1+\beta}$

Z_n = Driving Point Impedance with $(V_o = Null)$

$V_o = 0 \Rightarrow i_c = 0 \Rightarrow i_B = 0 \Rightarrow Z_n = 0$

$$\left[A\right]_{Z=Z} = \frac{R_B}{R_S + R_B} \frac{-\beta R_L}{R(\beta+1) + (R_S||R_B)} \frac{1}{\left(R||\frac{R_S||R_B}{1+\beta}\right)} \tag{B.41}$$

Problem Set

1. For the transistor amplifier circuit shown in Fig. 10,
   - Effect of input coupling capacitance C_S.
   - Effect of transition layer capacitance C_T

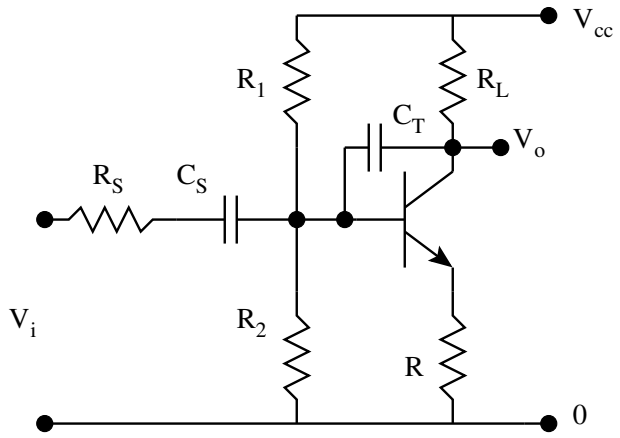

Figure B.10: Transistor Amplifier

Appendix C

Per Unit Description of Switched Mode Power Converters

C.1 Normalised Models of Switched Mode Power Converters

Consider the following two non-isolated converters.
Converter 1:

$$V_G = 40\ V\ ; \quad P_G = 100\ W\ ; \quad T_S = 50\ \mu S\ ;$$
$$R = 32\ \Omega\ ; \quad L = 8\ mH\ ; \quad C = 31.25\ \mu F\ ;$$

Converter 2:

$$V_G = 100\ V\ ; \quad P_G = 100\ W\ ; \quad T_S = 20\ \mu S\ ;$$
$$R = 200\ \Omega\ ; \quad L = 20\ mH\ ; \quad C = 2.0\ \mu F\ ;$$

C.1.1 Normalisation

Although the element values of these two converters vary widely, both these converters, when scaled properly, have identical mathematical descriptions. While comparing different converters for their performance indices, it is necessary to scale the defining equations suitably so that comparisons may be made readily. It is usual therefore, to scale the model such that the switching time period of the simulated model is always 1 unit. One such scaled description of the converters is the "per unit" description of the converter. Such descriptions are standard in power systems and electrical machines analysis.

C.1.2 Dynamic Equations

Consider the ideal converters and their defining equations. Table 1 gives the defining equations of the basic converters. Let the normalising quantities be defined as follows:

Table C.1: Defining Equations of the Converters

Buck Converter	$L\frac{di}{dt} = v_G u - v_O$	$C\frac{dv_O}{dt} = i - \frac{v_O}{R}$
Boost Converter	$L\frac{di}{dt} = v_G - v_O\overline{u}$	$C\frac{dv_O}{dt} = i\overline{u} - \frac{v_O}{R}$
Buck-Boost Converter	$L\frac{di}{dt} = v_G u - v_O\overline{u}$	$C\frac{dv_O}{dt} = -i\overline{u} - \frac{v_O}{R}$

Base Voltage: V_G ; Base Power: P_G ;
Base Time: $T_S = 1/f_S$; Base Current: $I_G = P_G/V_G$;

Then the normalised (per unit) converter variables are,

$$i^* = \frac{i}{I_G} \; ; \; v_O^* = \frac{v_O}{I_G} \; ; \; v_G^* = \frac{v_G}{V_G} \; ; \; t^* = \frac{t}{T_S} \; ;$$

The pu (per unit) description of the buck converter may then be derived as

$$L\frac{di}{dt} = v_G u - v_O \; ; \; C\frac{dv_O}{dt} = i - \frac{v_O}{R} \; ;$$

The transformed equations are

$$\left[\frac{LI_G}{V_G T_S}\right]\frac{di^*}{dt^*} = v_G^* u - v_O^* \; ; \; \left[\frac{CV_G}{I_G T_S}\right]\frac{dv_O^*}{dt^*} = i^* u - \frac{v_O^*}{R^*} \; ;$$

The pu parameters may be defined for the equation given above.

$$L^* = \frac{LI_G}{V_G T_S} \; ; \; C^* = \frac{CV_G}{I_G T_S} \; ; \; R^* = \frac{RI_G}{V_G} \; ;$$

The simplified per unit description is

$$L^*\frac{di^*}{dt^*} = v_G^* u - v_O^* \; ; \; C^*\frac{dv_O^*}{dt^*} = i^* - \frac{v_O^*}{R^*} \; ;$$

C.1.3 Dynamic Equations in pu

The equations are identical to the original set except that they are now in per unit parameters. Usually the stars for the parameters may be conveniently

omitted.

Advantages of pu system:

- Simulation frequency is 1 unit.
- Normalised element values are more convenient to handle.
- Simulation step size can be fixed (at say 0.01 unit) and the total simulation time can also be fixed (at say 100 units).

Disadvantages of pu system:

- The results are scaled and therefore have to be interpreted carefully. One unit of voltage in simulation will correspond to Vg volts, one unit of time in simulation will correspond to Ts seconds, and so on.

Table C.2: Per Unit Equations of the Converters

Buck Converter	$L^* \frac{di^*}{dt^*} = v_G^* u - v_O^*$	$C^* \frac{dv_O^*}{dt^*} = i^* - \frac{v_O^*}{R^*}$
Boost Converter	$L^* \frac{di^*}{dt^*} = v_G^* - v_O^* \overline{u}$	$C^* \frac{dv_O^*}{dt^*} = i^* \overline{u} - \frac{v_O^*}{R^*}$
Buck-Boost Converter	$L^* \frac{di^*}{dt^*} = v_G^* u - v_O^* \overline{u}$	$C^* \frac{dv_O^*}{dt^*} = -i^* \overline{u} - \frac{v_O^*}{R^*}$

Table 2 gives the per unit description of the the three basic dc to dc converters. With practice normally the stars are dropped and the normal description directly holds for the pu description, except that the parameters are in pu quantities.

We may carry the pu description further and draw some more important conclusions. In power converters, the selection of L and C follow from the specifications of current ripple allowed in the inductor and the voltage ripple allowed in the output voltage.

Let δI and δV_o be the specified limits on the current and voltage ripple respectively. The steady state current & voltage ripple for the different converters are given in Table 3. The same quantities in pu parameters are given in Table 4.

Table C.3: Ripple Current and Voltage in the Basic Converter

	$\delta I/I = \delta_i$	$\delta V_o/V_o = \delta_v$
Buck Converter	$(1-d)T_S R/L$	$(1-D)T_S^2/8LC$
Boost Converter	$d(1-d)^2 RT_S/L$	dT_S/RC
Buck-Boost Converter	$(1-d)^2 RT_S/L$	dT_S/RC

Table C.4: Ripple Current and Voltage in pu Parameters

	$\delta I/I = \delta_i$	$\delta V_o/V_o = \delta_v$
Buck Converter	$(1-d)R^*/L^*$	$(1-d)/8L^*C^*$
Boost Converter	$d(1-d)^2 R^*/L^*$	d/R^*C^*
Buck-Boost Converter	$(1-d)^2 R^*/L^*$	d/R^*C^*

The pu power P^* is related to the pu resistance $R^* = (v_O^*)^2 / P^*$. The relationship between the ripple factors and the per unit power is given in Table 5. The design criteria for selecting L and C may be obtained as follows. Table 6 gives the desired pu inductance and capacitance as a function of operating paramenters.

Table C.5: Ripple Current and Voltage as a Function of Power

	$\delta I/I = \delta_i$	$\delta V_o/V_o = \delta_v$
Buck Converter	$(1-d)(v_O^*)^2 / P^* L^*$	$(1-d)/8L^*C^*$
Boost Converter	$d(1-d)^2(v_O^*)^2 / P^* L^*$	$dP^*/(v_O^*)^2 C^*$
Buck-Boost Converter	$(1-d)^2(v_O^*)^2 / P^* L^*$	$dP^*/(v_O^*)^2 C^*$

Table C.6: PU Inductance and Capacitance as a Function of Ripple

	L^*	C^*
Buck Converter	$(1-d)(v_O^*)^2 / P^* \delta_i$	$(1-d)/8L^*\delta_v$
Boost Converter	$d(1-d)^2(v_O^*)^2 / P^* \delta_i$	$dP^*/(v_O^*)^2 \delta_v$
Buck-Boost Converter	$(1-d)^2(v_O^*)^2 / P^* \delta_i$	$dP^*/(v_O^*)^2 \delta_v$

We may also find the total energy handling capacity of the reactive elements in the converter.

$$E^* = E_L^* + E_C^* = \frac{L^* \left(i^*\right)^2}{2} + \frac{C^* \left(v_O^*\right)^2}{2}$$

The total energy storage requirement of the different converters are given in Table 7.

Table C.7: Energy Storage Requirements of the Different Converters

Energy pu	Buck	Boost	Buck-Boost
E^*	$\frac{(1-d)P^*}{2\delta_i} + \frac{\delta_i P^*}{16\delta_v}$	$\frac{dP^*}{2\delta_i} + \frac{dP^*}{2\delta_v}$	$\frac{P^*}{2\delta_i} + \frac{dP^*}{2\delta_v}$
Consider a representative example $P^* = 1$; $\delta_i = 0.2$; $\delta_v = 0.02$			
E^*	2.5(1-d) + 0.625	2.5d + 25d	2.5 + 25d

The energy storage requirements for the different converters may be plotted as a function of the duty ratio d as shown in Fig. 1. From the stored energy

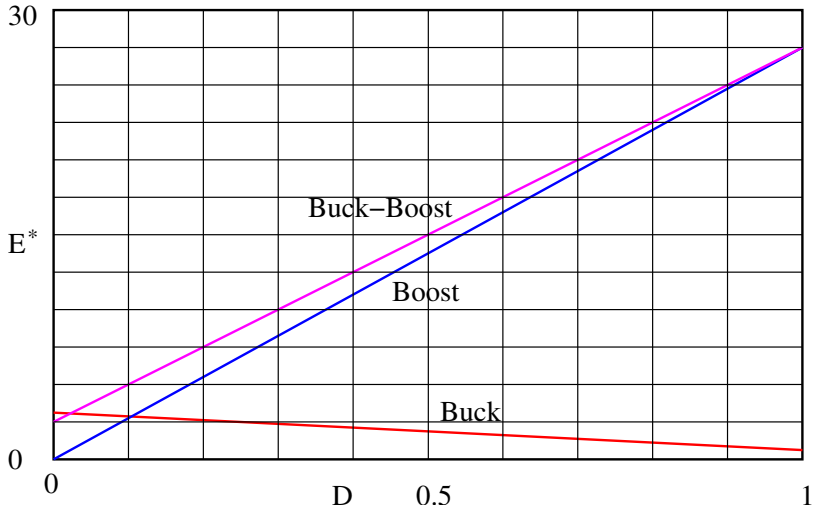

Figure C.1: Stored Energy Requirement for Different Converters

needs of different converters, we may conclude the following.

1. For the same power level and performance (steady-state ripple), buck converter needs nearly one order of magnitude less energy storage compared to the other two converters.
2. In buck converter the predominant energy storage element is the inductor. In the other two converters the predominant storage element is the capacitor.
3. The preferred operating duty ratio of buck converter is above 0.5. The preferred operating duty ratio of the other two converters is below 0.5.
4. The higher the energy stored in the converter, the slower is its response. This may be seen from Table 8 giving the natural frequency of the different converters.

Table C.8: Natural Frequency of Different Converters

	Natural Frequency	
Buck Converter	$\frac{1}{\sqrt{L^*C^*}}$	$\sqrt{\frac{8\delta_v}{1-d}}$
Boost Converter	$\frac{1-d}{\sqrt{L^*C^*}}$	$\sqrt{\frac{\delta_i\delta_v}{d^2}}$
Buck-Boost Converter	$\frac{1-d}{\sqrt{L^*C^*}}$	$\sqrt{\frac{\delta_i\delta_v}{d}}$

For representative ripple values, the natural frequency is plotted in Fig. 2 as a function of duty ratio. From the figure the following conclusions can be made.

1. For the same power level and performance, buck converter has a corner frequency of about an order of magnitude higher than the other two converters.
2. It is preferable to operate the buck converter with $d > 0.5$ and the other two converters with $d < 0.5$.

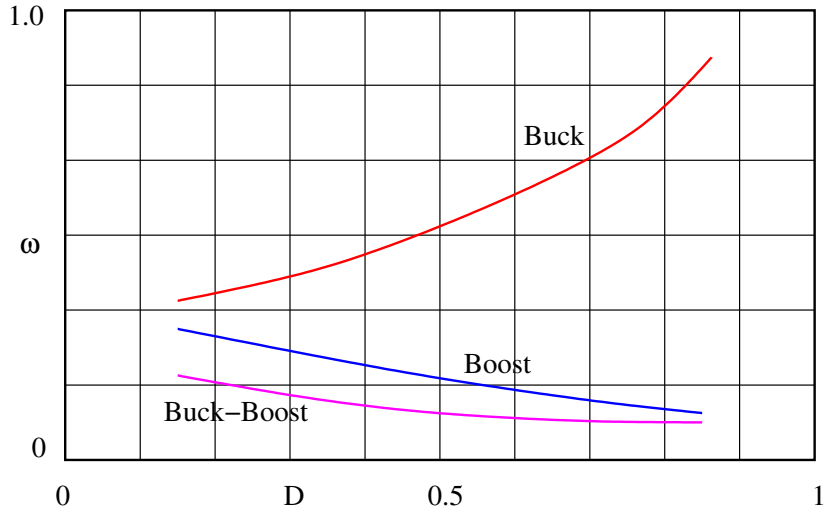

Figure C.2: Natural Frequency of Different Converters

C.1.4 Some Sample Converters

Buck Converter

Table C.9: Buck Converter

V_G	V_O	P_O	δ_i	δ_v	D	L^*	C^*	E^*
100	50	100	0.2	0.01	0.5	1.25	5	3.75

Boost Converter

Table C.10: Boost Converter

V_G	V_O	P_O	δ_i	δ_v	D	L^*	C^*	E^*
100	200	100	0.2	0.01	0.5	5	12.5	27.5

Buck-Boost Converter

Table C.11: Buck-Boost Converter

V_G	V_O	P_O	δ_i	δ_v	D	L^*	C^*	E^*
100	100	100	0.2	0.01	0.5	2.5	50	30

C.2 Problem Set

1. Derive the per unit description of the following converters. Verify that structurally the equations are identical to the normal description and that the parameters are replaced by the pu parameters.

   (A) Cuk Converter

   (B) Sepic Converter

   (C) Forward Converter

Appendix D

Visualisation of Functions

The skill of visualisation is essential for any designer. In this direction it will be good to develop such skills through visualisation of mathematical functions.

D.1 Mathematical Functions

D.1.1 Polynomials

A general polynominal function is given in Eq. 1.

$$y(t) = a_o + a_1 t + a_2 t^2 + ... \tag{D.1}$$

The simplest of the polynomial function is the constant function.

$$y(t) = a_o \tag{D.2}$$

This functional relationship is given in Fig. 1.

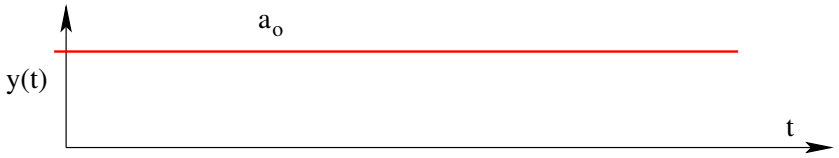

Figure D.1: A Constant Function

$$y(t) = a_o + a_1 t \tag{D.3}$$

The next level of complexity in such fuctions is the function given in Eq. 3. The functional relationship is shown in Fig. 2. Notice that this function y(t) is not linear in t. Verify that this relationship does not satisfy the conditions for linearity (homogeneity and superposition). Figure 3 shows the function which is linear ($y(t) = a_1 t$). Figure 4 shows the functions $y(t) = t$ and $y(t) = t^2$ on the same graph. It may be noticed that the function $y(t) = t$ is linear,

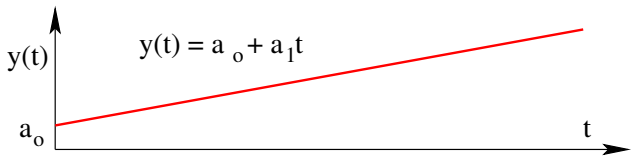

Figure D.2: A Polynomial Function of First Degree

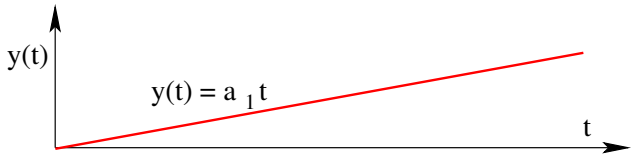

Figure D.3: A Polynomial Function Linear in t

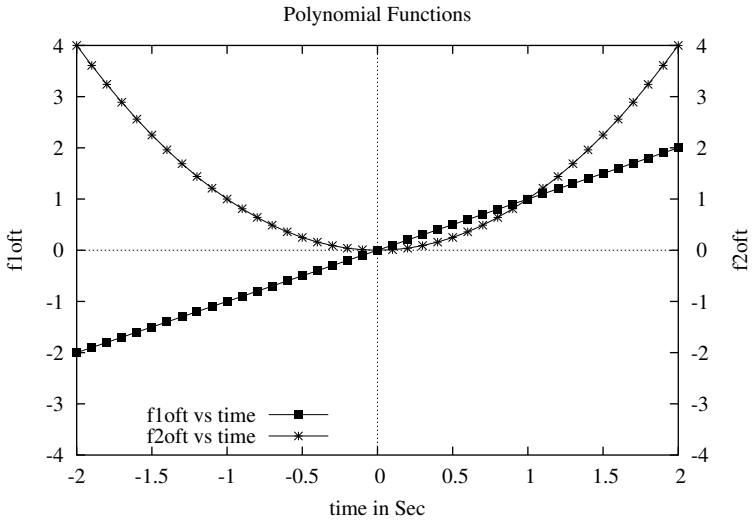

Figure D.4: Functions $y(t) = t$ and $y(t) = t^2$

while the function $y(t) = t^2$ is nonlinear. The function $y(t) = t$ is odd and the function $y(t) = t^2$ is even. Both the functions are continuous. It is a good practice to visualise functions, sketch the same and note the salient features of the fucntion such as properties of oddness or evenness, values at crucial points (such as $t = 0$, $t = 1$, $t = \infty$), polarity, minimum, maximum, slopes at crucial points, discontinuities if any, etc.

D.1.2 Exponential Function

The next level of complexity in functions leads to exponential function.

$$f(t) \;=\; e^t \tag{D.4}$$

The polynomial expansion of the exponential function is as given in Eq. [5].

$$e^t \;=\; 1 + \frac{t}{1!} + \frac{t^2}{2!} + \frac{t^3}{3!} + \;... \tag{D.5}$$

This exponential function in the interval $-2 < t < +2$ is shown in Fig. 5. The

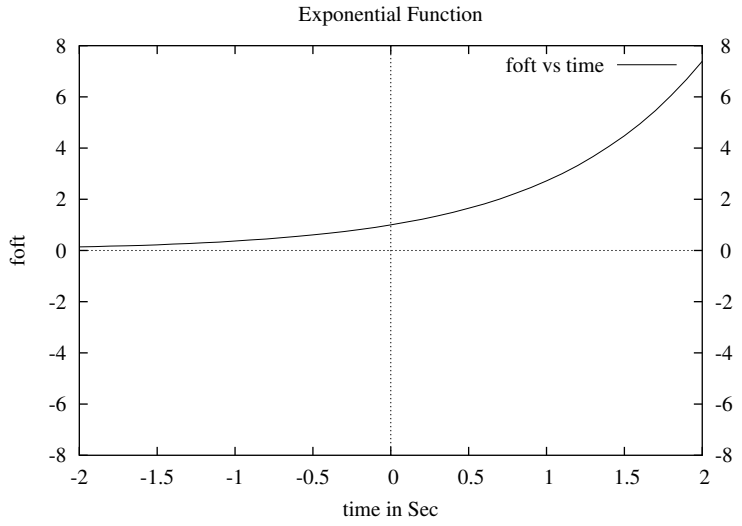

Figure D.5: Function $y(t) = e^t$

exponential function is neither even nor odd. The value of the function is 1 for $t = 0$. The function increases monotonically with time and goes to ∞ as time goes to ∞. Another important feature of the exponential function is that the slope of the function is the function itself $\left(\frac{dy}{dt} = y = e^t\right)$. At time $t = 0$, the functional value is 1 and so the slope $\left(\frac{dy}{dt}\right)$ of the function at $t = 0$.

Consider the function

$$f(t) \;=\; e^{-t} \tag{D.6}$$

The polynomial expansion of the exponential function is as given in Eq. [7].

$$e^{-t} \;=\; 1 - \frac{t}{1!} + \frac{t^2}{2!} - \frac{t^3}{3!} + ... \;=\; \frac{1}{1 + \frac{t}{1!} + \frac{t^2}{2!} + \frac{t^3}{3!} + ...} \tag{D.7}$$

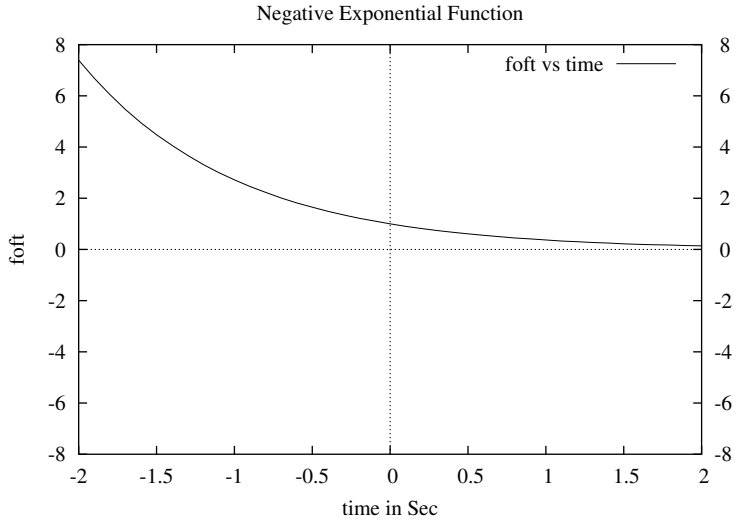

Figure D.6: Function $y(t) = e^{-t}$

The negative exponential function is also neither even nor odd. It may be seen that the negative exponential function is a mirror reflection of the positive exponential function about the y axis. The negative exponential function monotonically falls to 0 as t goes to ∞. The slope of the negative exponential function is negative of the function itself $\left(\frac{dy}{dt} = -y = -e^{-t}\right)$. At time $t = 0$, the functional value is 1 and the slope $\left(\frac{dy}{dt}\right)$ of the function at $t = 0$ is -1.

D.1.3 A Composite Function

We may now see a composite function which is a product of a simple polynomial and a negative exponential function.

$$f(t) \;=\; te^{-t} \tag{D.8}$$

The function may be decomposed into t and e^{-t}. The function t monotonically increases with t and goes to ∞ as t goes to ∞. The part e^{-t} is a monotonically decreasing function with t and goes to $infty$ as t goes to ∞. The product is 0 at $t = 0$ and at $t = \infty$. This may be verified by expanding e^{-t} in the denominator and taking in t to the denominator. We also see that the function has a maxima for some t between 0 and ∞. This may be verified to be at $t = 1$. The function $f(t) = te^{-t}$ is plotted for values $t = 0$ to 4 in Fig. 7.

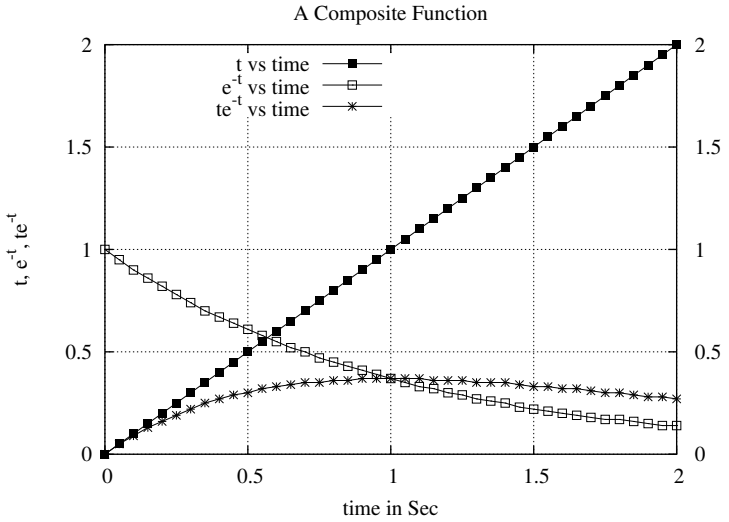

Figure D.7: Function $y(t) = te^{-t}$

D.1.4 Trigonometric Functions

Consider the following trigonometric functions.

$$f_1(t) = Sin(2\pi t) \tag{D.9}$$

$$f_2(t) = Cos(2\pi t) \tag{D.10}$$

Notice that the sine function is odd and the cosine function is even. The

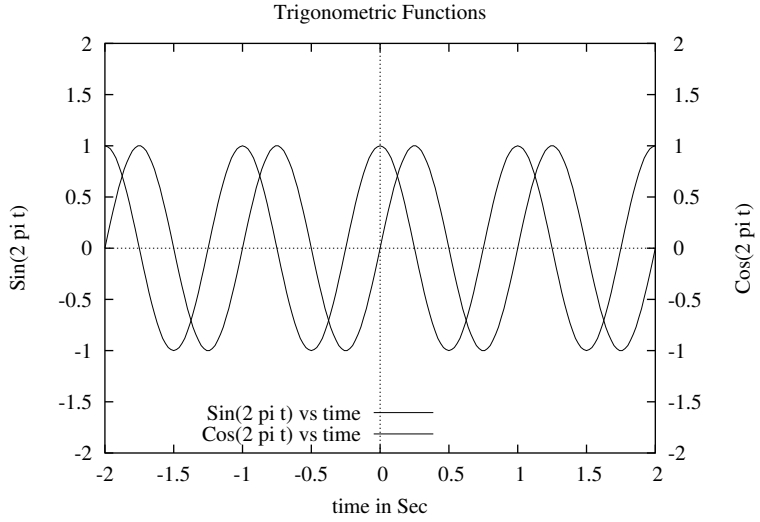

Figure D.8: Functions $Sin(2\pi t)$ and $Cos(2\pi t)$

functional value of these trigonometric functions are bounded between -1 and +1. It may also be seen that the slope of the sine function is a cosine function and the slope of the cosine function is a negative sine function. The period of the functions is one second.

D.1.5 Composite Trigonometric Functions

Consider the following composite transfer functions.

$$f_1(t) = t\ Sin(2\pi t) \tag{D.11}$$

$$f_2(t) = t\ Cos(2\pi t) \tag{D.12}$$

The composite trigonometic functions $t\ Sin(2\pi t)$ and $t\ Cos(2\pi t)$ are shown in

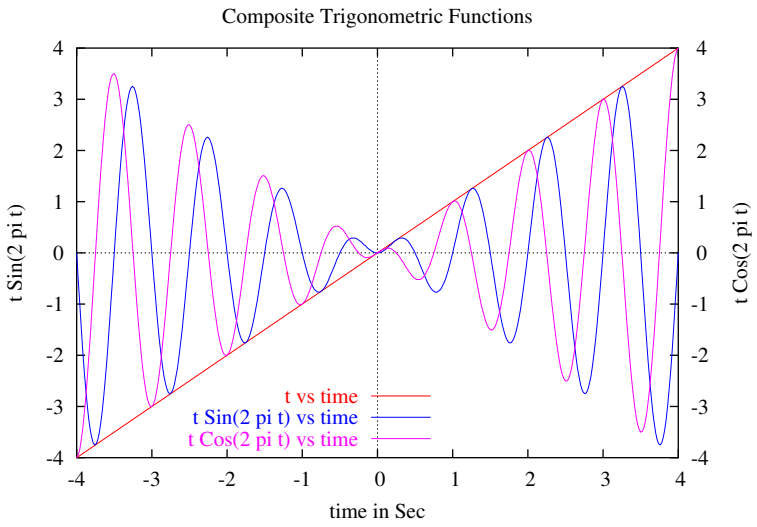

Figure D.9: Functions $t\ Sin(2\pi t)$ and $t\ Cos(2\pi t)$

Fig. 9. The function $t\ Sin(2\pi t)$ is an even function. The function $t\ Cos(2\pi t)$ is an odd function. Notice that the functions are enveloped by the line $y = t$.

D.1.6 Hyperbolic Functions

Consider the following composite transfer functions.

$$f_1(t) = Sinh(t) \tag{D.13}$$

$$f_2(t) = Cosh(t) \tag{D.14}$$

The composite trigonometic functions $Sinh(t)$ and $Cosh(t)$ are shown in Fig. 10. The function $Cosh(t)$ is an even function. The function $Sinh(t)$ is an odd function. Notice that both functions go to ∞ as t goes to ∞. An important

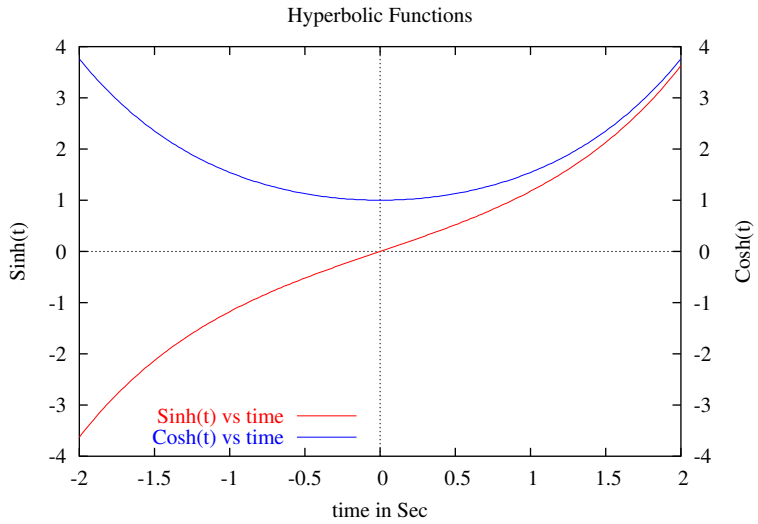

Figure D.10: Functions $Sinh(t)$ and $Cosh(t)$

advantage of visualisation of functions is that we will be able to obtain simple approximations to complex functions in the regions of interest to us. Notice that the functions $Sinh\ (t)$ and $Cosh\ (t)$ are nearly equal when t is large ($t\ >\ 2$). Similarly for low values of t ($t\ <\ -2$), $Cosh\ (t)$ is negative of $Sinh\ (t)$. We also notice that for small values of t, $Cosh(t)$ is 1, and $Sinh(t)$ is t. Such approximations become easy when we develop the habit of visualising the functions.

D.2 Functions as Differential Equations

In the previous section we saw several simple functions such as polynomials, exponential functions, trigonometric functions, hyperbolic functions etc. They all appear to belong to different families of functions. We may look at all these functions to be solutions of differential mathematical equations. Such a perception will bring out the common features among several functions. Consider for example the differential equation,

$$\frac{dy}{dt}\ =\ a_1 \tag{D.15}$$

By simple integration, we may solve this and write the solution as

$$y\ =\ a_1 t\ +\ a_o \tag{D.16}$$

This function is the same as the one visualised in Fig. 2.
Consider the differential equation,

$$\frac{dy}{dt}\ =\ \pm\ y \tag{D.17}$$

By simple integration, we may solve this and write the solution as

$$y \;=\; e^{\pm\, t} \tag{D.18}$$

This function is the same as the one visualised in Figs. 5 and 6.
Consider the differential equation,

$$\frac{d^2y}{dt^2} \;=\; \pm\, y \tag{D.19}$$

By simple integration, we may solve this and write the solution as

$$y \;=\; A\; Sin(t) \;+\; B\; Cos(t) \tag{D.20}$$

The constants in the solution A and B depend on the initial conditions on y and $\frac{dy}{dt}$. This function is similar to the ones visualised in Fig. 8. In general any of these functions can be represented by the general differential equation as follows.

$$f(D, y) \;=\; 0 \tag{D.21}$$

D is the differential operator $\frac{d}{dt}$.

D.2.1 Some Common Functions as Differential Equations

The following are some of the common functions in the form of a differential finction. Note that it is necessary to define adequate number of initial conditions.

Constant Function

$$\frac{dy}{dt} \;=\; 0;\; y(0) \;=\; 1; \tag{D.22}$$

$$y(t) \;=\; 1$$

Linear Polynomial

$$\frac{dy}{dt} \;=\; a_1;\; y(0) \;=\; a_o; \tag{D.23}$$

$$y(t) \;=\; a_o \;+\; a_1\; t$$

Positive Exponential Function

$$\frac{dy}{dt} \;=\; \omega\; y;\; y(0) \;=\; a_o; \tag{D.24}$$

$$y(t) \;=\; a_o\; e^{\omega\; t}$$

Negative Exponential Function

$$\frac{dy}{dt} = -\omega\ y;\ y(0) = a_o; \tag{D.25}$$
$$y(t) = a_o\ e^{-\omega\ t}$$

Cosinusoidal Function

$$\frac{d^2y}{dt^2} = -\omega^2\ y;\ y(0) = a_o;\ \left(\frac{dy}{dt}\right)_{t=0} = 0; \tag{D.26}$$
$$y(t) = a_o\ Cos\ (\omega t)$$

Sinusoidal Function

$$\frac{d^2y}{dt^2} = -\omega^2\ y;\ y(0) = 0;\ \left(\frac{dy}{dt}\right)_{t=0} = b_o\ \omega; \tag{D.27}$$
$$y(t) = b_o\ Sin\ (\omega t)$$

Mixed Trigonometric Function

$$\frac{d^2y}{dt^2} = -\omega^2\ y;\ y(0) = a_o;\ \left(\frac{dy}{dt}\right)_{t=0} = b_o\ \omega; \tag{D.28}$$
$$y(t) = a_o\ Cos\ (\omega t) + b_o\ Sin\ (\omega t)$$

Hyperbolic Cosine Function

$$\frac{d^2y}{dt^2} = \omega^2\ y;\ y(0) = a_o;\ \left(\frac{dy}{dt}\right)_{t=0} = 0; \tag{D.29}$$
$$y(t) = a_o\ Cosh\ (\omega t)$$

Hyperbolic Sine Function

$$\frac{d^2y}{dt^2} = \omega^2\ y;\ y(0) = 0;\ \left(\frac{dy}{dt}\right)_{t=0} = b_o\ \omega; \tag{D.30}$$
$$y(t) = b_o\ Sinh\ (\omega t)$$

Mixed Hyperbolic Function

$$\frac{d^2y}{dt^2} = \omega^2\ y;\ y(0) = a_o;\ \left(\frac{dy}{dt}\right)_{t=0} = b_o\ \omega; \tag{D.31}$$
$$y(t) = a_o\ Cosh\ (\omega t) + b_o\ Sinh\ (\omega t)$$

Mixed Exponential Function

Consider the following differential equation.

$$\frac{d^2y}{dt^2} - 2\frac{dy}{dt} + y = 0 \tag{D.32}$$

Verify by substitution that the solution to the above equation is given by

$$y(t) = A\ t\ e^t + B\ e^t$$

State the intitial conditions under which the solution will reduce to

$$y(t) = A\ t\ e^t$$

Consider the following differential equation.

$$\frac{d^2y}{dt^2} + 2\frac{dy}{dt} + y = 0 \tag{D.33}$$

Verify by substitution that the solution to the above equation is given by

$$y(t) = A\ t\ e^{-t} + B\ e^{-t}$$

State the intitial conditions under which the solution will reduce to

$$y(t) = A\ t\ e^{-t} + B\ e^{-t}$$

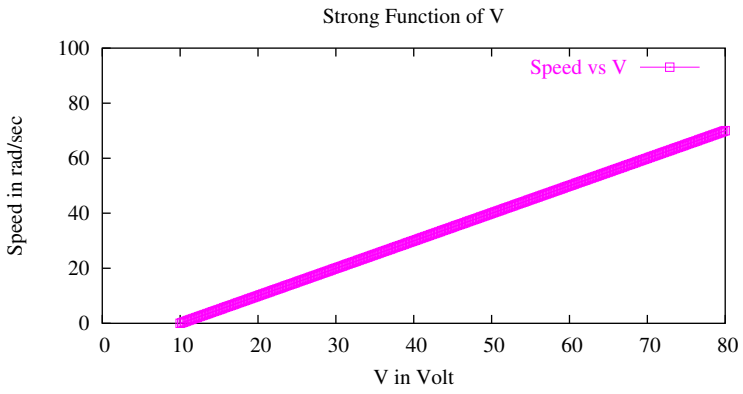

Figure D.11: Function *Speed* vs V at a fixed Torque

D.3 Strong and Weak Functions

Visualisation of functions will bring out an important feature of a function namely strong and weak relationships. Consider the following voltage equation of a separately excited dc machine.

$$V = K\ \Omega + I_a R_a \tag{D.34}$$

For, $I = 10\ A$, $R_a = 1\ \Omega$, $K = 1\ V sec/rad$, the function Speed (Ω) is plotted for different values of V. The function is shown in Fig. 11. It is

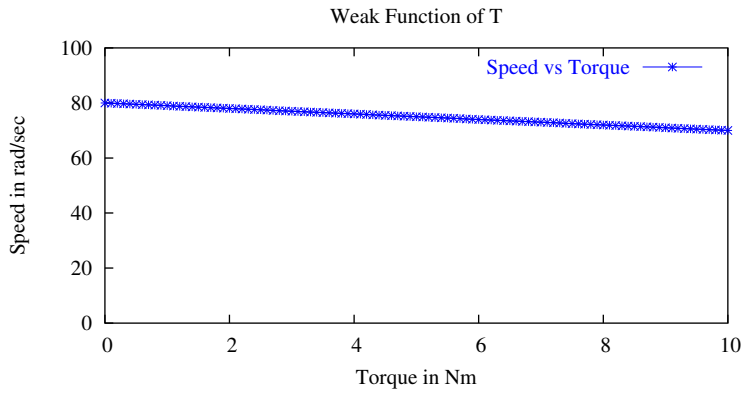

Figure D.12: Function *Speed* vs T at a fixed Voltage

seen that the speed is a strong function of V. Figure 12 shows the speed as a function of torque. It may be seen that the speed is a weak function of torque in a separately excited dc machine.
Consider the function $Y = f(X)$ as shown in Fig. 13. It may be seen that Y is a weak function of X in the range of $0 < X < 15$. In the range $15 < X < 40$, Y is a strong function of X.

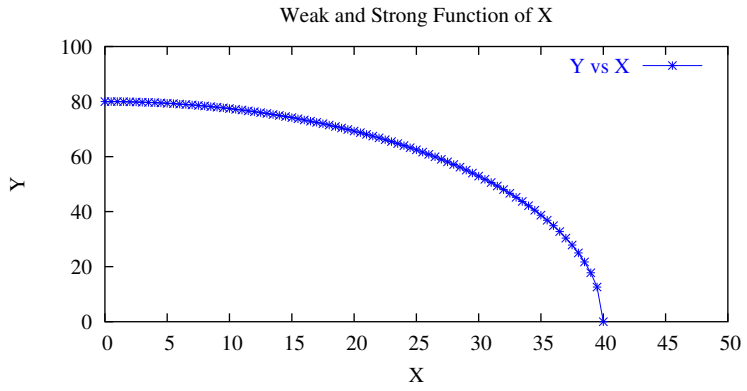

Figure D.13: Function Y vs X which is both Strong and Weak Function

D.4 Linear and Non-linear Functions

Linear and non-linear functions can be visualised to get a broader and deeper understanding. Consider the function

$$V_o = \frac{V_g}{(1-d)} \left\{ \frac{1}{1 + \frac{\alpha}{(1-d)^2}} \right\} \tag{D.35}$$

This is the gain relationship of the output voltage V_o of a boost converter as a function of input voltage V_g, duty ratio d, and parasitic resistance ratio $\alpha = R_l/R$. It is seen that this gain relationship is linear between V_g and V_o, and non-linear between d and V_o. This may be seen from Figs. 14 and 15.

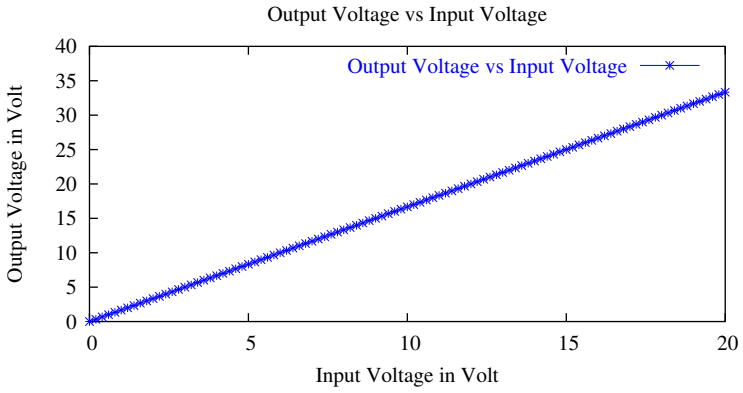

Figure D.14: Linear Relationship V_o vs V_g for $d = 0.5$ and $\alpha = 0.05$

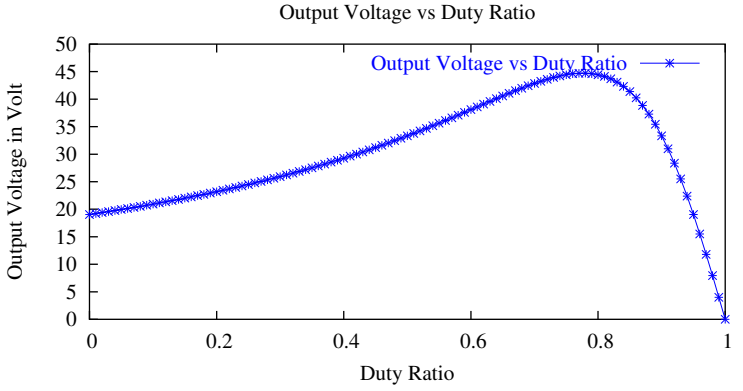

Figure D.15: Non-linear Relationship V_o vs d at $V_g = 20\ V$

Other features that may be noticed in Fig. 15 are the maximum present in the

gain, positive incremental gain for small values of d, and negative incremental gain for large values of d.

D.5 Steady-State and Dynamic Performance

In many situations, it will be advantageous to visualise the steady-state and dynamic performance in a single picture. Such a visualisation will add to the understanding of the performance of the system. Consider the dynamic equation:

$$\frac{d\omega}{dt} = \frac{T_G - T_L}{J} \tag{D.36}$$

This is the dynamic equation of a rotary mechanical system (e.g. a motor connected to a load). Under steady-state, the solution to the above equation

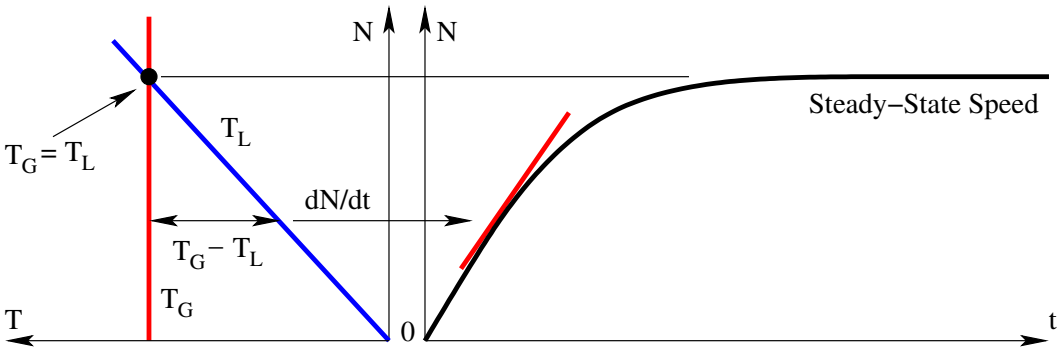

Figure D.16: Acceleration Characteristics of a Mechanical System

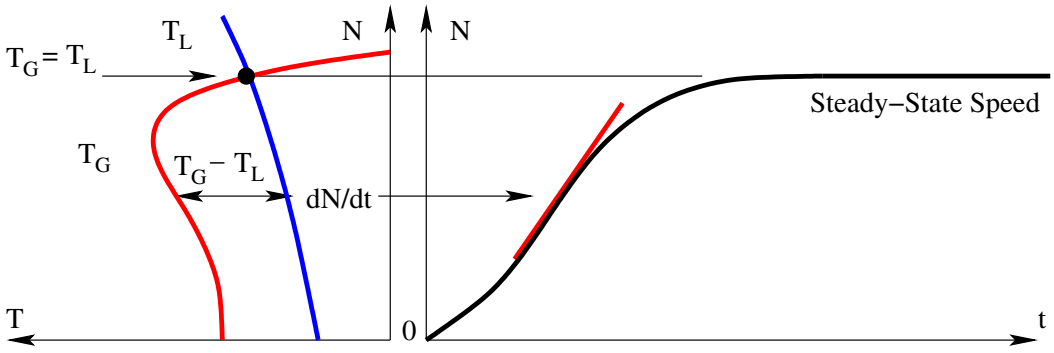

Figure D.17: Starting Characteristics of an Induction Motor

will be $T_G = T_L$. During transient conditions, the rate of change of angular velocity ω (or the rate of change of speed N in rpm), is related to the net torque

$(T_G - T_L)$. Both these features of steady-state and dynamic performance can be visualised in a single picture shown in Fig. 16. On the left hand side is the figure T_G *vs* N and T_L *vs* N. Here the steady-state is indicated by the point where $T_G = T_L$. In this picture, we may notice the accelerating torque to be $T_G - T_L$, marked accordingly for any speed. The figure on the right hand side shows N *vs* t. At any speed, the rate of change of speed dN/dt is related to the net accelerating torque as marked in the picture. Figure 17 shows the starting characteristics of an induction motor connected to a load. The load (T_L) characteristics shows a torque requirement non-linear with the speed. The generated torque (T_G) of the motor is also non-linear with speed. The various features of the starting characteristics may be seen in Fig. 17.

D.6 Impedance Functions

Many circuit impedance functions and approximations may be done conveniently, if impedances are visualised as suitable functions. Figure 18 shows the $|Z|$ of circuit elements expressed in $dB\ \Omega$ against frequency ($log\ rad/sec$).

The impedance of inductance is seen as a straight line with a slope of

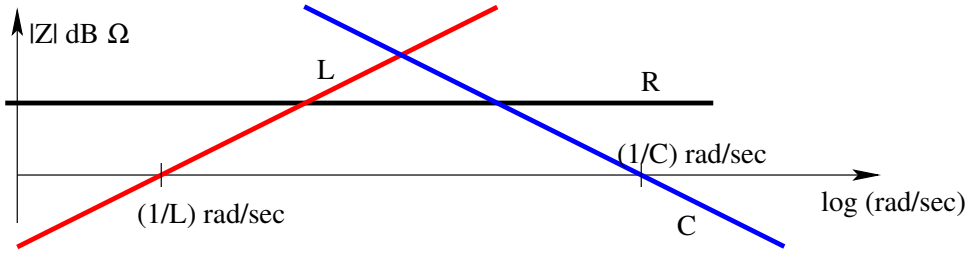

Figure D.18: Impedance of Simple Circuit Elements

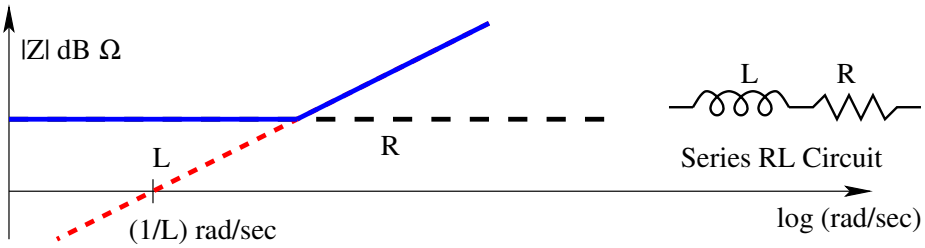

Figure D.19: A Series RL Circuit

20 $dB\Omega/decade$ with an x axis intercept of $1/L$ rad/sec. The impedance of capacitance is seen as a straight line with a slope of $-20\ dB\Omega/decade$ with an x axis intercept of $1/C$ rad/sec.

D.6.1 Series RL Circuit

Consider a series RL circuit as shown in Fig. 19. In a series circuit, the higher of the impedances will prevail. This may be readily seen in the figure.

D.6.2 Shunt RC Circuit

Consider a shunt RC circuit as shown in Fig. 20. In a shunt circuit, the lower of the impedances will prevail. This may be readily seen in the figure.

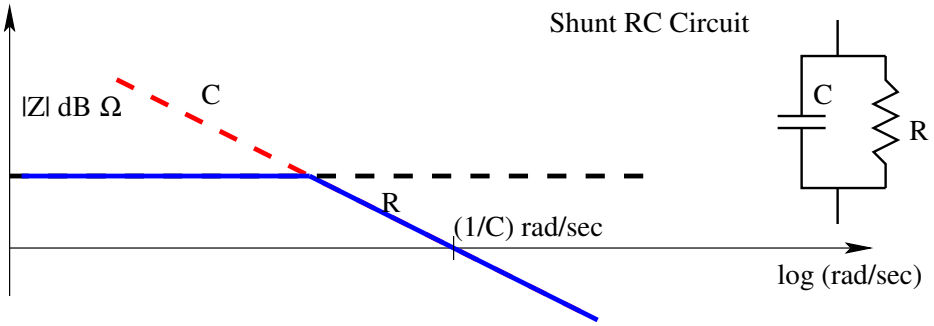

Figure D.20: A Shunt RC Circuit

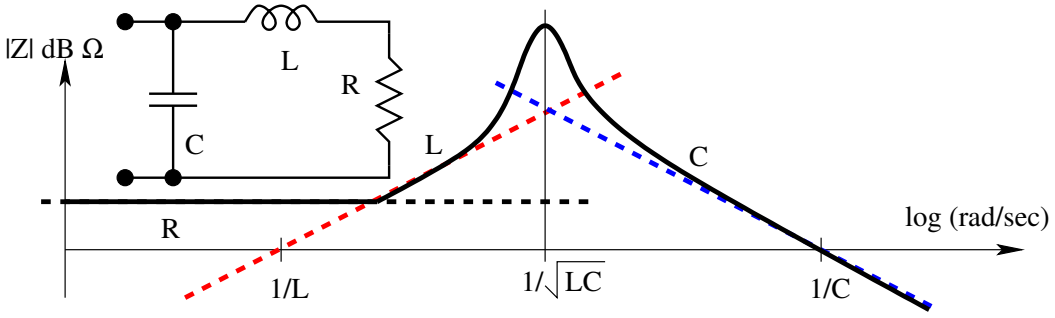

Figure D.21: A Composite RLC Circuit

D.6.3 A Composite RLC Circuit

Consider the circuit shown in Fig. 21. The circuit consists of a capacitor in parallel with a series RL circuit. The impedance diagram is shown in Fig. 21. The parallel resonance of L and C is also seen in the impedance diagram. The intercepts of the asymptotes give the various circuit elements as well.

D.7 Rational Polynomials

In power electronics, we come across several functions which are rational polynomials. These could be transfer functions of linear systems, impedance functions, admittance functions etc. In general, these functions are all referred to as network functions. All these functions may be visualised in the form of magnitude and phase plots (bode plots) as a function of frequency. Many design problems can be solved graphically with considerable ease without compromising on the quality/accuracy/effectiveness of the solutions.
Consider the network function:

$$G(s) = \frac{N(s)}{D(s)} = \frac{a_m s^m + a_{m-1}s^{m-1} + ... + a_2 s^2 + a_1 s + a_0}{b_n s^n + b_{n-1}s^{n-1} + ... + b_2 s^2 + b_1 s + b_0} \tag{D.37}$$

This function may be factorised and put into normalised pole-zero form as below.

$$G(s) = G(0) \frac{\left(1 + \frac{s}{\omega_{z1}}\right)\left(1 + \frac{s}{Q_{zo}} + \frac{s^2}{\omega_{zo}^2}\right) ...}{\left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{Q_{po}} + \frac{s^2}{\omega_{po}^2}\right) ...} \tag{D.38}$$

$$G(s) = G(0) \frac{Nrz(s)Nsz(s) ...}{Drp(s)Dsp(s) ...} \tag{D.39}$$

The network function $G(s)$ is seen as having a dc value $G(0)$ and several real simple zeroes (N_{rz}), complex (N_{cz}), real simple poles (D_{rp}), and complex poles (D_{cp}). These functions are best visualised as bode plots - magnitude plot in dB vs frequency in $log\ (rad/sec)$. Figure 22 shows the asymptotic magnitude

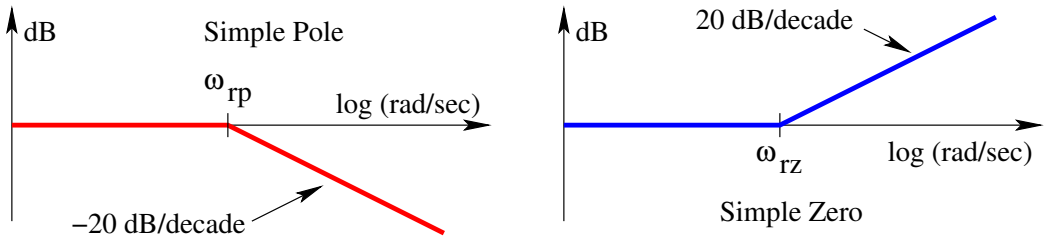

Figure D.22: Asymptotic Magnitude Plots of $D_{rp}(s)$ and $N_{rz}(s)$

plots for normalised simple real pole $D_{rp}(s)$ and normalised simple real zero $N_{rz}(s)$. Figure 23 shows the asymptotic magnitude plots for complex pole pair $D_{cp}(s)$ and normalised complex zero pair $N_{cz}(s)$. It may be seen that the plot for zeroes is the mirror reflection (on the 0 dB axis) of the plot for poles. The overall plot for the network function $G(s)$ will be the sum of the individual plots for $G(0)$, $N(s)$, $D(s)$ etc. Consider the network function given by the

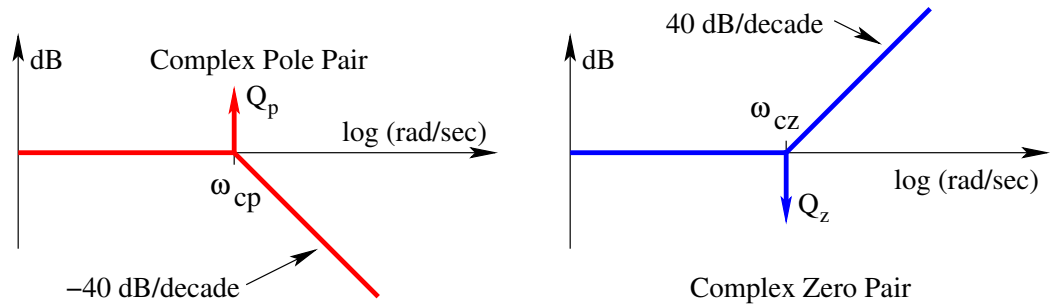

Figure D.23: Asymptotic Magnitude Plots of $D_{cp}(s)$ and $N_{cz}(s)$

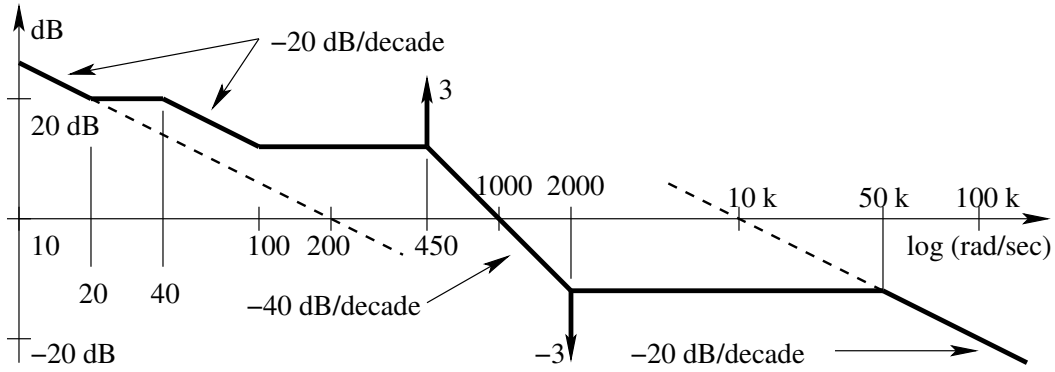

Figure D.24: Asymptotic Magnitude Plot of a Network Function

following rational polynomial.

$$G(s) = \frac{200}{s} \frac{\left(1+\frac{s}{20}\right)\left(1+\frac{s}{100}\right)\left(1+\frac{s}{3*2000}+\frac{s^2}{2000^2}\right)}{\left(1+\frac{s}{40}\right)\left(1+\frac{s}{3*447}+\frac{s^2}{447^2}\right)\left(1+\frac{s}{50000}\right)} \tag{D.40}$$

Figure 24 shows the asymptotic magnitude plot of the network function $G(s)$. The low frequency asymptote is seen as $200/s$. The high frequency asymptote is seen as $10000/s$. The network function also shows two resonances - one at 447 rad/sec and another at 2000 rad/sec. Figure 25 shows the asymptotic magnitude plot of an impedance function. From the plot it is possible to write the impedance function by inspection as follows.

$$Z(s) = \frac{s}{160} \frac{\left(1+\frac{s}{50}\right)\left(1+\frac{s}{5*2000}+\frac{s^2}{2000^2}\right)}{\left(1+\frac{s}{20}\right)\left(1+\frac{s}{10*200}+\frac{s^2}{200^2}\right)\left(1+\frac{s}{10000}\right)\left(1+\frac{s}{20000}\right)} \tag{D.41}$$

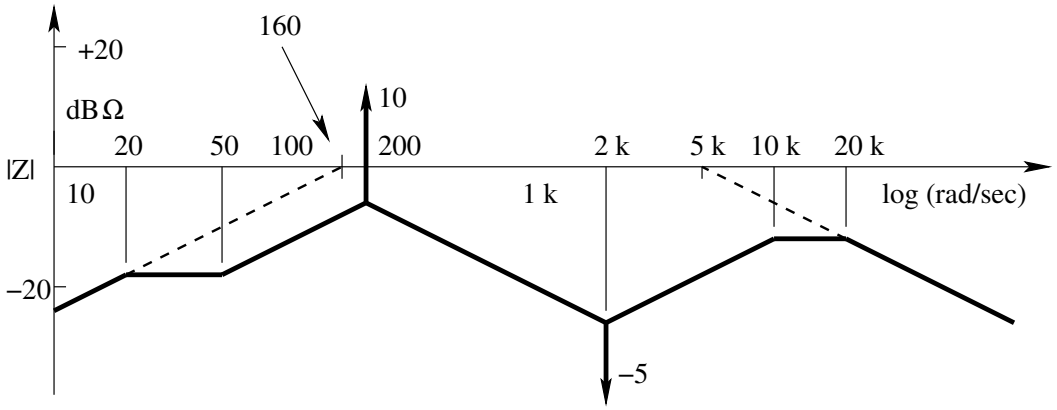

Figure D.25: Asymptotic Magnitude Plot of an Impedance Function

It may be observed that the circuit is effectively an inductance of 6250 μH at low frequencies - below 20 rad/sec - $(s/160)$, and a capacitance of 200 μF at high frequencies - above 20000 rad/sec - $(5000/s)$. It may also be seen that the circuit exhibits two resonances - one at 200 rad/sec, and another at 2000 rad/sec. Figure 26 shows the circuit whose impedance is given in Fig. 25.

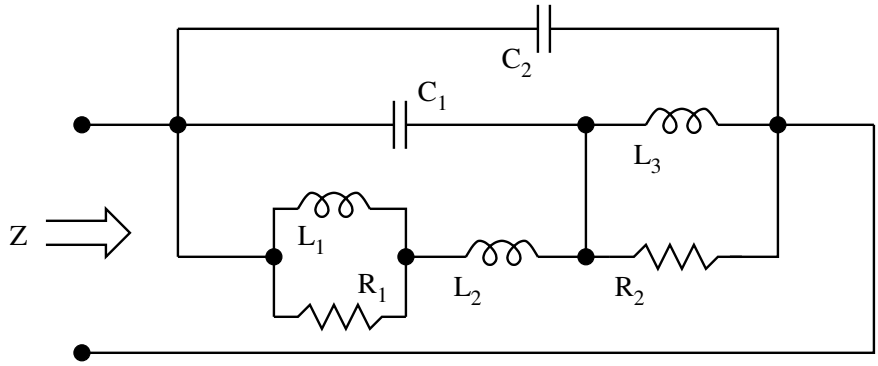

Figure D.26: The Circuit Realisation of the Impedance Function in Fig. 25

It is left as an exercise to relate the element values in Fig. 26 to the various frequencies in Fig. 25.

D.8 Periodic Functions

Periodic functions play a very important role in ac circuits. Decomposition of periodic functions into fundamental frequency component and higher harmonis is a standard method in ac circuit analysis. Figure 27 shows a typical periodic circuit waveform. In the analysis of periodic waveforms, fourier series

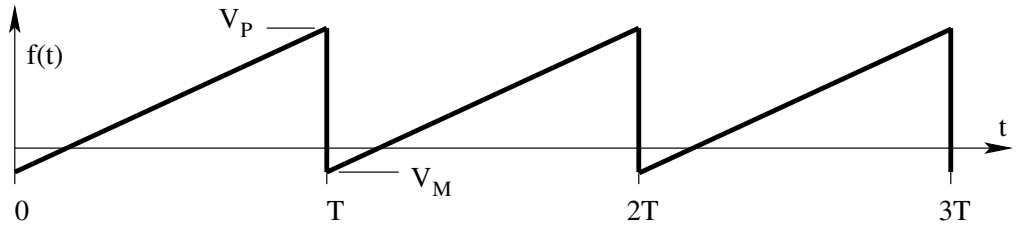

Figure D.27: A Typical Periodic Circuit Waveform

decomposition is very useful. The fourier series decomposition of the periodic waveform shown in Fig. 27 is written as follows.

$$f(t) \;=\; \frac{a_o}{2} \;+\; \sum_{n=1}^{\infty} \; a_n \; Cos \; n\omega t \;+\; \; b_n \; Sin \; n\omega t \tag{D.42}$$

$$\omega \;=\; \frac{2\pi}{T} \tag{D.43}$$

$$a_0 \;=\; \frac{1}{T} \; \int_0^T \; f(t) \; dt \tag{D.44}$$

$$a_n \;=\; \frac{2}{T} \; \int_0^T \; f(t) \; Cos \; n\omega t \; dt \tag{D.45}$$

$$b_n \;=\; \frac{2}{T} \; \int_0^T \; f(t) \; Sin \; n\omega t \; dt \tag{D.46}$$

The coefficients a_n are the even fourier coefficients of $f(t)$ and b_n are the odd fourier coefficients of $f(t)$.

D.8.1 Certain Symmetries

The coefficient a_0 is the average value of the periodic function $f(t)$ as given in Eq. [44]. Figure 28 shows two periodic waveforms whose average value is

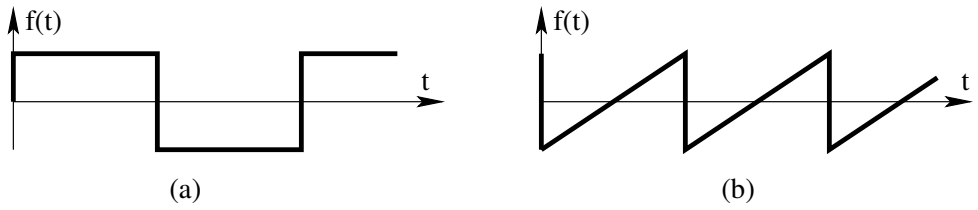

Figure D.28: Two Periodic Waveforms with Zero Average Value

zero. It is obvious that for these functions, the coefficient a_0 is zero. Figure 29 shows two periodic waveforms with non-zero average value and therefore non-zero a_0. It is possible therefore by inspecting a periodic waveform, to

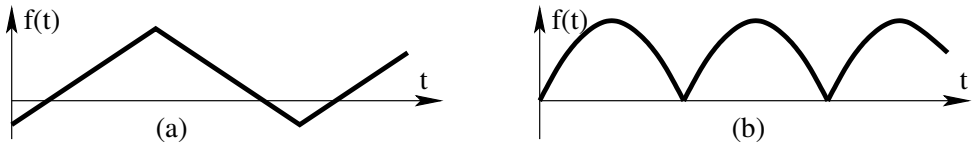

Figure D.29: Two Periodic Waveforms with Non-Zero Average Value

conclude if the function has average value or in other words zero or non-zero coefficient a_0. In a similar way it is possible to conclude zero or non-zero values of a_n and b_n. Periodic functions which are even, will have only non-zero a_n. Periodic functions which are odd, will have only non-zero b_n. Functions which are neither even nor odd will have both a_n and b_n. In other words, odd periodic functions may be decomposed into sine series; even periodic functions may be decomposed into cosine series. General periodic functions which are neither odd or even may be decomposed into sum of one even and one odd periodic function. These functions may be respectively expanded into a cosine series and a sine series respectively. For example consider the periodic function $f(t)$. This may be decomposed into an even function $f_e(t)$ and an odd function $f_o(t)$.

$$f_e(t) = \frac{f(t) + f(-t)}{2} \tag{D.47}$$

$$f_o(t) = \frac{f(t) - f(-t)}{2} \tag{D.48}$$

Figure 30 shows two even functions. They have only cosine terms. Figure 31

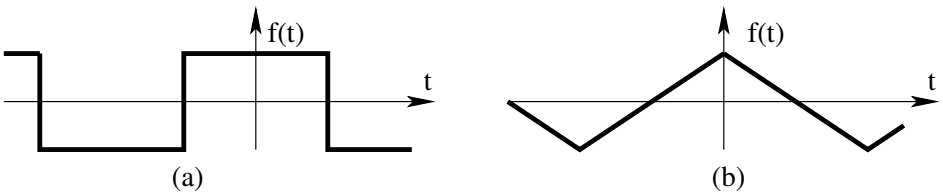

Figure D.30: Two Even Periodic Waveforms

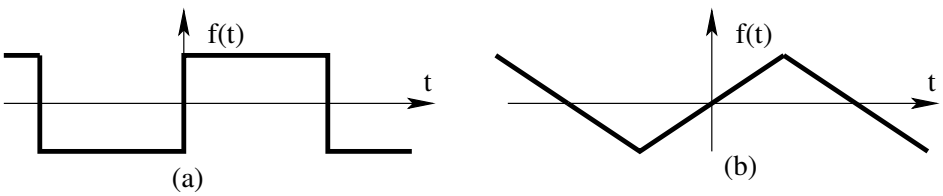

Figure D.31: Two Odd Periodic Waveforms

shows two odd functions which have only sine terms. It may also be noticed that pure odd/even functions may be seen as even/odd functions by just shifting the origin. In power electronic systems, power source is synthesised with electronic switches. Pulse width modulation is employed in order to synthesise voltages/currents with low harmonic content. In such cases it is usual to seek zero average voltage from inverters, eliminate even harmonics and push the lowest order harmonics to as high a frequency as possible. It may be verified

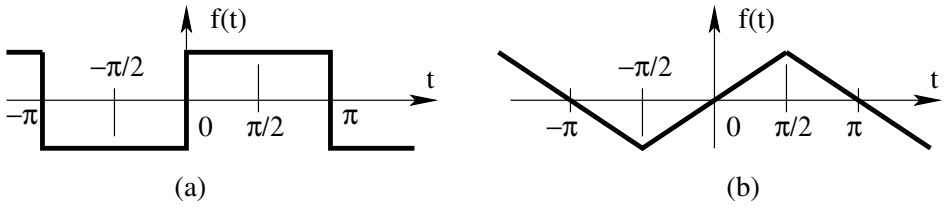

Figure D.32: Quarter Wave Symmetry in Odd Functions

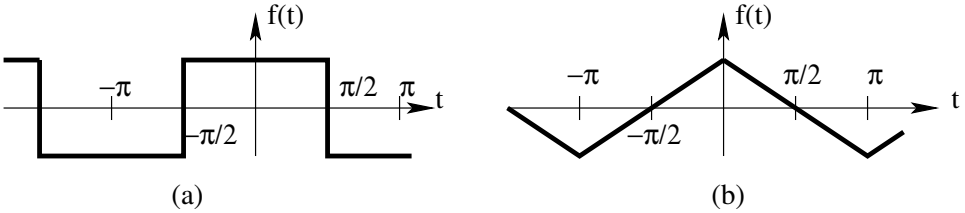

Figure D.33: Quarter Wave Symmetry in Even Functions

that functions exhibiting quarter wave symmetry as shown in Fig. 32 and Fig. 33 do not have even harmonics.

Appendix E

Transients in Linear Electric Circuits

Power electronic circuits consist of electric circuit elements connected with one or more switches. The circuit elements are R, L, and C. These circuits are piece-wise (for each switch position) linear. Therefore it is helpful to catalogue and analyse such circuits in their generic form. These results may be adopted as and when necessary while analysing power electronic circuits.

E.1 Series RC Circuit

Figure 1 shows a series RC circuit, excited by a voltage source V_i, and switched (S closed) at $t = 0$. The initial voltage on the capacitor is $V(0)$. The desired analytical result is $V(t)$.

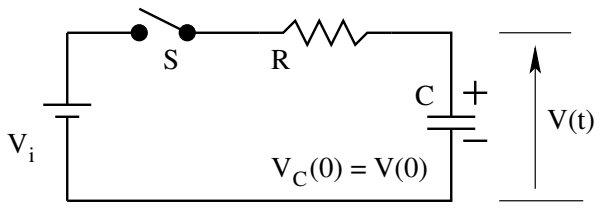

Figure E.1: A Series RC Circuit Excited with a Voltage Source

$$V(t) = V(0)\, e^{-t/RC} + V_i \left(1 - e^{-t/RC}\right) \tag{E.1}$$

E.2 Shunt RL Circuit

Figure 2 shows a shunt RL circuit, excited by a current source I_i, and switched (S opened) at $t = 0$. The initial current in the inductor is $I(0)$. The desired analytical result is $I(t)$. This circuit is the dual of the circuit in Fig. 1.

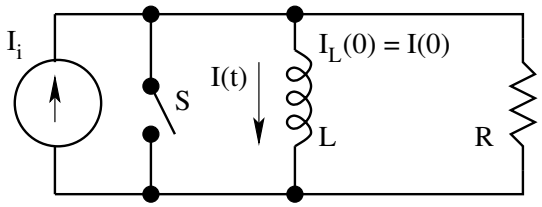

Figure E.2: A Shunt RL Circuit Excited with a Current Source

$$I(t) \;=\; I(0)\; e^{-Rt/L} \;+\; I_i \;\left(1 \;-\; e^{-Rt/L}\right) \tag{E.2}$$

E.3 Series RL Circuit

Figure 3 shows a series RL circuit, excited by a voltage source V_i. The initial current on the inductor is $I(0)$. The desired analytical result is $I(t)$. The throw positions T_1 and T_2 of the switch are respectively the freewheeling (discharging) and power transfer (charging) positions. The switch S is thrown from T_2 to

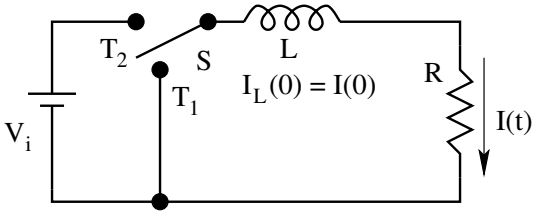

Figure E.3: A Series RL Circuit Excited with a Voltage Source

T_1 at $t \;=\; 0$.

$$I(t) \;=\; I(0)\; e^{-Rt/L} \tag{E.3}$$

When we consider that the switch S is thrown from T_1 to T_2 at $t \;=\; 0$,

$$I(t) \;=\; I(0)\; e^{-Rt/L} \;+\; \frac{V_i}{R}\;\left(1 \;-\; e^{-Rt/L}\right) \tag{E.4}$$

E.4 Shunt RC Circuit

Figure 4 shows a shunt RC circuit, excited by a current source I_i. The initial voltage on the capacitor is $V(0)$. The desired analytical result is $V(t)$. The throw positions T_1 and T_2 of the switch are respectively the freewheeling (discharging) and power transfer (charging) positions. The switch S is thrown from T_2 to T_1 at $t \;=\; 0$.

$$V(t) \;=\; V(0)\; e^{-t/RC} \tag{E.5}$$

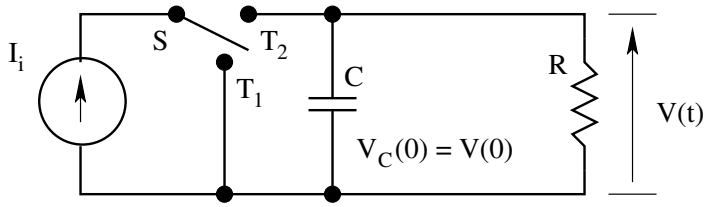

Figure E.4: A Shunt RC Circuit Excited with a Current Source

When we consider that the switch S is thrown from T_1 to T_2 at $t = 0$,

$$V(t) = V(0)\, e^{-t/RC} + I_i\, R \left(1 - e^{-t/RC}\right) \tag{E.6}$$

The circuits in Fig. 3 and Fig. 4 are dual of each other.

E.5 Series LC Circuit

Figure 5 shows a series LC circuit, excited by a voltage source V_i. The initial voltage on the capacitor is $V(0)$. The desired analytical result is $V(t)$ and $I(t)$. The switch S is closed at $t = 0$.

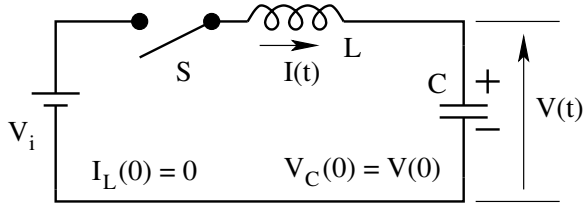

Figure E.5: A Series LC Circuit Excited with a Voltage Source

$$I(t) = (V_i - V(0)) \sqrt{\frac{C}{L}}\, sin\, \frac{t}{\sqrt{LC}} \tag{E.7}$$

$$V(t) = V_i - (V_i - V(0))\, cos\, \frac{t}{\sqrt{LC}} \tag{E.8}$$

Figure 6 shows the inductor current and capacitor voltage for $V_i = 10\ V$, $V(0) = 5\, V$, $L = 1\, H$, and $C = 1\, F$. Notice the starting values of $I(0) = 0$ and $V(0) = 5\, V$. The circuit is loss-less and therefore the current drawn from the source is a pure sinusoid. It may be also noticed that the average voltage on the capacitor is $V_i = 10\ V$. This also confirms that the average dc voltage across the inductor is 0. The current peak is seen to be the net circuit voltage $(V_i - V(0)))$ divided by the natural impedance $\left(Z = \sqrt{\frac{L}{C}}\right)$. The frequency of oscillation is seen to have a period of 2π $(T = 2\pi\sqrt{LC})$ seconds.

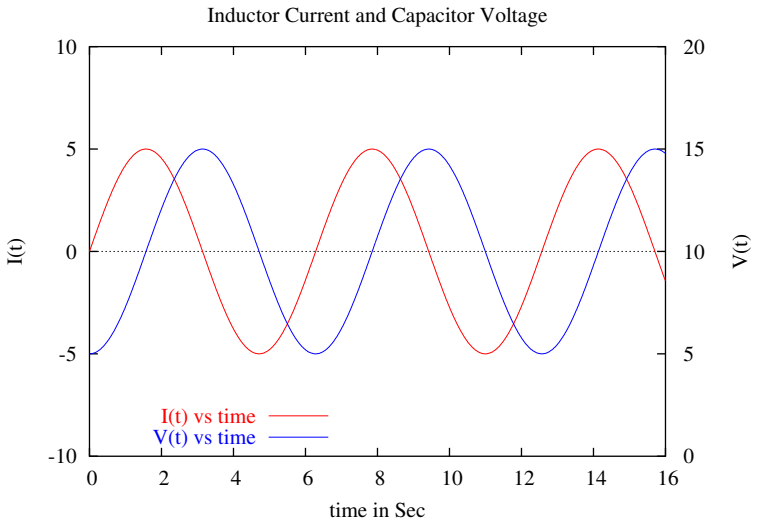

Figure E.6: The Inductor Current and Capacitor Voltage

E.6 Shunt LC Circuit

Figure 7 shows a series LC circuit, excited by a current source I_i. The initial current in the inductor is $I(0)$. The desired analytical result is $V(t)$ and $I(t)$. The switch S is opened at $t = 0$.

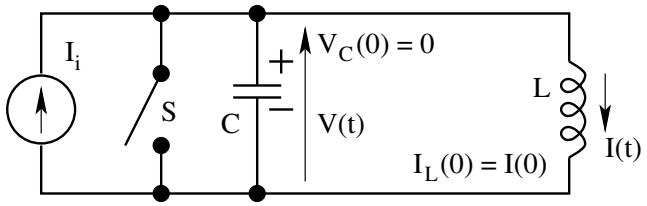

Figure E.7: A Shunt LC Circuit Excited with a Current Source

$$V(t) = (I_i - I(0)) \sqrt{\frac{L}{C}}\, sin\, \frac{t}{\sqrt{LC}} \tag{E.9}$$

$$I(t) = I_i - (I_i - I(0))\, cos\, \frac{t}{\sqrt{LC}} \tag{E.10}$$

Figure 8 shows the inductor current and capacitor voltage for $I_i = 10\ A$, $I(0) = 5\ A$, $L = 1\ H$, and $C = 1\ F$. Notice the starting values of $V(0) = 0$ and $I(0) = 5\ A$. The circuit is loss-less and therefore the voltage across the source is a pure sinusoid. It may be also noticed that the average current on the inductor is $I_i = 10\ A$. This also confirms that the average dc

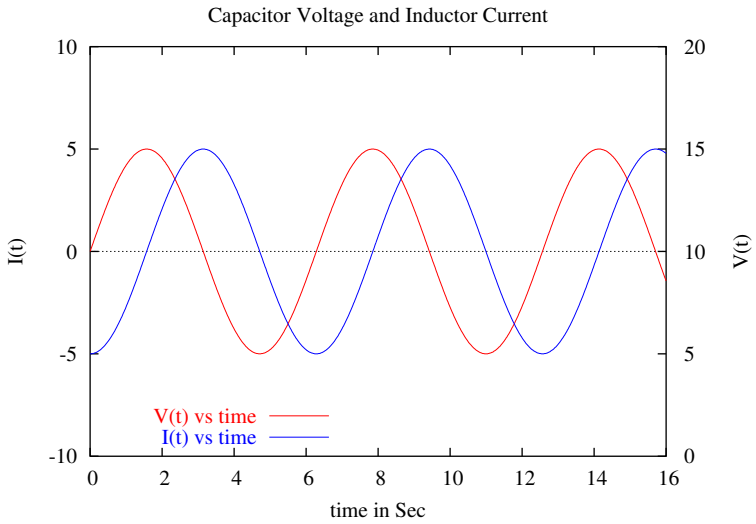

Figure E.8: The Capacitor Voltage and Inductor Current

current through the capacitor is 0. The voltage peak of the capacitor is seen to be the net capacitor current $(I_i - I(0))$ multiplied by the natural impedance $\left(Z = \sqrt{\frac{L}{C}}\right)$. The frequency of oscillation is seen to have a period of 2π $(T = 2\pi\sqrt{LC})$ seconds. It may be seen that the circuits in Figs 5 and 7 are dual of each other.

E.7 LC Circuit with Series and Shunt Excitation

Figure 9 shows an LC circuit with dual excitation. There are several possible

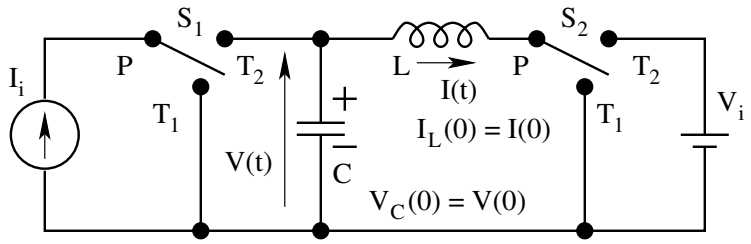

Figure E.9: An LC Circuit with Dual Excitation

transients in this circuit. Depending upon the initial position of the switches S_1 and S_2, the initial conditions also vary.

E.7.1 LC Circuit with Zero Stored Energy

Voltage Excitation

$$\left(S_1 : PT_1 \ ; \ S_2 : PT_1 \text{ at } t = 0^- \text{ to } S_1 : PT_1 \ ; \ S_2 : PT_2 \text{ at } t = 0^+ \right)$$

The initial conditions are as follows.

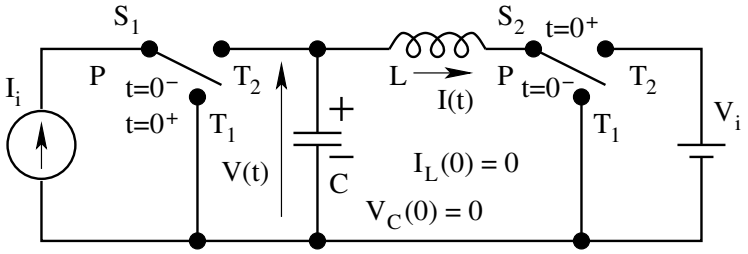

Figure E.10: LC Circuit Transient 1

$$V(0) \ = \ 0 \ ; \ I(0) \ = \ 0 \tag{E.11}$$

The inductor current and capacitor voltage are as follows.

$$I(t) \ = - \ V_i \sqrt{\frac{C}{L}} \ sin \ \frac{t}{\sqrt{LC}} \tag{E.12}$$

$$V(t) \ = \ V_i \left(1 \ - \ cos \ \frac{t}{\sqrt{LC}} \right) \tag{E.13}$$

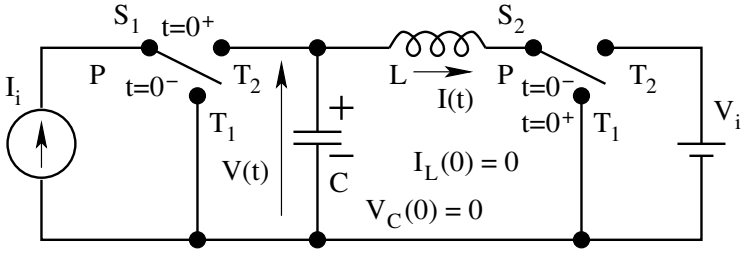

Figure E.11: LC Circuit Transient 2

Current Excitation

$$\left(S_1 : PT_1 \ ; \ S_2 : PT_1 \text{ at } t = 0^- \text{ to } S_1 : PT_2 \ ; \ S_2 : PT_1 \text{ at } t = 0^+ \right)$$

The initial conditions are as follows.

$$V(0) \ = \ 0 \ ; \ I(0) \ = \ 0 \tag{E.14}$$

The capacitor voltage and inductor current are as follows.

$$V(t) \;=\; I_i \sqrt{\frac{L}{C}}\; sin\; \frac{t}{\sqrt{LC}} \tag{E.15}$$

$$I(t) \;=\; I_i \left(1 \;-\; cos\; \frac{t}{\sqrt{LC}}\right) \tag{E.16}$$

Dual Excitation

$\left(S_1 : PT_1 \;;\; S_2 : PT_1 \text{ at } t = 0^- \text{ to } S_1 : PT_2 \;;\; S_2 : PT_2 \text{ at } t = 0^+ \right)$

The initial conditions are as follows.

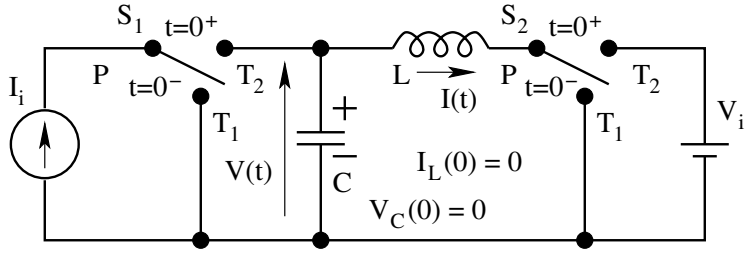

Figure E.12: LC Circuit Transient 3

$$V(0) \;=\; 0 \;;\; I(0) \;=\; 0 \tag{E.17}$$

The inductor current and capacitor voltage are as follows.

$$I(t) \;=\; I_i \left(1 \;-\; cos\; \frac{t}{\sqrt{LC}}\right) -\; V_i \sqrt{\frac{C}{L}}\; sin\; \frac{t}{\sqrt{LC}} \tag{E.18}$$

$$V(t) \;=\; V_i \left(1 \;-\; cos\; \frac{t}{\sqrt{LC}}\right) +\; I_i \sqrt{\frac{L}{C}}\; sin\; \frac{t}{\sqrt{LC}} \tag{E.19}$$

E.7.2 LC Circuit with Initial Voltage

Voltage Excitation

$\left(S_1 : PT_1 \;;\; S_2 : PT_2 \text{ at } t = 0^- \text{ to } S_1 : PT_1 \;;\; S_2 : PT_1 \text{ at } t = 0^+ \right)$

The initial conditions are as follows.

$$V(0) \;=\; V_i \;;\; I(0) \;=\; 0 \tag{E.20}$$

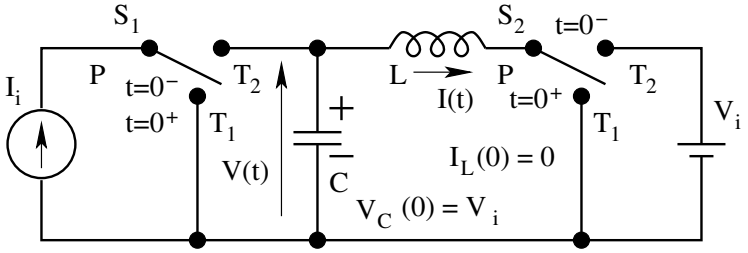

Figure E.13: LC Circuit Transient 4

The inductor current and capacitor voltage are as follows.

$$I(t) \;=\; V_i \sqrt{\frac{C}{L}}\; sin\; \frac{t}{\sqrt{LC}} \tag{E.21}$$

$$V(t) \;=\; V_i\; cos\; \frac{t}{\sqrt{LC}} \tag{E.22}$$

Current Excitation

$\left(S_1 : PT_1 \;;\; S_2 : PT_2 \text{ at } t = 0^- \text{ to } S_1 : PT_2 \;;\; S_2 : PT_2 \text{ at } t = 0^+ \right)$

The initial conditions are as follows.

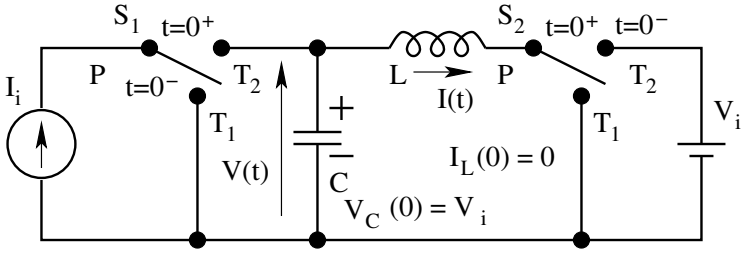

Figure E.14: LC Circuit Transient 5

$$V(0) \;=\; V_i \;;\; I(0) \;=\; 0 \tag{E.23}$$

The inductor current and capacitor voltage are as follows.

$$I(t) \;=\; I_i \left(1 \;-\; cos\; \frac{t}{\sqrt{LC}} \right) \tag{E.24}$$

$$V(t) \;=\; V_i \;+\; I_i \sqrt{\frac{L}{C}}\; sin\; \frac{t}{\sqrt{LC}} \tag{E.25}$$

Dual Excitation

$\left(S_1 : PT_1 \ ; \ S_2 : PT_2 \text{ at } t = 0^- \text{ to } S_1 : PT_2 \ ; \ S_2 : PT_1 \text{ at } t = 0^+ \right)$

The initial conditions are as follows.

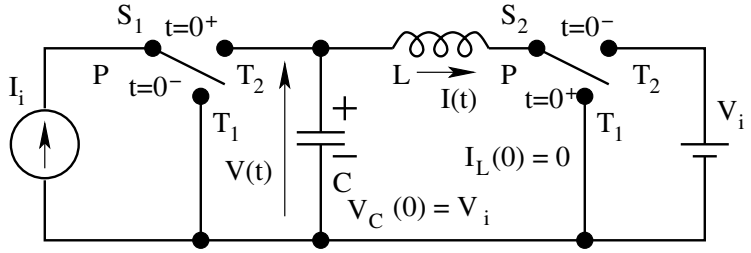

Figure E.15: LC Circuit Transient 6

$$V(0) \ = \ V_i \ ; \ I(0) \ = \ 0 \tag{E.26}$$

The inductor current and capacitor voltage are as follows.

$$I(t) \ = \ V_i \sqrt{\frac{C}{L}} \ sin \ \frac{t}{\sqrt{LC}} \ + \ I_i \left(1 \ - \ cos \ \frac{t}{\sqrt{LC}} \right) \tag{E.27}$$

$$V(t) \ = \ V_i \ cos \ \frac{t}{\sqrt{LC}} + \ I_i \sqrt{\frac{L}{C}} \ sin \ \frac{t}{\sqrt{LC}} \tag{E.28}$$

E.7.3 LC Circuit with Initial Current

Voltage Excitation

$\left(S_1 : PT_2 \ ; \ S_2 : PT_1 \text{ at } t = 0^- \text{ to } S_1 : PT_2 \ ; \ S_2 : PT_2 \text{ at } t = 0^+ \right)$

The initial conditions are as follows.

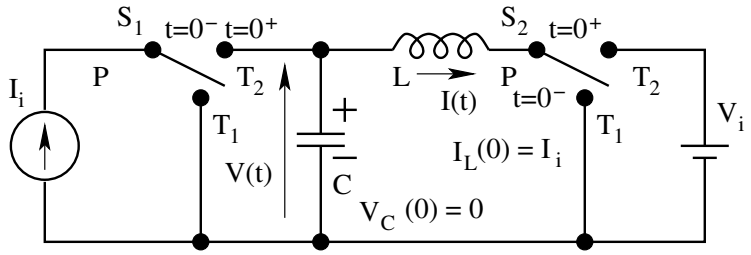

Figure E.16: LC Circuit Transient 7

$$V(0) \;=\; 0 \;;\; I(0) \;=\; I_i \tag{E.29}$$

The inductor current and capacitor voltage are as follows.

$$I(t) \;=\; I_i \;-\; V_i \sqrt{\frac{C}{L}}\; sin\; \frac{t}{\sqrt{LC}} \tag{E.30}$$

$$V(t) \;=\; V_i \;-\; V_i\; cos\; \frac{t}{\sqrt{LC}} \tag{E.31}$$

Current Excitation

$$\left(S_1 : PT_2 \;;\; S_2 : PT_1 \text{ at } t = 0^- \text{ to } S_1 : PT_1 \;;\; S_2 : PT_1 \text{ at } t = 0^+ \right)$$

The initial conditions are as follows.

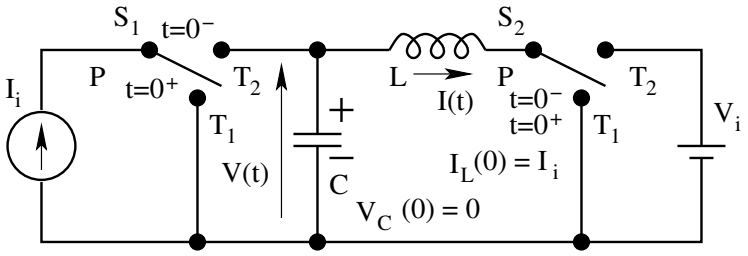

Figure E.17: LC Circuit Transient 8

$$V(0) \;=\; 0 \;;\; I(0) \;=\; I_i \tag{E.32}$$

The inductor current and capacitor voltage are as follows.

$$I(t) \;=\; I_i\; cos\; \frac{t}{\sqrt{LC}} \tag{E.33}$$

$$V(t) \;=\; -\; I_i \sqrt{\frac{L}{C}}\; sin\; \frac{t}{\sqrt{LC}} \tag{E.34}$$

Dual Excitation

$$\left(S_1 : PT_2 \;;\; S_2 : PT_1 \text{ at } t = 0^- \text{ to } S_1 : PT_1 \;;\; S_2 : PT_2 \text{ at } t = 0^+ \right)$$

The initial conditions are as follows.

$$V(0) \;=\; 0 \;;\; I(0) \;=\; I_i \tag{E.35}$$

The inductor current and capacitor voltage are as follows.

$$I(t) \;=\; -\; V_i \sqrt{\frac{C}{L}}\; sin\; \frac{t}{\sqrt{LC}} \;+\; I_i\; cos\; \frac{t}{\sqrt{LC}} \tag{E.36}$$

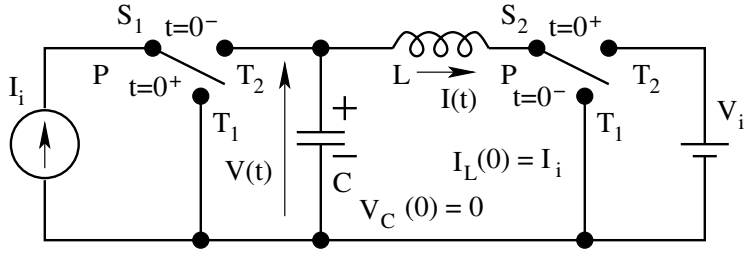

Figure E.18: LC Circuit Transient 9

$$V(t) \;=\; V_i \;-\; V_i \; cos \; \frac{t}{\sqrt{LC}} \;-\; I_i \; \sqrt{\frac{L}{C}} \; sin \; \frac{t}{\sqrt{LC}} \tag{E.37}$$

E.7.4 LC Circuit with Initial Voltage and Initial Current

Voltage Excitation

$\left(S_1 : PT_2 \; ; \; S_2 : PT_2 \text{ at } t = 0^- \text{ to } S_1 : PT_2 \; ; \; S_2 : PT_1 \text{ at } t = 0^+ \right)$

The initial conditions are as follows.

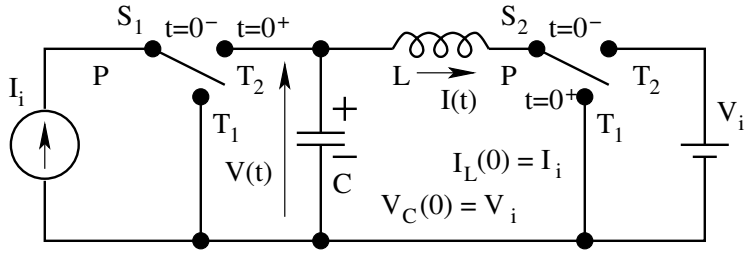

Figure E.19: LC Circuit Transient 10

$$V(0) \;=\; V_i \; ; \; I(0) \;=\; I_i \tag{E.38}$$

The inductor current and capacitor voltage are as follows.

$$I(t) \;=\; I_i \;+\; V_i \; \sqrt{\frac{C}{L}} \; sin \; \frac{t}{\sqrt{LC}} \tag{E.39}$$

$$V(t) \;=\; V_i \; cos \; \frac{t}{\sqrt{LC}} \tag{E.40}$$

Current Excitation

$\left(S_1 : PT_2 \; ; \; S_2 : PT_2 \text{ at } t = 0^- \text{ to } S_1 : PT_1 \; ; \; S_2 : PT_2 \text{ at } t = 0^+ \right)$

The initial conditions are as follows.

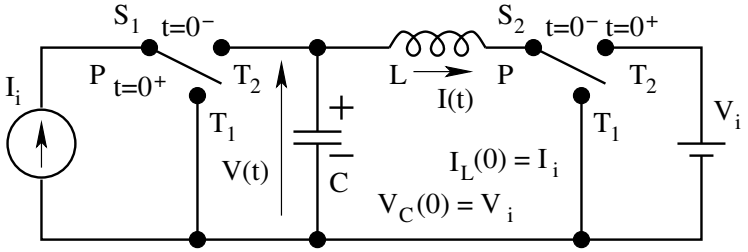

Figure E.20: LC Circuit Transient 11

$$V(0) \; = \; V_i \; ; \; I(0) \; = \; I_i \tag{E.41}$$

The inductor current and capacitor voltage are as follows.

$$I(t) \; = \; I_i \; cos \; \frac{t}{\sqrt{LC}} \tag{E.42}$$

$$V(t) \; = \; V_i \; - \; I_i \sqrt{\frac{L}{C}} \; sin \; \frac{t}{\sqrt{LC}} \tag{E.43}$$

Dual Excitation

$\left(S_1 : PT_2 \; ; \; S_2 : PT_2 \text{ at } t = 0^- \text{ to } S_1 : PT_1 \; ; \; S_2 : PT_1 \text{ at } t = 0^+ \right)$

The initial conditions are as follows.

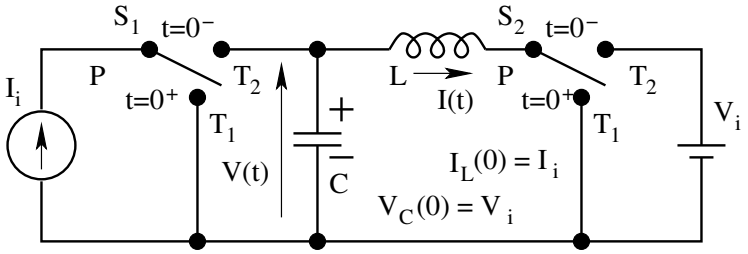

Figure E.21: LC Circuit Transient 12

$$V(0) \; = \; V_i \; ; \; I(0) \; = \; I_i \tag{E.44}$$

The inductor current and capacitor voltage are as follows.

$$I(t) \;=\; V_i \sqrt{\frac{C}{L}}\; sin\; \frac{t}{\sqrt{LC}} \;+\; I_i\; cos\; \frac{t}{\sqrt{LC}} \tag{E.45}$$

$$V(t) \;=\; V_i\; cos\; \frac{t}{\sqrt{LC}} \;-\; I_i \sqrt{\frac{L}{C}}\; sin\; \frac{t}{\sqrt{LC}} \tag{E.46}$$

Appendix F

Design Reviews

F.1 Introduction

In this section we will see the design reviews of a few sample converters taken from the application notes of device/controller manufacturers.

F.2 A 250W Off-Line Forward Converter

This refers to the design review of a 250W off-line switched mode converter (from Application Handbook 1987-88, pp 316). The design review from Unitrode is also available in the document 250WOffLine.pdf.

F.2.1 Specifications

Topology:
Two Switch forward converter with proportional drive
Input:
117 V ±15% (99 - 135 V), 60 Hz
230 V ±15% (195 - 265 V), 50 Hz
Output:
Voltage: 5 V Current: 5 – 50 A
Current Limit:
60A – Short circuit
Ripple Voltage:
100 mV – peak to peak
Line Regulation:
±1%
Load Regulation:
±1%
Others:
Efficiency: 75%
Isolation: 3750 V

Frequency: 40 kHz

The input consists of an EMI filter followed by a fullwave rectifier connected in the voltage doubler mode for 110V ac input and normal mode for 230V ac input. The rectifier is followed by a capacitive filter made up of C_1 and C_2.

F.2.2 Selection of Input Capacitors

The dc bus voltage will be the peak of the input ac voltage (because the dc bus filter is purely capacitive), with superimposed 100 Hz ripple. The criterion for the selection of the capacitor is that the ripple on the capacitor is within 15%.

$$V_{dc}(min) = 195\sqrt{2} = 276\ V$$

The maximum of average dc bus current may be evaluated from the output power, minimum dc bus voltage, and an estimate of the overall efficiency.

$$I_{dc}(max) = \frac{P_o}{V_{dc}(min)\eta} = \frac{250}{276\ x\ 0.75} = 1.21\ A$$

The capacitor has to supply this current for about a half cycle without dropping the dc bus voltage below 85%.

$$C = \frac{I_{dc}(max)(2/f)}{0.15\ x\ V_{dc}(min)} = \frac{1.2\ x\ 0.010}{0.15\ x\ 276} = 290\ \mu F$$

The design uses 2x600 μF in series, which is equivalent to 300 μF bus capacitance.

F.2.3 Power Circuit Topology

The power circuit topology used is that of a forward converter. The output power level of 250W is too high for a single switch forward converter. In the case of dissipative reset, the efficiency will be too low. In the case of a tertiary winding reset, the leakage between the primary and tertiary will result in large voltage spikes on the device. The advantage of the two switch forward converter are

1. Transformer design is simple. There is no reset winding.
2. Device voltage rating is the same as the dc bus voltage.
3. The clamp diodes completely recover the magnetising energy in the core.
4. Filter requirement is low.
5. Dynamic model is simple and closed loop control is easy.

The limitation of the circuit is that two power switches are needed with the associated drive circuits. The duty ratio is restricted to 50%.

F.2.4 Transformer turns ratio

The forward converter can not have duty ratio more than 50%, on account of the magnetising flux reset requirement. Therefore the maximun operating duty ratio (while input voltage is minimum and load is maximum) must be limited to less than 0.5.

$$V_{dc}\frac{d}{n} = V_o + V_D$$

V_{dc} = dc link voltage ; d = duty ratio ; n = turns ratio
V_o = output voltage ; V_D = freewheeling diode ON state voltage

Maximum value of d occurs when Vdc is minimum. Notice that the transistor ON drop is neglected, while the diode ON drop is not.

$$d(max) = \frac{V_o + V_D}{n\ V_{dc}} \leq 0.5$$

$d(max) = 0.5$; $V_o = 5$; $V_D = 1$; $V_{dc} = 0.85$ Vdc(min)

$$n = \frac{1}{19.55}$$

The design employs a turns ratio of 1/15.33 (6:92), so that $d(max)$ is less than 0.5 (0.39). This gives extra margin on the duty ratio to get a better dynamic range. With the selected duty ratio of 15.33, minimum duty ratio is obtained when the dc link voltage Vdc is maximum. The minimum duty ratio is

$$d(min) = \frac{V_o + V_D}{n\ V_{dc}} = 0.25$$

F.2.5 Output Inductor Selection

The output inductor L is selected to prevent discontinuous conduction at minimum load condition.

$$\delta I \leq 2\ I_{dc}(min)\ =\ 10\ A$$

$$\delta I = \frac{V_o + V_D}{L} T_S\ \leq\ 10\ A\ ;\ L\ \geq\ 11.3\mu H$$

The design uses an output inductor of 10 H.

F.2.6 Output Capacitor Selection

The output capacitor is selected based on ripple specification. The switching frequency is 40KHz. This design allows a ripple of 100 mV.

$$\frac{\delta V_o}{V_o} = \frac{(1-D)T_S^2}{8LC} \;\leq\; \frac{0.1}{5}$$
$$C \;\geq\; \frac{(1-D(min))T_S^2 V_o}{8L\delta V_o} \;=\; 295\ \mu F$$

Further ESR of the capacitor must be

$$\delta I\ R_c \;\leq\; \delta V_o\ ;\ R_c \;\leq\; \frac{\delta V_o}{\delta I_o} \;=\; 0.01\ \Omega$$

The design uses a capacitor of 600 μF with ESR less than 0.01 Ω.

F.2.7 Natural Frequencies of the Converter

From the values of the output filter elements the characteristic frequencies (the natural frequency f_o of LC and the LHP zero frequency f_a on account of the ESR of the capacitor) of the power circuit may be evaluated.

$$f_o = \frac{1}{2\pi\sqrt{LC}} \;=\; 2055Hz \;\simeq\; 2kHz\ ;\ f_a = \frac{1}{2\pi C R_c} \;\simeq\; 26kHz.$$

F.2.8 Control Transfer Function

In the modulator used in the controller IC 1524A, an input control voltage of 2.5 V, produces a duty ratio of 0.5. Therefore the modulator dc gain is 1/5. The modulator is assumed to have no dynamics (poles or zeroes). The transformer turns ratio is n. The topology used is the forward converter, which has a dc gain of Vdc/n, a complex pole pair at f_o, and a real zero at f_a. The overall control transfer function is therefore

$$G = K\frac{\left(1+\frac{s}{\omega_a}\right)}{\left(1+\frac{s}{Q\omega_o}+\frac{s^2}{\omega_o^2}\right)}$$

$\omega_a = 26\ kHz\ ;\ \omega_o = 2\ kHz\ ;\ K = V_{dc}/n$

V_{dc} ranges from $0.85 * 195\sqrt{2}$ (minimum input voltage & full load) to $265\sqrt{2}$

(maximum input voltage & light load). K therefore varies from 3.1 (9.7 dB) to 4.9 (14 dB). The control transfer function is shown on Fig. 1 for both minimum (G_{min}) & maximum (G_{max}) conditions. The dc gain is noticed to be quite low. The zero dB crossover slope is also seen to be more than 1. Therefore the compensator must have a pole-zero pair to achieve sufficient stability margins, and a PI part to achieve the desired steady state error.

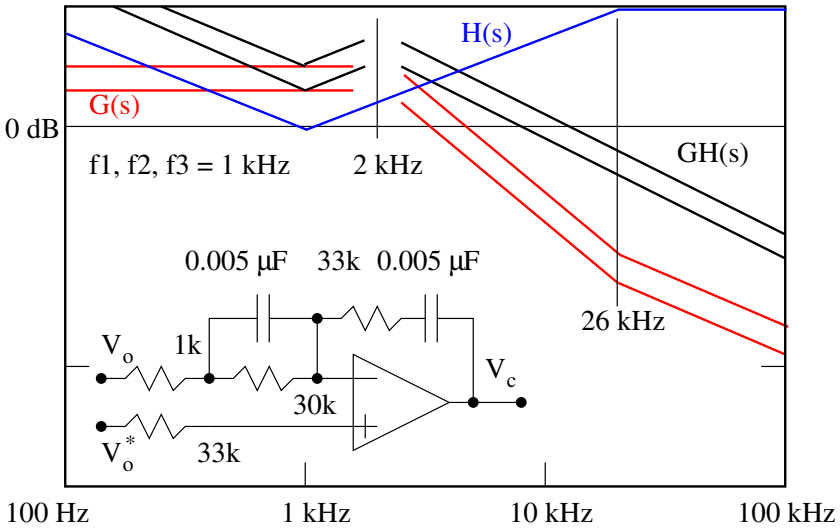

Figure F.1: Control Gain, Compensator Gain and Loopgain

F.2.9 Compensator Design

The compensator used is also shown in Fig. 1. The transfer function of the compensator is The compensator transfer function is plotted on Fig. 1. On the same plot the overall loop gain is also plotted. It is seen that the compensator design is satisfactory with a bandwidth of about 20 KHz, and a phase margin of 45. Notice that only the gain magnitude is plotted. This is because, the forward converter does not have any RHP zeros and so the phase function will be a minimal phase function. Notice also that the Q of the complex pole pair is really not important as far as the compensator design is concerned.

F.2.10 Feedback Circuit

Notice that the feedback voltage is obtained by an auxiliary dc to dc converter (Q_6 & T_3). This auxiliary converter has no inductor & so will operate in discontinuous current mode. C_6 will therefore charge to nearly V_o. Notice that the diode D_1 compensates for the voltage drop in D_2 in sensing.

F.2.11 Control Power Supply

The control power supply for the IC 1524A is obtained through a simple zener regulator (D_7), while starting and an auxiliary flyback converter (N_a & D_6) during running.

F.2.12 Switching Frequency

The switching frequency is selected by R_t & C_t (connected to pins 6 & 7 of IC 1524A).

$$f_s \simeq \frac{1.18}{R_t C_t} \simeq 80kHz$$

This corresponds to 40 kHz with half-bridge (¡ 50% duty ratio) connection.

F.2.13 Soft Start

The capacitor connected to the reference voltage (pin 16), provides soft start to a limited extent.

F.2.14 Drive circuits

The switch drive is given by Q_3. Turning off Q_3 transfers the magnetising current of N_d to the secondary N_b thereby turning on the main switches Q_4 & Q_5. Turning on Q_3 injects a spike voltage on N_d (C_5, D_3, N_d, & Q_3), which provides the necessary negative base current to turn off Q_4 & Q_5.

F.2.15 Dual Input Voltage Operation

The input diode bridge & filter capacitors are connected either as fullwave rectifier or as voltage doubler to achieve dual input voltage (220/115 V) operation.

F.2.16 Snubber Circuit

Transistor switches in general or more rugged during switch-on than during switch-off. This converter employs only turn-off snubber.

F.2.17 Current Limit

Current limit is provided by sensing the primary current (R_{10}). For the current limit threshold of 200 mV, this current corresponds to 4 Amps on the primary side. With a turns ratio of 15.33, this corresponds to about 60 Amps on the load side. The specifications of the controller IC and the schematic of 1524A is also shown separately. UC1524A.pdf.

F.3 A 500W Current Controlled Push-Pull Converter

The following is the specification of a 200 KHz, 500 W, converter (taken from Unitrode Applications Handbook, pp 234, 1987-88), operating with current programmed control. The following documents cover the converter, the controller, driver and the feedback chips employed.
Application Note:
500WPushPullConverter.pdf
Controller:
UC2842Data.pdf
Driver:
UC2706.pdf
Feedback Generator:
UC2901.pdf
Application Note:
UC2842AppNote.pdf

F.3.1 Specifications

Input Voltage:
48 ± V
Output Voltage:
5V
Output Current:
25 A to 100 A
Short Circuit Current:
120 A
Switching Frequency:
200 kHz
Line Regulation:
0.12 %
Load Regulation:
0.25 %
Efficiency:
75 %
Large Signal Slew Rate:
30 A/ms

F.3.2 Power Circuit

Input power is directly available from a dc source (40 to 56V). The power circuit used is that of a center tapped push-pull buck derived converter operating in continuous conduction. The advantage of buck derived converter is well known. The push-pull topology has the advantage of utilising simple

non-isolated drive circuits for the power devices. The disadvantage is that the push-pull converter is prone to dc saturation of the transformer. However this disadvantage can be overcome if the converter is operated in the current programmed mode. This converter employs current mode control.

F.3.3 Transformer Turns Ratio

The preferred operating duty ratio of a push-pull converter is above 2/3. We may select a maximum operating duty ratio of about 0.75.

$$V_o + V_F = \frac{d(V_{dc} - V_T)}{n}$$

V_o = Output Voltage; d = Duty ratio;

V_F, V_T : Output diode and input transistor drop;

n = transformer turns ratio;

$$n = \frac{d_{max}(V_{dc}(min) - V_T)}{(V_o + V_F)} = 4.88$$

The turns ratio chosen in the design is 5. Accordingly the maximum and minimum duty ratios are

$d_{max} = 0.77$; $d_{min} = 0.55$;

F.3.4 Transformer VA Rating

The transformer is center-tapped type. For each half

$$V_{rms}(min) = V_{dc}(min)\sqrt{d_{max}} = 40\sqrt{0.77} = 35\ V$$

$$V_{rms}(max) = V_{dc}(max)\sqrt{d_{min}} = 56\sqrt{0.55} = 42\ V$$

$$I_{rms}(max) = \frac{I_o(max)\sqrt{d_{max}}}{2n} = \frac{120}{5}\sqrt{0.385} = 14.9\ A$$

VA rating = 2 * 14.9 * 42 = 1252 A

F.3.5 Output Inductor Selection

For the current programmed converter model to be valid, the conduction parameter K $(2L/RT_s)$ has to be much higher than 1.

$$K_{min} = \frac{2L}{R_{max}T_s} = 10$$

$$R_{max} = \frac{5}{25} = 0.2\ \Omega\ ;\ T_s = 5\mu s$$
$$L = \frac{K_{min} R_{max} T_s}{2} = 5\mu H$$

The design uses a 5.8 μH inductor. The ripple current is

$$\delta I = \frac{(V_o + V_F)(1 - d_{min})T_s}{L} = \frac{6 * 0.45 * 5 * 10^{-6}}{5.8 * 10^{-6}} = 2.3\ A$$

F.3.6 Output Capacitor Selection

The ripple voltage at the output may be assumed to be equally devided between the capacitor and the ESR of the capacitor.

$$\delta V_o = \frac{\delta I T_s}{8C} + ESR\ \delta I$$
$$C = \frac{\delta I T_s}{4\delta V_o} = \frac{2.3 * 5 * 10^{-6}}{4 * 0.1} = 28.8\ \mu F$$

$$ESR = \frac{\delta V_o}{2\delta I} = \frac{0.1}{2 * 2.3} = 22\ m\Omega$$

The design uses a 20 μF capacitor with ESR of 7.5 $m\Omega$. The zero on account of the ESR will be beyond 1 MHz and can be conveniently neglected for the compensator design.

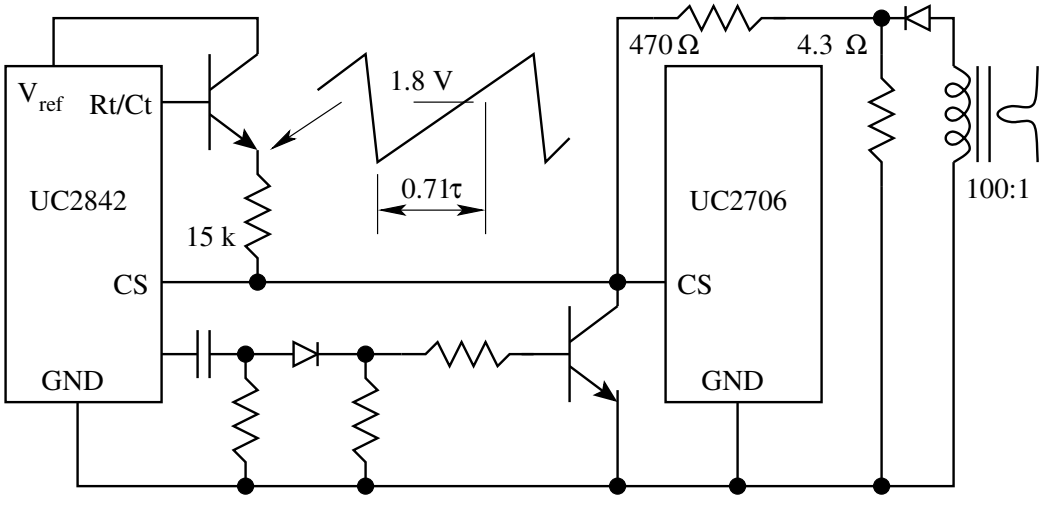

Figure F.2: Compensation Ramp

F.3.7 Compensation Ramp

The control circuit has available a ramp generated from the internal oscillator as shown in the Fig. 2. The slope of the available ramp is

$$\frac{1.8}{0.71\tau} = 0.3\ V/\mu s\ ;\ \tau = 5.6k\ *\ 0.0015\ \mu F$$

The compensation ramp desired is

$$M_2 = \frac{V_o + V_F}{L}\ R_F\ CT_{rati}\ PT_{ratio} = 0.0089\ V/\mu s$$

The desired attenuation for the compensating ramp is therefore

$$\frac{0.3}{0.0089} = 33.7$$

The design uses an attenuator (32.9) made up of 470 Ω and 15 KΩ. The control is therefore adequately compensated.

F.3.8 Closed Loop Control

The dynamic model of the converter is

$$\frac{RV_c}{R_f(1+sCR)(1+sL/R_d)}\ ;$$

$$R_f = \frac{4.3}{500}\ ;\ V_c = 3\ ;\ R = 0.2 \text{ to } 0.05$$

The dc gain varies from 18 dB to 6 dB. There is one pole at 36 KHz (R_d/L), and another pole between 40 KHz and 160 KHz. The openloop transfer function is plotted on Fig. 3. In the range of the desired bandwidth gain is flat. Therefore a simple integrator is used as a compensator. For convenience the compensating integrator is devided into two sections.

$$h_1(s) = 10.2\frac{1 + s/(2\pi 100)}{(s/2\pi 100)}\ ;\ \text{in 2901}$$

$$h_2(s) = \frac{4.55}{(1 + s/2\pi 100)}\ ;\ \text{in 2842}$$

The compensator transfer functions and the overall loopgain are also plotted on Fig. 3. The realisation of the compensator is also shown in Fig. 3. The bandwidth is seen to be in the range of 9 KHz to 36 KHz.

F.3.9 Isolated Voltage Feedback

IC 2901 is a modulator-demodulator chip used to generate isolated feedback signal with a gain of 1.

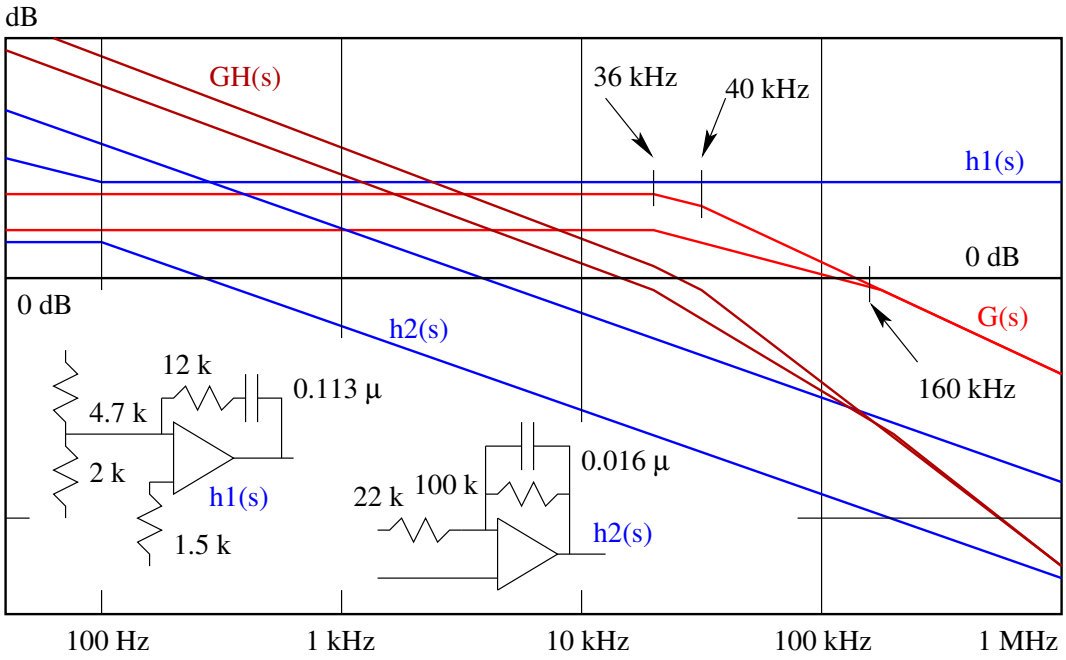

Figure F.3: Controller Performance

F.3.10 Push-Pull Drive

IC 2842 does not provide push-pull drives required for center tapped topologies. IC 2706 converts the single output of IC 2842 into push-pull outputs.

F.3.11 Leading Edge Current Blanking

The sensed current at the leading edges will exhibit sizable switching noise, which if allowed to go into the current sense circuit will lead to malfunction. Therefore the leading edges of the sensed current are blanked for a period of about 200 nanoseconds (through the 220pF, 22K, 1N914, 10K and 2N2222).

F.3.12 Output Diodes

The output diodes are shottky barrier type to limit the conduction losses.

F.4 A Multiple Output Flyback Converter in DCM

Another example of a real life converter is given in Unitrode Application Note 60WFlyback.pdf. This is a more sophisticated design using the controller IC chip UC 3840. The example is that of a 60 W flyback converter (taken from Unitrode Applications Handbook, 1987 - 88, page 383). Related datasheets are

Application Note:
60WFlyback.pdf
Controller IC:
UC3841.pdf

F.4.1 Specifications

Input Voltage:
117 V ± 15%, 60 Hz

Output Voltage:
1) 5V, ± 5%, 2.5 A to 5 A, $\delta V < 1\%$

2) 12V, ± 3%, 1 A to 2.9 A, $\delta V < 1\%$

Switching Frequency:
80 kHz

Efficiency:
70 % minimum

Isolation:
3750 V

The control IC 3841 (3840 is now obsolete) is given in UC3841.pdf. Before

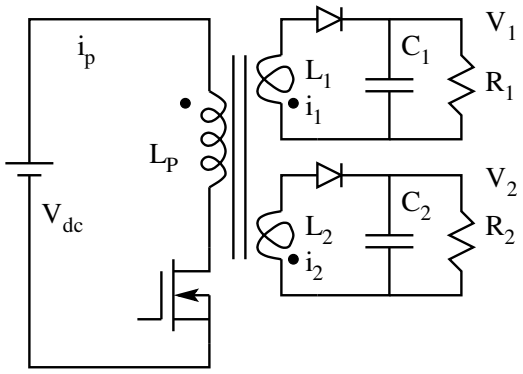

Figure F.4: Two Output Flyback Converter

we go on to study the design, let us look into the flyback topology operating in the discontinuous conduction mode (in its ideal behaviour) with multiple outputs, in order to obtain the necessary design relationships. These design relationships may be later on used to obtain a coherent design procedure. The ideal, two output, isolated, flyback converter operating in the dcm, is shown

in Fig. 4. The steady state waveforms of the converter are shown in Fig. 5.

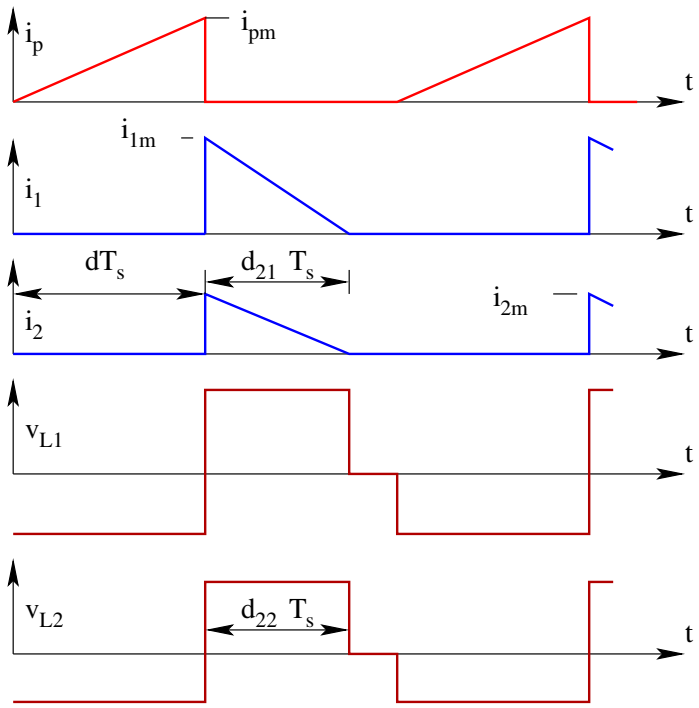

Figure F.5: Primary and Secondary Current and Voltage Waveforms

F.4.2 Diode Conduction Times d21 and d22

i_{1m} and i_{2m} are related to the intervals d_{21}, d_{22}, and the load currents by the following relationships.

$$i_{1m} = \frac{V_1 d_{21} T_s}{L_1} \qquad \frac{i_{1m} d_{21}}{2} = \frac{V_1}{R_1}$$
$$i_{2m} = \frac{V_2 d_{22} T_s}{L_2} \qquad \frac{i_{1m} d_{21}}{2} = \frac{V_1}{R_1}$$

Combining the above sets of relationship, we get

$$\frac{2V_1}{R_1 d_{21}} = \frac{V_1 d_{21} T_s}{L_1} \qquad d_{21} = \sqrt{K_1}\ ; \left(K_1 = \frac{2L_1}{R_1 T_s}\right)$$
$$\frac{2V_2}{R_2 d_{22}} = \frac{V_2 d_{22} T_s}{L_2} \qquad d_{22} = \sqrt{K_2}\ ; \left(K_2 = \frac{2L_2}{R_2 T_s}\right)$$

F.4.3 Voltage Transfer Ratios

Applying volt-sec balance on L_1, and L_2, we get

$$\frac{V_{dc} d T_s N_1}{N_p} - V_1 d_{21} T_s = 0$$
$$V_1 = \frac{d}{\sqrt{K_1}} \frac{N_1}{N_p} V_{dc}$$

$$\frac{V_{dc} d T_s N_2}{N_p} - V_2 d_{22} T_s = 0$$
$$V_2 = \frac{d}{\sqrt{K_2}} \frac{N_2}{N_p} V_{dc}$$

F.4.4 Range of Duty Ratio

$$d = \frac{\sqrt{K_1}}{V_{dc}} \frac{N_p}{N_1} V_1 = \frac{\sqrt{K_2}}{V_{dc}} \frac{N_p}{N_2} V_2$$

$$\frac{d_{max}}{d_{min}} = \frac{\sqrt{K_{1max}}}{\sqrt{K_{1min}}} \frac{V_{dcmax}}{V_{dcmin}}$$

$$\frac{d_{max}}{d_{min}} = \frac{\sqrt{K_{2max}}}{\sqrt{K_{2min}}} \frac{V_{dcmax}}{V_{dcmin}}$$

F.4.5 Condition for Discontinuous Conduction

At the boundary of ccm & dcm

$$d_2 = (1 - d)$$

For discontinuous conduction

$$d_2 < (1 - d)$$

$$d_{21} = \sqrt{K_1} < (1 - d) \; ; \; d_{22} = \sqrt{K_2} < (1 - d)$$

F.4.6 Voltage Ripple

The load is supplied by the capacitor during approximately $(1 - d_{2x})T_s$

$$\delta V_1 = \frac{(1 - d_{21}) T_s V_1}{C_1 R_1} = \frac{(1 - \sqrt{K_1}) T_s}{C_1 R_1}$$

$$\delta V_2 = \frac{(1-d_{22})T_s V_2}{C_2 R_2} = \frac{(1-\sqrt{K_2})T_s}{C_2 R_2}$$

F.4.7 ESR of the Capacitor

The voltage ripple is the sum of the above capacitor ripple and the ripple voltage on account of the ESR. The ESR ripple is $\delta I R_c$.

$$i_{1m} R_{c1} = \delta V_1 \; ; \; i_{2m} R_{c2} = \delta V_2$$

$$\frac{2R_{c1}}{R_1\sqrt{K_1}} < \frac{\delta V_1}{V_1} \; ; \; \frac{2R_{c2}}{R_2\sqrt{K_2}} < \frac{\delta V_2}{V_2}$$

F.4.8 Dynamic Model of the Converter

For the ideal flyback converter operating in the discontinuous conduction mode, without isolation, the state equations of the converter are

$$L\frac{di}{dt} = V_{dc} \; ; \; C\frac{dV}{dt} = -\frac{V}{R} \; ; \text{ during } dT_s$$

$$L\frac{di}{dt} = V \; ; \; C\frac{dV}{dt} = -i - \frac{V}{R} \; ; \text{ during } d_2 T_s$$

$$L\frac{di}{dt} = 0 \; ; \; C\frac{dV}{dt} = -\frac{V}{R} \; ; \text{ during } (1-d-d_2)T_s$$

The state equation in the usual notation are

$$A_1 = \begin{bmatrix} 0 & 0 \\ 0 & -\dfrac{1}{RC} \end{bmatrix} ; A_2 = \begin{bmatrix} 0 & \dfrac{1}{L} \\ -\dfrac{1}{C} & -\dfrac{1}{RC} \end{bmatrix} ; A_3 = \begin{bmatrix} 0 & 0 \\ 0 & -\dfrac{1}{RC} \end{bmatrix}$$

$$b_1 = \begin{bmatrix} \dfrac{1}{L} \\ 0 \end{bmatrix} ; b_2 = \begin{bmatrix} 0 \\ 0 \end{bmatrix} ; b_3 = \begin{bmatrix} 0 \\ 0 \end{bmatrix}$$

$$A = \begin{bmatrix} 0 & \dfrac{d_2}{L} \\ -\dfrac{d_2}{C} & -\dfrac{1}{RC} \end{bmatrix} ; b = \begin{bmatrix} \dfrac{d}{L} \\ 0 \end{bmatrix}$$

Steady state solution

$$X = -A^{-1}\ b\ V_{dc} = -\frac{LC}{d_2^2}\begin{bmatrix} -\frac{1}{RC} & -\frac{d_2}{L} \\ \frac{d_2}{C} & 0 \end{bmatrix}\begin{bmatrix} \frac{d}{L} \\ 0 \end{bmatrix} V_{dc}$$

$$\begin{bmatrix} I \\ V \end{bmatrix} = \begin{bmatrix} \frac{dV_{dc}}{Rd_2^2} \\ -\frac{dV_{dc}}{d_2} \end{bmatrix}$$

$$V = \frac{d}{d_2}V_{dc}\ ;\ I = \frac{d}{d_2^2}\frac{V_{dc}}{R}\ =\ -\frac{I_{dc}}{d_2}$$

The small signal model of the converter is

$$\dot{\hat{x}} = A\hat{x} + b\hat{v}_{dc} + f\hat{d} + g\hat{d}_2$$

$$f = (A_1 - A_2)X + (b_1 - b_2)V_{dc} = \begin{bmatrix} \frac{V_{dc}}{L} \\ 0 \end{bmatrix}$$

$$g = (A_2 - A_3)X + (b_2 - b_3)V_{dc} = \begin{bmatrix} 0 & \frac{V_{dc}}{L} \\ -\frac{1}{C} & 0 \end{bmatrix}\begin{bmatrix} \frac{dV_{dc}}{Rd_2^2} \\ -\frac{dV_{dc}}{d_2} \end{bmatrix}$$

The small signal model in the state space form is

$$\dot{\hat{x}} = \begin{bmatrix} 0 & \frac{D_2}{L} \\ -\frac{D_2}{C} & -\frac{1}{RC} \end{bmatrix}\hat{x} + \begin{bmatrix} \frac{D}{L} \\ 0 \end{bmatrix}\hat{v}_{dc} + \begin{bmatrix} \frac{V_{dc}}{L} \\ 0 \end{bmatrix}\hat{d} + \begin{bmatrix} -\frac{DV_{dc}}{D_2L} \\ -\frac{DV_{dc}}{RCD_2^2} \end{bmatrix}\hat{d}_2$$

From the above equation $\hat{d}_2$ may be eliminated with the help of the following relationship.

$$I_p = \frac{V_{dc}dT_s}{L} = -\frac{Vd_2T_s}{L}$$

$$\hat{d}_2 = -\frac{V_{dc}}{V}\hat{d} - \frac{D}{V}\hat{v}_{dc} - \frac{D_2}{V}\hat{v}$$

The system equation on elimination of $\hat{d}_2$, reduces to

$$\dot{\hat{x}} = \begin{bmatrix} 0 & 0 \\ -\frac{D_2}{C} & -\frac{2}{RC} \end{bmatrix} \hat{x} + \begin{bmatrix} 0 \\ -\frac{D}{D_2 RC} \end{bmatrix} \hat{v}_{dc} + \begin{bmatrix} 0 \\ -\frac{V_{dc}}{D_2 RC} \end{bmatrix} \hat{d}$$

As expected the top row is zero. In other words, the inductor current velocity is zero and has ceased to be a state of the system.

$$\dot{\hat{i}} = 0$$

$$\dot{\hat{v}} = -\frac{D_2}{C}\hat{i} - \frac{D}{D_2 RC}\hat{v}_{dc} - \frac{V_{dc}}{D_2 RC}\hat{d}$$

From the above equation $\hat{i}$ may be eliminated with the help of the following relationship.

$$I = \frac{DV_{dc}}{RK}$$

$$\hat{i} = \frac{V_{dc}}{KR}\hat{d} + \frac{D}{KR}\hat{v}_{dc}$$

Substitution for $\hat{i}$ leads to

$$\dot{\hat{v}} = -\frac{2}{RC}\hat{v} - \frac{2D}{D_2 RC}\hat{v}_{dc} - \frac{2V_{dc}}{D_2 RC}\hat{d}$$

Or, in frequency domain

$$\frac{\hat{v}(s)}{\hat{d}(s)} = -\frac{V_{dc}\sqrt{K}}{1 + s/\omega_p}$$

$K = 2L/RT_s$; $\omega_p = 2/RC$; $M = V/V_{dc}$

$$\frac{\hat{v}(s)}{\hat{v}_{dc}(s)} = -\frac{M}{1 + s/\omega_p}$$

The above results obtained for the single output flyback converter can not be applied directly for the multiple output converter. However, if we assume that the individual diode conduction times of the multiple outputs are nearly equal ($d_{21} = d_{22}$), then we may reflect all the secondaries to a common winding

and apply the above results. With the above results on the dcm operation of the flyback converter now we may study the converter.

F.4.9 Input Voltage

The maximum and minimum input voltages are

$$V_{dc}(min) = 117 * \sqrt{2} * 0.85 * 0.85 = 120\ V$$

$$V_{dc}(max) = 117 * \sqrt{2} * 1.15 = 190\ V$$

F.4.10 Input Capacitor

The ripple on the dc bus is taken to be 15% of the minimum dc voltage (21V).

$$C = \frac{I_{max} T_s}{2\delta V_{dc}} = \frac{P_o}{\eta V_{dcmin}} \frac{T_s}{2\delta V_{dc}} = 283\ \mu F$$

The design uses an input capacitor of 300 μF.

F.4.11 Variation of Conduction Parameter

$$K = \frac{2L}{RT_s}\ \alpha\ \frac{1}{R}\ \alpha\ I$$

$$\frac{K_{1min}}{K_{1max}} = \frac{I_{1min}}{I_{1max}} = \frac{1}{2}$$

$$\frac{K_{2min}}{K_{2max}} = \frac{I_{2min}}{I_{2max}} = \frac{1}{2.9}$$

F.4.12 Selection of Duty Ratio

The preferred operating duty ratio for a flyback converter is below 0.5. The maximum duty ratio used in this design is 0.45.

F.4.13 Range of Variation of Duty Ratio

$$\frac{d_{max}}{d_{min}} = \frac{\sqrt{K_{1max}}}{\sqrt{K_{1min}}} \frac{V_{dcmax}}{V_{dcmin}} = \sqrt{2} \frac{190}{120} = 2.24$$

$$\frac{d_{max}}{d_{min}} = \frac{\sqrt{K_{2max}}}{\sqrt{K_{2min}}} \frac{V_{dcmax}}{V_{dcmin}} = \sqrt{2.9} \frac{190}{120} = 2.7$$

$$d_{min} = \sqrt{2}\ \frac{0.45}{2.7} = 0.17$$

The nominal duty ratio is (0.45+0.17)/2 = 0.31

F.4.14 Selection of Primary Inductance L

$$P_{in} = \frac{P_o}{\eta} = \frac{V_{dc} I_{pm} d}{2}$$

$$I_{pmax} = \frac{2P_{omax}}{\eta V_{dcmin} d_{max}} = 3.17\ A$$

$$I_{pmin} = \frac{2P_{omin}}{\eta V_{dcmax} d_{min}} = 2.63\ A$$

$$L_p = \frac{V_{dc} d T_s}{I_{pm}} = \frac{V_{dcmin} d_{max} T_s}{I_{pmax}} = 212\ \mu H$$

$$L_p = \frac{V_{dc} d T_s}{I_{pm}} = \frac{V_{dcmax} d_{min} T_s}{I_{pmin}} = 126\ \mu H$$

This design uses an L_p of 165 μH.

F.4.15 Selection of K

The maximum duty ratio is 0.45. During transients we may allow the duty ratio to go up to 0.7. Therefore K is chosen such that dcm is obtained upto a duty ratio of 0.7.

$$K\ <\ (1-d)^2\ =\ 0.31^2\ =\ 0.096$$

$$L_1 = \frac{0.096\ R_{1min}\ T_s}{2}\ =\ 0.56\ \mu H$$

$$\frac{N_1}{N_p} = \sqrt{\frac{L_1}{L_p}} = 0.06 = \frac{1}{17.2}$$

This design uses a turns ratio of 36:2

$$L_2 = \frac{0.096\ R_{2min}\ T_s}{2}\ =\ 2.33\ \mu H$$

$$\frac{N_2}{N_p} = \sqrt{\frac{L_2}{L_p}} = 0.12 = \frac{1}{8.42}$$

This design uses a turns ratio of 36:5

F.4.16 Output Capacitors

$$\delta V_1 = \frac{1 - \sqrt{K_1}}{R_1 C_1} T_s$$

$$\delta V_2 = \frac{1 - \sqrt{K_2}}{R_2 C_2} T_s$$

$$C_1 = \frac{1 - \sqrt{K_1}}{R_1 \delta V_1} T_s = 875 \ \mu F$$

$$C_2 = \frac{1 - \sqrt{K_2}}{R_2 \delta V_2} T_s = 250 \ \mu F$$

$$R_{c1} = \frac{\delta V_1 R_1 \sqrt{K_1}}{2} = 1.5 \ m\Omega$$

$$R_{c2} = \frac{\delta V_2 R_2 \sqrt{K_2}}{2} = 5.2 \ m\Omega$$

This design uses a 10000 μF capacitor with ESR less than 2.5 mΩ for output (1). In general the ESR of the capacitor is more stringent in flyback converter. Normally the capacitance used will be an order of magnitude higher than what is calculated based on the capacitor ripple. This design uses a capacitor of 4700 μF with ESR less than 8.6 mΩ for output (2).

F.4.17 Dynamic Model of the Converter

The power circuit and the feedback circuit used in the example are shown in Fig. 6. For the purpose of sensing and auxiliary power, the converter carries an auxiliary winding W1 (of 6 turns). With the simplifying assumption mentioned earlier, the load may be reflected to the auxiliary winding. The voltage on W1 will be proportional to the number of turns (5 6/2 = 15 V). The value of the reflected load R, may be found from power balance.

$$P_o = 25 \ W \text{ to } 60 \ W \ \Rightarrow \ R_{omin} = 3.75 \ \Omega \ ; \ R_{omax} = 9.2 \ \Omega$$

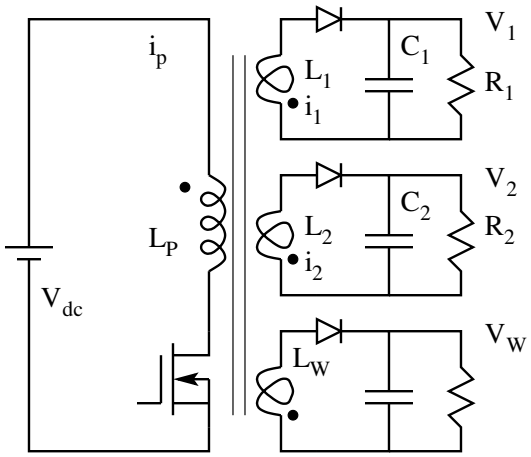

Figure F.6: Power Circuit of the Multiple Output Flyback Converter

The inductance L is proportional to the square of the turns.

$$L_W = L_p \left(\frac{6}{36}\right)^2 = 3.5\ \mu H$$

Conduction parameter may now be found out.

$$K = \frac{2L}{RT_s} \ \Rightarrow \ K_{min} = 0.06\ ;\ K_{max} = 0.15$$

The eqivalent capacitance is found by reflecting C_1 and C_2 to the auxiliary winding.

$$C = C_1 \left(\frac{2}{6}\right)^2 + C_2 \left(\frac{5}{6}\right)^2 + C_W = 4475\ \mu F$$

The single pole ω_p of the transfer function is

$$\omega_p = \frac{2}{RC} \ \Rightarrow \ \omega_{pmin} = 48.6\ rad/s \ \Rightarrow \ 7.7\ Hz$$

$$\omega_{pmax} \ = \ 119 rad/s \ \Rightarrow \ 19\ Hz$$

Converter dc gain is then found.

$$G_{dc} = \frac{V_{dc} N_w}{N_p \sqrt{K}}$$

Modulator gain is $\frac{1}{3.5}$ (for IC 3840)

$$G_{max} = 36.9 \text{ (31 dB)} \; ; \; G_{min} = 14.8 \text{ (23 dB)}$$

The overall transfer function is

$$G(s) = \frac{K}{1 + s/\omega_p}$$

$K = 23$ to 31 dB ; $\omega_p \Rightarrow 8$ to 19 Hz

The openloop bode plot of the converter is shown in Fig. 7. The gain is not a single function of s, because of the variation in load as a function of the converter parameters. Therefore the extreme values G_{min} and G_{max} are shown.

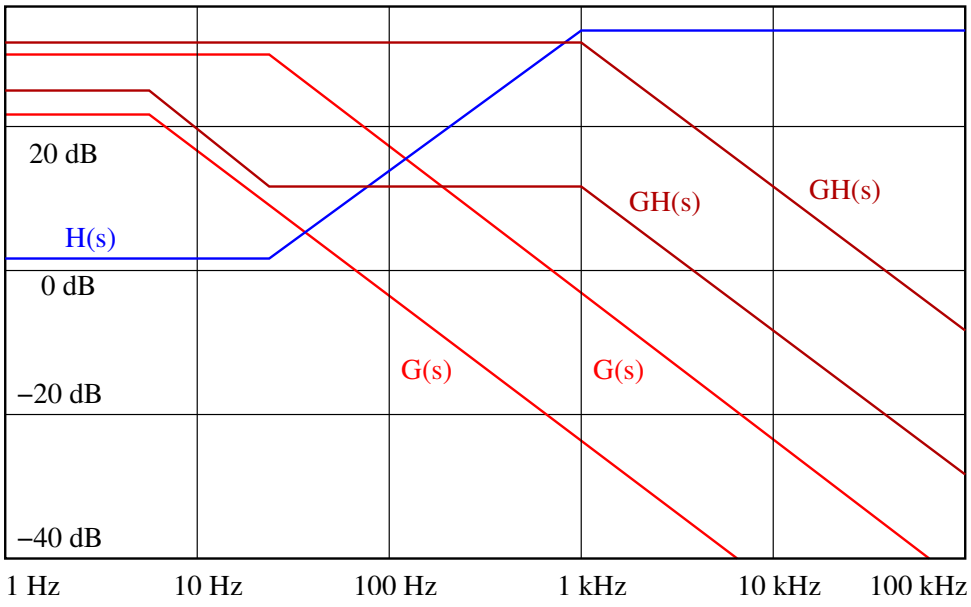

Figure F.7: Converter and Controller Gain

F.4.18 Compensator

The compensator used for this design example is shown in Fig. 8. The compensator gain and the overall loopgain are also shown in Fig. 7. The compensator transfer function is $H(s) = \frac{R_2\,(1 + s/\omega_1)}{R_1\,(1 + s/\omega_2)} = H_{dc}\frac{(1 + s/\omega_1)}{(1 + s/\omega_2)}$

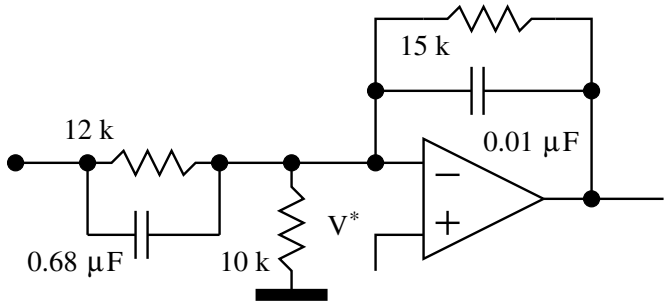

Figure F.8: Controller Circuit

$$H_{dc} = 2 \text{ dB} \; ; \; \omega_1 = \frac{1}{R_1 C_1} \; \Rightarrow 1 \text{ kHz} \; ; \; \omega_2 = \frac{1}{R_2 C_2} \; \Rightarrow 20 \text{ Hz}$$

It may be sen that the loopgain crossover frequency varies widely and is well into the region where the converter non-idealities become appreciable (ESR zero in the vicinity above 10 KHz, and Nyquist frequency namely $f_s/2 = 40$ KHz). We will see later on how these drawbacks in this design example are managed.

F.4.19 Undervoltage Lockout

The design incorporates the feature of disabling the drive circuit if the input voltage (for some reason) falls below a threshold. The same feature also inhibits the drive pulses till the input is stabilised and the capacitor C_A has charged adequately.

F.4.20 Overvoltage Lockout

Similar to the undervoltage lockout, the overvoltage lockout disables the drive if for some reason the output rises above a threshold. The undervoltage and overvoltage thresholds are set as desired by the resistive network R_4, R_5, and R_6.

F.4.21 Maximum Duty Ratio Limit

An input level to the SLS input limits the duty ratio to the desired level. The same control also serves as a slow start.

F.4.22 Frequency Setting

The operating frequency ($f_s = 1/R_t C_t$) is set by selecting R_t and C_t (in this example approximately 80 KHz).

F.4.23 Current Limit

Current is sensed by the voltage across R_{12} (0.16). When this voltage rises above the voltage set at current threshold (CT) input by 0.4 V, the current limit is effective. In this design the current limit is set to about 8 A.

F.4.24 Compensation

The compensator elements are connected to the error amplifier terminals to achieve the desired compensator transfer function.

F.4.25 Drive Circuit

The drive is a simple emitter follower driven from the output of the control IC. R_{11} is the pull-up resistor used because the output of the IC is open collector. The drive is considerably simple on account of the MOSFET switches used in the converter. Fast turn on is provided by Q_2 and fast turn off by diode D_3.

F.4.26 Feedback and Auxiliary Power

The feedback sensing and the auxiliary power to the control circuit are provided through the auxiliary winding W_1 operating in the flyback mode.

F.4.27 Feedforward Feature

While discussing the compensator design we found that the loopgain calculated varied in a wide range and was not quite satisfactory. This example incorporates a feature known as feedforward to improve the loopgain characteristics. The dc gain of the flyback converter was seen to be

$$G_{dc} = \frac{V_{dc}}{\sqrt{K}} \frac{N_W}{N_p} \frac{1}{V_s}$$

where $(1/V_s)$ is the modulator gain. Or V_s is the peak of the comparison

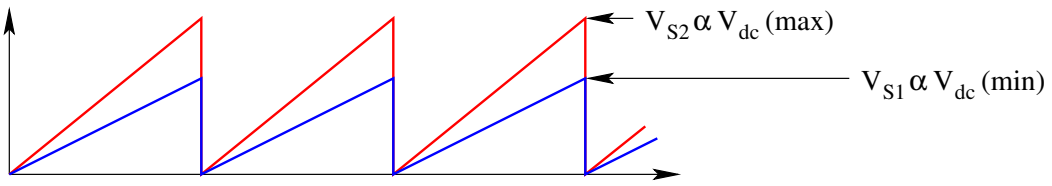

Figure F.9: Feed Forward Feature

ramp. If V_s is made proportional to V_{dc}, then the variation of dc gain of the converter on account of variation of the input voltage V_{dc} can be completely

nullified. Then the variation of dc gain will be on account of only the conduction parameter K, which is quite small. Earlier we took V_s to be 3.5 and V_{dc} in the range of 120 to 190 V. In this example V_s is nominally 3.5 and varies in proportion to V_{dc}. This feature is shown in Fig. 9. As a result the gain is

$$G_{dc} = \frac{V_{dc}(nominal)}{\sqrt{K}} \frac{N_W}{N_p} \frac{1}{V_s(nominal)} = \frac{6.9}{\sqrt{K}}$$

$G_{dc}(max) = 29$ dB ; $G_{dc}(min) = 25$ dB

G_{max} occurs for R_{max}, and corresponds to ω_{pmin}. Similarly G_{min} occurs for R_{min}, and corresponds to ω_{pmax}. With these recalculated G_{max} and G_{min}, the overall loopgain is shown in Fig. 10. The range of variation in loopgain crossover frequency is seen to be verymuch improved (6 KHz to 15 KHz). Another point to observe is that the duty ratio limit is also now fed from V_{dc}.

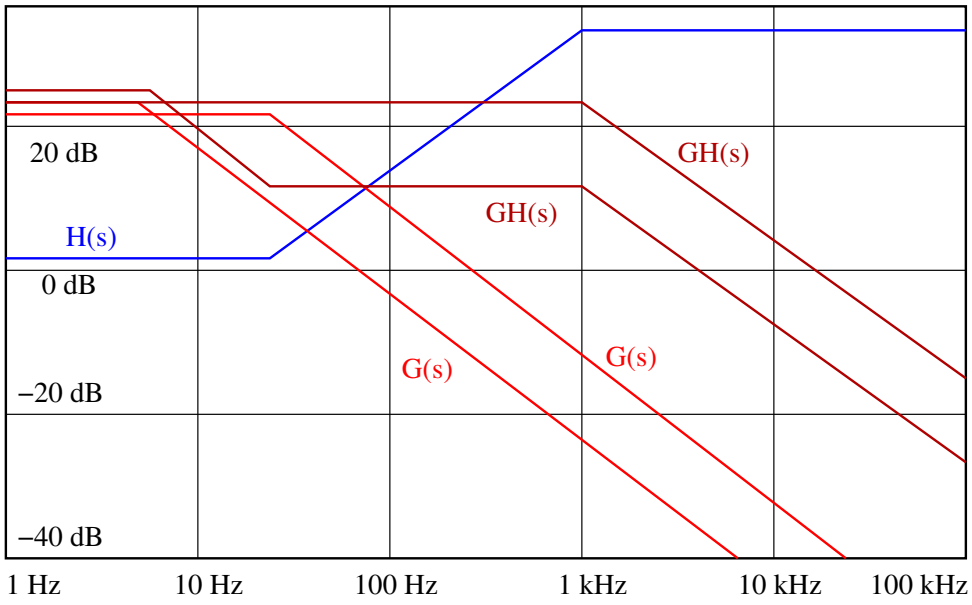

Figure F.10: Loopgain with Feedforward Feature

F.4.28 Snubber Circuit

Converters operating in dcm do not need turn-on snubbers. The turn-off snubber is made of D_4, R_{14}, and C_3. For converters operating in dcm, the reverse recovery times of the freewheeling diodes are not critical.

F.4.29 Output Diodes

For good efficiency, the low voltage high current output uses a shottky diode which has low forward voltage drop.

F.5 Problem Set

1. For the converter reviewed in Example 1, if the power rating is changed to 150W at 5V, what power circuit components will require redesign?. Make a suitable design of the power circuit components and the compensator.
2. For the converter reviewed in Example 2, if the compensating ramp addition circuit resistor 470 is changed to 150, evaluate the range of duty ratio for which the converter will be stable?
3. In the converter in Example 2, if the snubber resistor R_{14} is dissipating 1 W, make an estimate of the leakage inductance of the primary winding.

Appendix G

Construction Projects

G.1 Introduction

It is noticed that the curriculum in most subjects are currently moving away from laboratory based instruction. The laboratory sessions when stated, invariably are based on canned software loaded on PCs and almost totally divorced from the theoretical basis of the subject. Hardware laboratory sessions are missing and the students miss the most exciting and durable mode of learning. Most universities now teach an elective course on switched mode power conversion (SMPC). However, the students rarely learn the skills of assembling circuits, testing and debugging the same, and eventually designing application circuits. Most students have not had an opportunity to use independently simple instruments such as signal generators and multimeters; nor have they acquired prototyping skills such as breadboards, printed circuit boards, soldering etc. As a result most students feel diffident about the subject and stay away from a career in engineering industry.

The purpose of this section is to present short construction projects which will enable the student to learn the skills of fabrication, testing and debugging skills and eventually design skills. The objective is to make these projects as part of the SMPC curriculum. The resource base needed may not be more than a the soldering iron for assembling the circuit; a laboratory power supply & a multimeter for testing the same, a signal generator & a general purpose oscilloscope (CRO) for debugging the same. Each project may not take more than one session of 3 hours. The execution of the construction work may not take more than about Rs. 150/= worth of components.

G.1.1 Example Circuits

The following are the circuits available for the student to build and learn from the construction projects.

1. Constant Current Load.

2. Constant Voltge Current Limited Power Supply.
3. Constant Voltage Constant Current Linear Power Supply.
4. Non-isolated Boost Converter.

The project is covered with adequate operating theory and design background to the student. The materials required for the project are given to each student in a kit form. The kit consists of the printed circuit board on which the circuit will be assembled along with all the components needed. The components cover the active and passive components, control ICs, magnetic components (inductors and transformers), and heatsinks. The first exercise for the student is to obtain independently through the net the data sheets of all the critical components such as the power devices, ICs, etc. A class room session presents the basis of the design briefly (This is optional since the purpose of the laboratory session is mainly to impart the construction, testing and debugging skills).

G.2 More Details

The circuits, components etc are given in the following link.

ConstructionProjects
The circuits, components etc are given in the following link.

Assembly Instructions

Kit Vendors

The following vendor has the construction project kits available in ready to assemble kit as well as fully assembled boards.

New Tech Systems,
Attention: Mr. Jayaram Raju,
No. 1774, 3rd Stage,
Prakash Nagar,
Bangalore 560021
Phone: 080 2342 2263
Fax: 080 2292 3970
email: newtechjayram@gmail.com , newtechjayram@yahoo.co.in

Appendix H

Simulation of Power Converters

H.1 Introduction

This section points to several programmes covering circuit simulation of power switching devices, power converters, drives etc. There are several circuit simulation software such as PSPICE, SABER, etc which are commercially available. This section presents the application of an open source circuit simulation software developed by Prof. M.B. Patil of IIT Mumbai. The same is available from the website of IIT Mumbai.

Sequel also can be extended by the user by developing suitable device libraries. The accompanying document also demonstrates many of these features.

H.2 More Details

The application programmes covering several features of the Software Sequel are given in the following document link.

Sequel Simulation Examples

Kit Vendors

The following vendor has the construction project kits available in ready to assemble kit as well as fully assembled boards.
Hardware Kits
New Tech Systems,
Attention: Mr. Jayaram Raju,
No. 1774, 3rd Stage,
Prakash Nagar,
Bangalore 560021
Phone: 080 2342 2263

Fax: 080 2292 3970
email: newtechjayram@gmail.com , newtechjayram@yahoo.co.in

Appendix I

Theses

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   Utilisation of Three Phase Self-Excited Induction Generator for Microhydel Power Plants

2. **Venkatesha L., Ph.D., June 1999**
   Determination of Flux-Linkage Characteristics and Torque Ripple Minimisation with Pre-Computed Currents in Switched Reluctance Motor
   Venkatesha

3. **Debiprasad Panda, Ph.D., August 1999**
   Control Strategies for Sensorless and Low-Noise Operation of Switched Reluctance Motor
   Panda

4. **Gurumurthy S. R., M.Sc (Engg), January 2006**
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I.2 Power Quality

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   Analysis and Synthesis of Hybrid Active Filter for Harmonic Compensation

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   Parthasarathi Sensarma

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1. **Ramanarayanan V., Ph.D., May 1986**
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   Ramanarayanan V

2. **Souvik Chattopadhyay, M.Sc (Engg), December 1990**
   A Personal Computer based Analysis and Evaluation System for Switched Mode Power Converters

3. **Kamalesh Chatterjee, M.Sc (Engg), November 1991**
   Design of Induction Heater

4. **Rajapandian A., M.Sc (Engg), August 1995**
   A Constant Frequency Resonant Transtion Converter
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5. **Sanjay Lakshmi Narayanan, M.Sc (Engg), November 1995**
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6. **Giridharan S., M.Sc (Engg), September 1996**
   A Novel Transformer-less Uninterruptible Power Supply
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7. **Biju S. Nathan, M.Sc (Engg), December 1999**
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   Biju

8. **Souvik Chattopadhyay, Ph.D., April 2002**
   Carrier Control Methods for Resistor Emulator Rectifiers and Impedance Emulator Shunt Active Filter
   Souvik Chattopadhyay

9. **Hariharan K., M.Sc (Engg), April 2002**
   High Frequency AC Link Transformer
   Hariharan

10. **Rajaganesh K., M.Sc (Engg), April 2003**
    Design of Efficient Low Voltage High Current DC to DC Power Supply
    Rajaganesh

11. **Vishwanathan N., Ph.D., February 2004**
    DC to DC Converter Topologies for High Voltage Power Supplies Under Pulsed Loading
    Vishwanathan

12. **Swaminathan B., M.Sc (Engg), May 2004**
    Resonant Transition Topologies for Push-Pull and Half-Bridge DC-DC Converters
    Swaminathan

13. **Vishal Anand A. G., M.Sc (Engg), June 2005**
    Single Phase and Three Phase Power Factor Correction Techniques Using Scalar Control
    Vishal

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    Design of 1400 W Telecom Power Supply with Wide Range Input AC Voltage
    Daiva Prakash

15. **Lakshminarasamma N., Ph.D., June 2007**
    A New Family of Soft Transition DC-DC Converters
    Lakshmi

16. **Rahmatollah Mirzaei, Ph.D., June 2007**
    Soft Switched Multi-Phase Tapped Boost Converter and its Control
    Mirzaei

I.4 Electromagnetics

1. **Ramanamurthy G. S., M.Sc (Engg), March 1999**
   Design of Transformers and Inductors at Power Frequency - A Modified Area-Product Method

2. **Milind, M.Sc (Engg), March 2005**
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   Milind

Appendix J

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   jiisc1992.pdf

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   jiisc1996.pdf

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   jiisc20001.pdf

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India, pp 146-151
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Appendix K

A Sample Innovation

This section gives a sample innovation written in the structure of a patent filing. The sample innovation pertains to a family of zero voltage transition (ZVT) dc to dc converters. This invention pertains to the field of Electrical Technology. In general this invention relates to power supplies for Electric devices and appliances. In particular this invention relates to efficient turn-on and turn-off of power semiconductor switches in power supplies and converters. Several new circuit topologies are proposed incorporating this invention.

The present trend in switched mode power supplies (SMPS) is to switch at high switching frequencies to meet the increasing demands on high power density. Switching frequencies in excess of 500 kHz are becoming standard.

K.1 Circuit Operation

Figure 1 shows the basic switching element common to switching power converter. The throw voltage (V_T), and the pole current (I_P) are defined. The active switch is S. The passive switch is D. The switch voltage V_S and switch current I_S are designated as shown in Fig. 1. In such a converter, the active switch is turned on and off with finite duty ratio d. The duty ratio is defined as

$$d \;=\; \frac{T_{on}}{T_{on} + T_{off}} \tag{K.1}$$

K.2 Hard Switching Waveforms

Figure 2 shows the typical switching waveforms of the switch current I_S and the switch voltage V_S under steady state. The critical switching times are the fall time (t_f) and rise time (t_r) as shown in Figure 2. Figure 3 shows the trajectory of the operating point of the switch in the v-i plane. Every turn-on and turn-off process transits through the high dissipation point of (V_T, I_P).

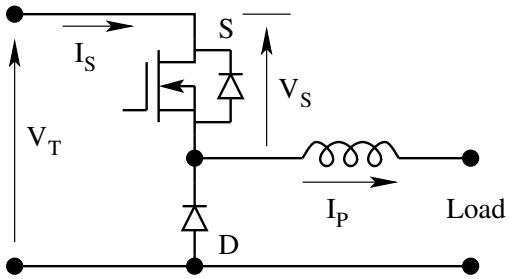

Figure K.1: A Typical Switching Pole in a Power Converter

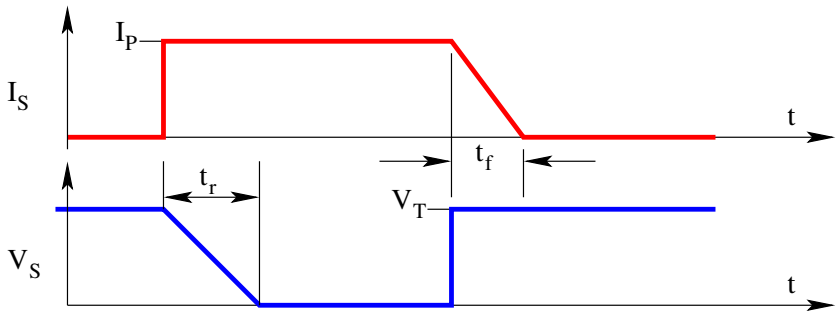

Figure K.2: Typical Hard Switching Waveforms

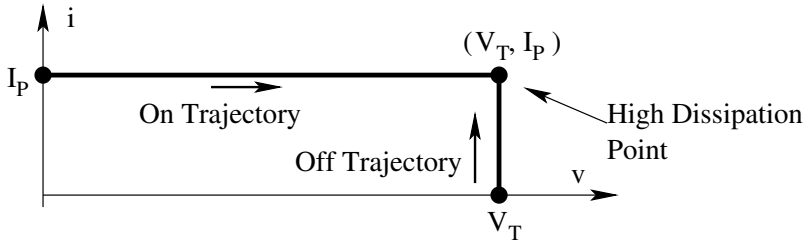

Figure K.3: Trajectory of the Switch Operating Point in v-i Plane

This results in high switching losses which are proportional to the switching frequency.

A number of circuit topologies and control strategies have been developed in the past two decades addressing this problem of switching losses. These methods go under the general name of Zero Voltage Switching (ZVS) and/or Zero Current Switching (ZCS) circuits. They are also referred to as soft switching techniques. Soft switching techniques become absolutely essential in order to operate at switching frequencies beyond about 200 kHz.

Currently there are several families of such soft switching power converters.

These are classified as follows. Some of their respective salient features are also listed here.

1. Resonant Load Power Converters
    - This family of power converters employs soft-switching and provide loss-less switching.
    - Consequently high switching frequencies are achievable.
    - The control in these converters is by variable switching frequency.
    - The performance is load dependent.
    - The (VA) rating of reactive components is much higher than the delivered power (W).
2. Resonant Switch Power Converters.
    - This family of power converters employs soft-switching and provide loss-less switching.
    - High switching frequencies are achievable.
    - The control is by variable switching frequency.
    - The performance is load dependent.
    - The (VA) rating of switches is much higher than the source voltage and load current.
    - The circuit has high additional component count.
3. Resonant Transition Converters.
    - This family of power converters employs soft-switching and provide loss-less switching.
    - High switching frequencies are achievable.
    - The control is at constant switching frequency.
    - The (VA) rating of switches is the same as the source voltage and load current.
    - The performance is load dependent.
4. Resonant Pole Zero Voltage Switching Converters.
    - This family of power converters employs soft-switching and provide loss-less switching.
    - High switching frequencies are achievable.
    - The control is at constant switching frequency.
    - The (VA) rating of switches is the same as the source voltage and load current.

- The performance is load dependent.
- The circuit is suitable for bridge circuits only

5. Active Clamp Zero Voltage Switching Converters.

   - This family of power converters employs soft-switching and provide loss-less switching.
   - High switching frequencies are achievable.
   - The control is at constant switching frequency.
   - The (VA) rating of switches is the same as the source voltage and load current.
   - The performance is load dependent.
   - The circuit has high additional component count.

The constraints of some of these converters are

- Variable switching frequency.
- High VA rating of reactive components.
- High Component count.
- Load dendendent zero voltage switching performance.
- Complex circuit models.
- Additional design constraints on account of the above features.
- Limited number of application circuits.

The present invention addresses the above constraints and proposes a circuit topology suitable for all switching power converters.

K.3 Principle of Operation

The present invention introduces an auxiliary circuit connected in parallel to the active switch. The auxiliary circuit when switched properly ensures ZVS of the active switch. The auxiliary circuit consists of an auxiliary switch S_a, a series diode D_a, a dependent voltage source V_a and a set of resonant elements L_a and C_a. The circuit is shown in Fig. 4. The auxiliary switch is turned on at a time prior to the turn-on of the active switch S. In other words, when the active switch S is to be turned on while the passive switch D is conducting, the auxiliary switch S_a is first turned on. After a brief delay of T_D, the active switch S is turned on. The gating signals to S_a and S are shown in Figure 5.

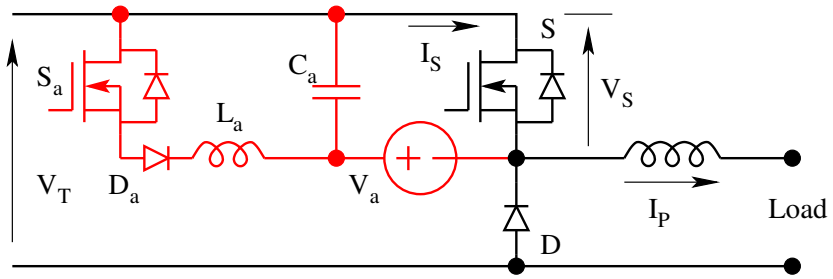

Figure K.4: Auxiliary Circuit to Achieve ZVS of the Active Switch

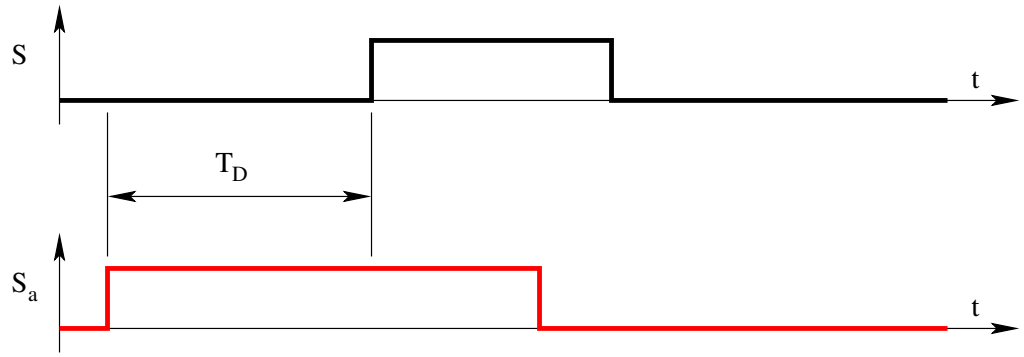

Figure K.5: The Gating Signals to S and S_a

K.4 Circuit Analysis and Waveforms

Consider the dependent source V_a to be zero. The current in the auxiliary switch will be given by the following equation immediately after turn-on of S_a.

$$i_{Sa} = \frac{V_T}{L_a} \tag{K.2}$$

At the end of time T_1, when i_{Sa} reaches I_P, the passive switch D will turn-off.

$$T_1 = \frac{I_P L_a}{V_T} \tag{K.3}$$

Following this interval T_1, the equivalent circuit is as shown in Fig. 6. During this interval, the circuit resonates and the resonant inductor current and the resonant capacitor voltage are as follows.

$$i_{La} = I_P + V_T\sqrt{\frac{C_a}{L_a}}\, Sin\ (\omega\ t) \tag{K.4}$$

$$v_{Ca} = V_T\ Cos\ (\omega\ t) \tag{K.5}$$

$$\omega = \frac{1}{\sqrt{L_a C_a}} \tag{K.6}$$

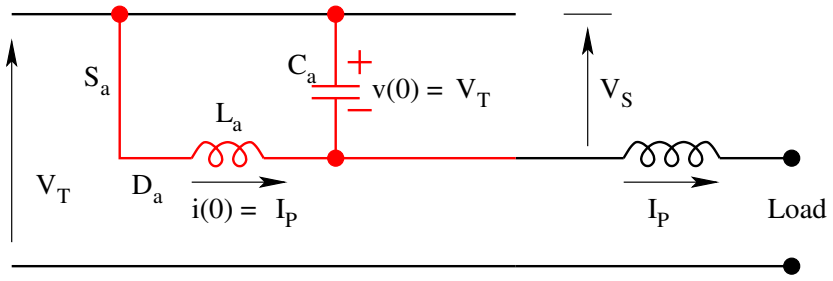

Figure K.6: Equivalent Circuit Following Turn-off of Passive switch D

The resonant process ends at the end of this interval T_2, when the resonant capacitor voltage reaches zero causing the body diode of the active switch S to become on. The interval T_2 is given by

$$T_2 = \frac{\pi}{2}\sqrt{L_a C_a} \tag{K.7}$$

The equivalent circuit and the circuit waveforms in intervals T_1, T_2 and thereafter are shown in Fig. 7. It may be noticed that the body diode of S has

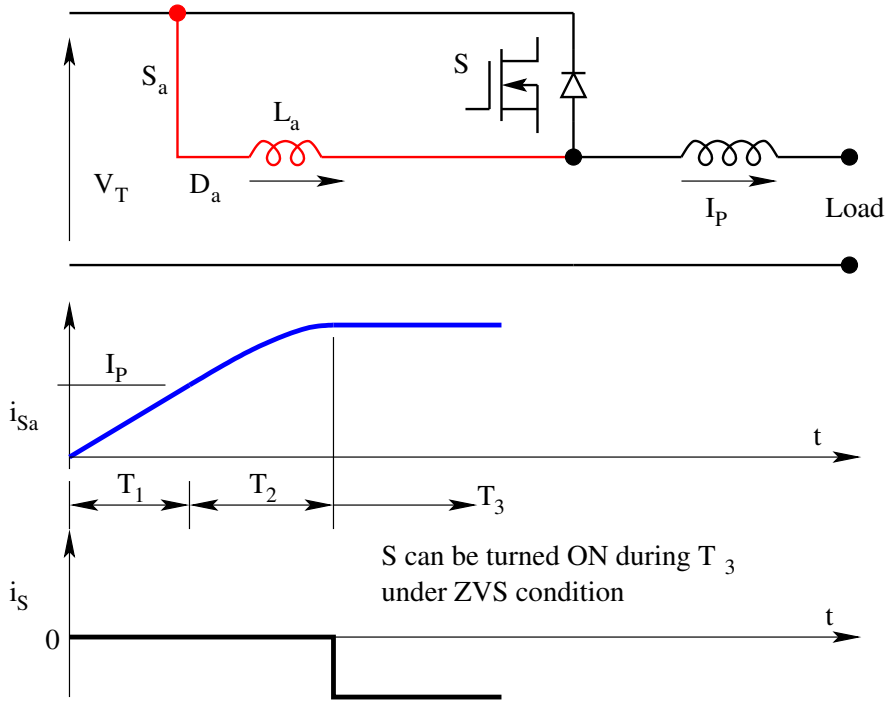

Figure K.7: ZVS Turn-on Process of the Active Switch S

started conducting after T_2. Therefore S may be turned on under ZVS without loss following T_2. However, the turn-off of S_a under this condition will be

hard with switching overvoltage on S_a on account of the current in L_a being interrupted. This is not desirable.

The Current Invention of ZVS for S and ZCS for S_a

We now explain the innovation covered by this document covering the invention of loss-less switching for both the active switch as well as the auxiliary switch.

Consider now the auxiliary circuit with the dependent source V_a a suitable negative value. The equivalent circuit under this constraint is shown in Fig. 8. Under this constraint, it may be shown that the intervals T_1 and T_2 will be

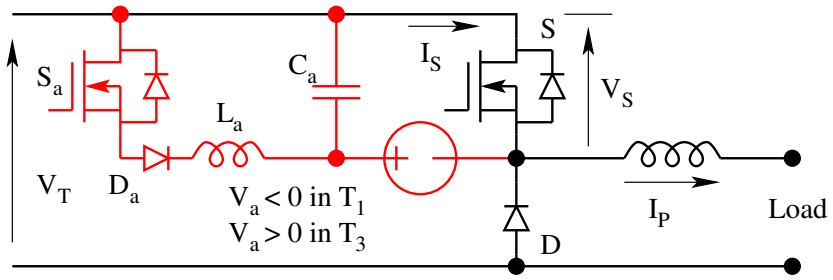

Figure K.8: Auxiliary Circuit with ($V_a < 0$)

as follows.
Interval 1:

$$i_{Sa}(t) = \frac{(V_T + V_a)}{L_a} \tag{K.8}$$

End of interval T_1 is when $i_{Sa} = I_P$

$$T_1 = \frac{I_P L_a}{V_T + V_a} \tag{K.9}$$

Interval 2:

$$i_{Sa}(t) = I_P + (V_T + V_a)\sqrt{\frac{C_R}{L_R}}\, Sin(\omega t) \tag{K.10}$$

$$v_{Ca}(t) = (V_T + V_a)\; Cos(\omega t) \tag{K.11}$$

$$\omega = \frac{1}{\sqrt{L_a C_a}} \tag{K.12}$$

End of interval T_2 is when $v_{Ca} = V_a$

$$\omega T_2 = Cos^{-1} - \frac{V_a}{V_T + V_a} \tag{K.13}$$

The valid solution for ωT_2 is from the second quadrant. The qualitative change in introducing the dependent voltage in the auxiliary circuit occurs following

the interval T_2. The trapped energy in the auxiliary circuit inductor is recovered into the auxiliary source V_a. The complete commutation process is shown in Figure 9 through the waveforms. With this auxiliary circuit, the turn-on

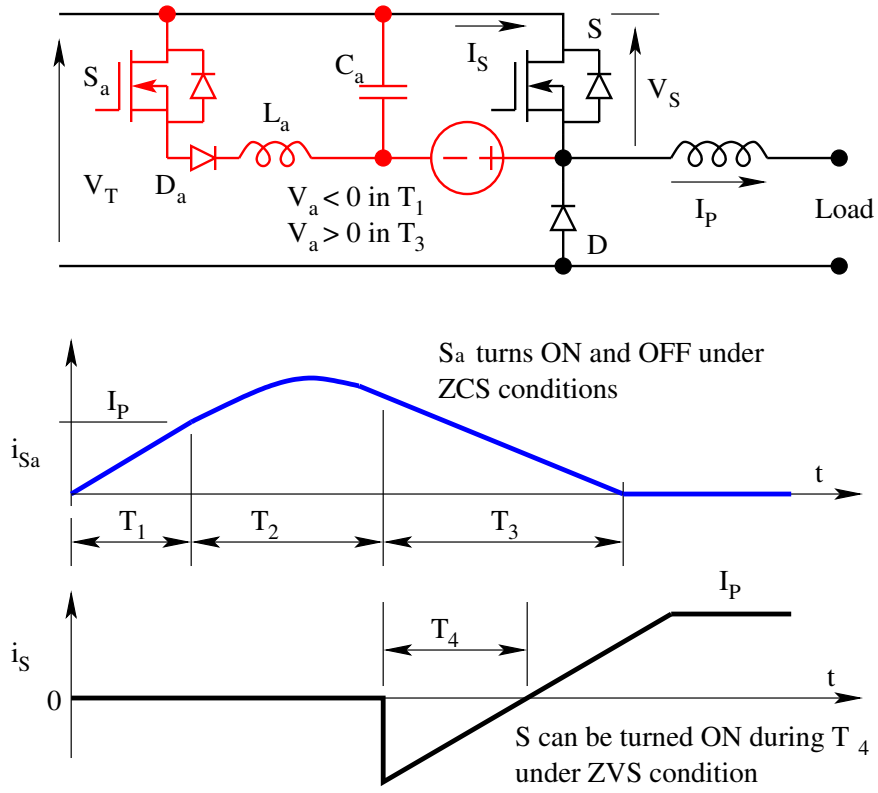

Figure K.9: ZVS Turn-on Process of the Active Switch S

process of the main switch S is at zero voltage. The turn-on and turn-off process of the auxiliary switch S_a is under zero current. The turn-off process of the main switch S is zero voltage (on account of the capacitor across the switch during turn-off). In effect all the transitions are loss-less.

K.5 Circuit Realisation of the Concept

It is necessary to obtain a dependent source V_a whose magnitude is less than zero during the turn-off of the passive switch D (Interval T_1) and positive during the reset of the auxiliary switch S_a (Interval T_2). The magnitude of V_a could be same or different during the intervals T_1 and T_3. It is essential that the polarity of V_a be appropriate in both these intervals. The innovation claimed by this invention is on the method of generating this dependent voltage. Figure 10 shows the primitive auxiliary circuit highlighting this method. The auxiliary voltage is obtained by a tapped winding coupled to the inductor.

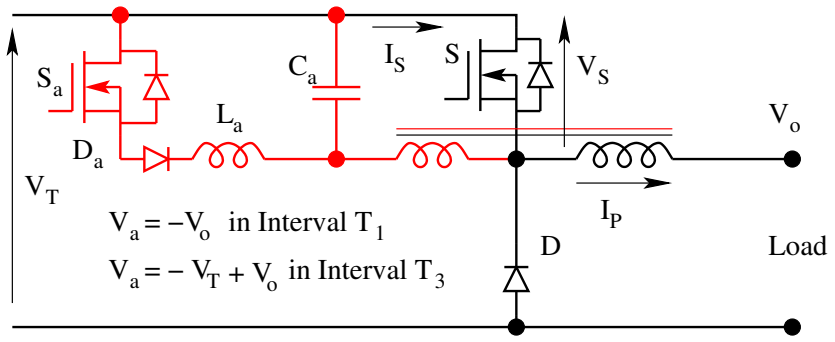

Figure K.10: The Primitive Auxiliary Switch Commutation Circuit

The turns ratio may be chosen conveniently. In the following exposition, it is taken as 1. This winding has to carry the commutation current and reset current only. Therefore the rms current rating of this coupled winding will be a small fraction of the current flowing in the main inductor L. Accordingly, this will not demand a higher size of inductor for the purpose. In the primitive circuit shown, the dependent voltage V_a is different in the intervals T_1 and T_3 as shown in Fig. 10. The complete commutation process is shown in Fig. 11. The advantages of the claimed ZVS circuits are as follows.

1. The method is applicable to all hard switching converter, isolated and non-isolated.
2. The switching frequency is constant.
3. The voltage and current ratings are the same as their hard switching counterparts.
4. The performance is independent of load.
5. The dynamic model of the converters are almost the same as their hard switching counterparts.
6. The mathematical analysis of the steady-state and dynamic performance is very simple and the results are identical in all types of power converters.

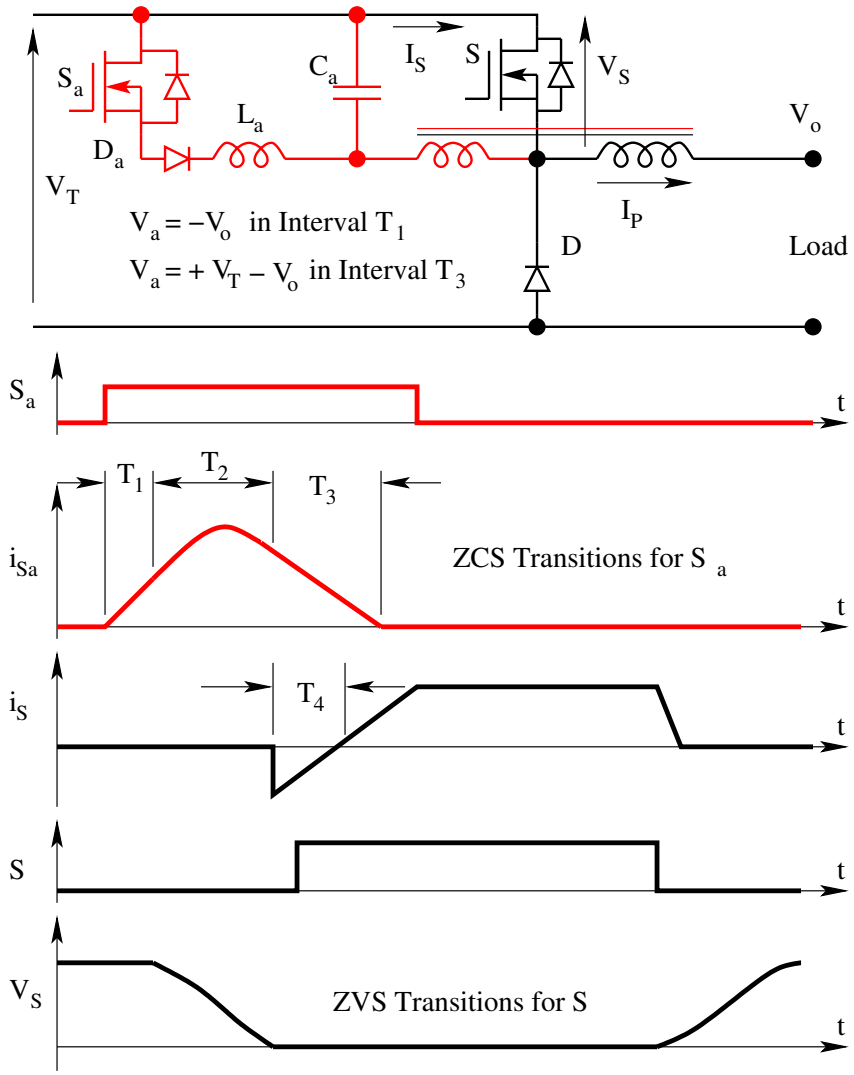

Figure K.11: The ZVS and ZCS Transitions in the Auxiliary Switch Circuit

K.6 Application to other circuits

The following are the different circuits on which the addition of auxiliary switch commutation is shown.

1. Buck Converter:

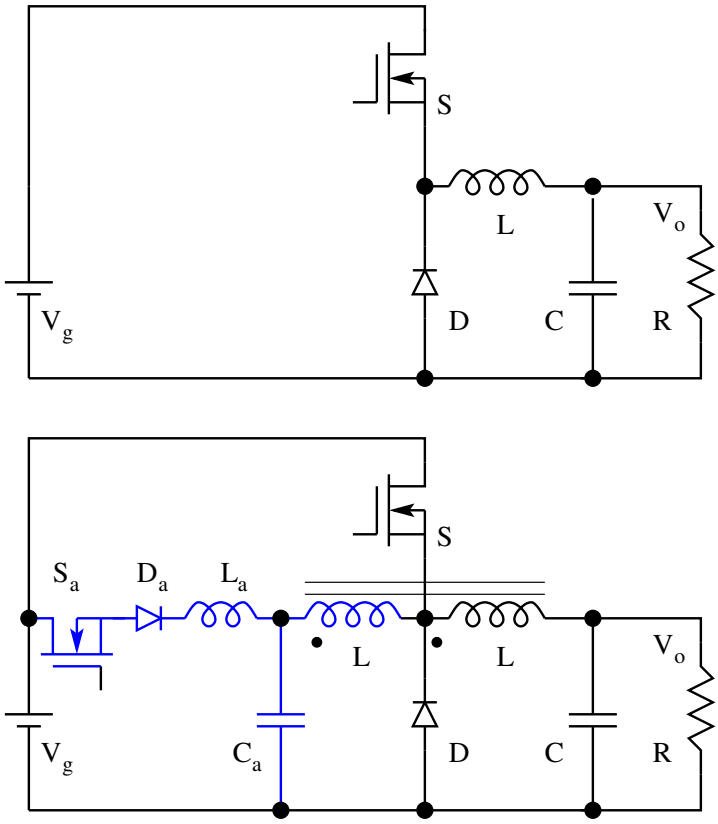

Figure K.12: Buck Converter and its ZVS Variant

2. Boost Converter

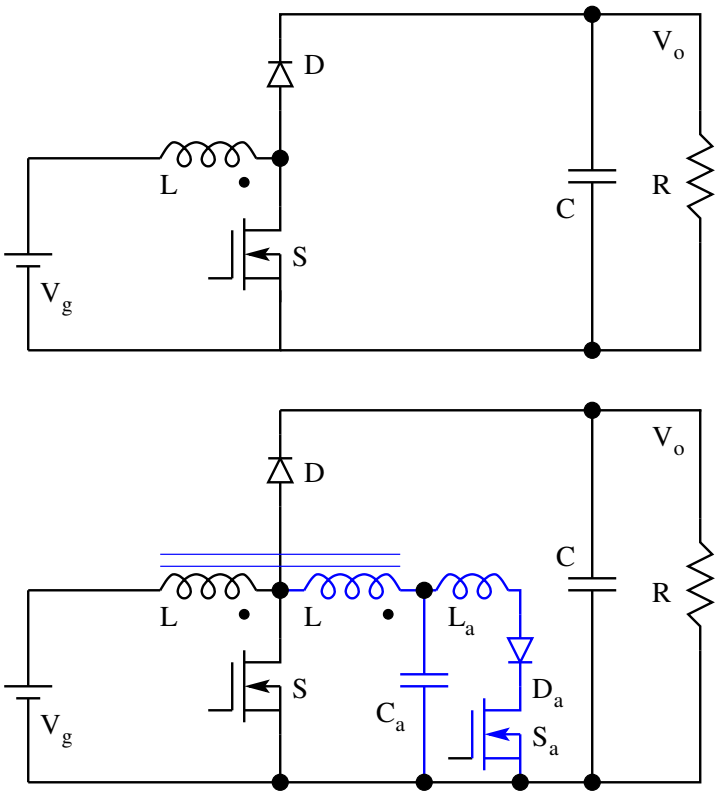

Figure K.13: Boost Converter and its ZVS Variant

3. Flyback Converter

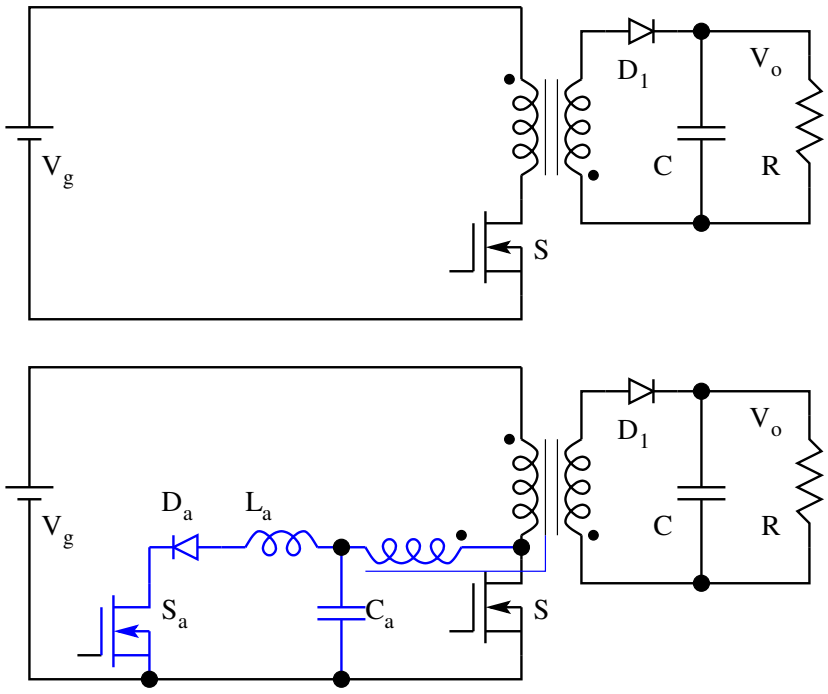

Figure K.14: Flyback Converter and its ZVS Variant

4. Forward Converter

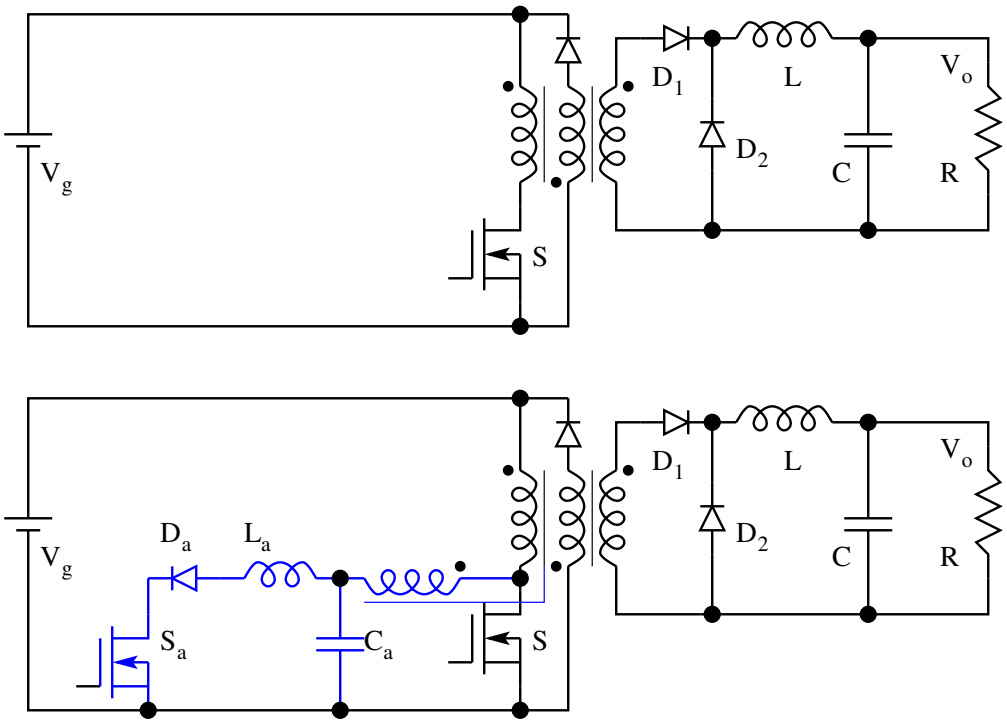

Figure K.15: Forward Converter and its ZVS Variant

5. Push-Pull Converter

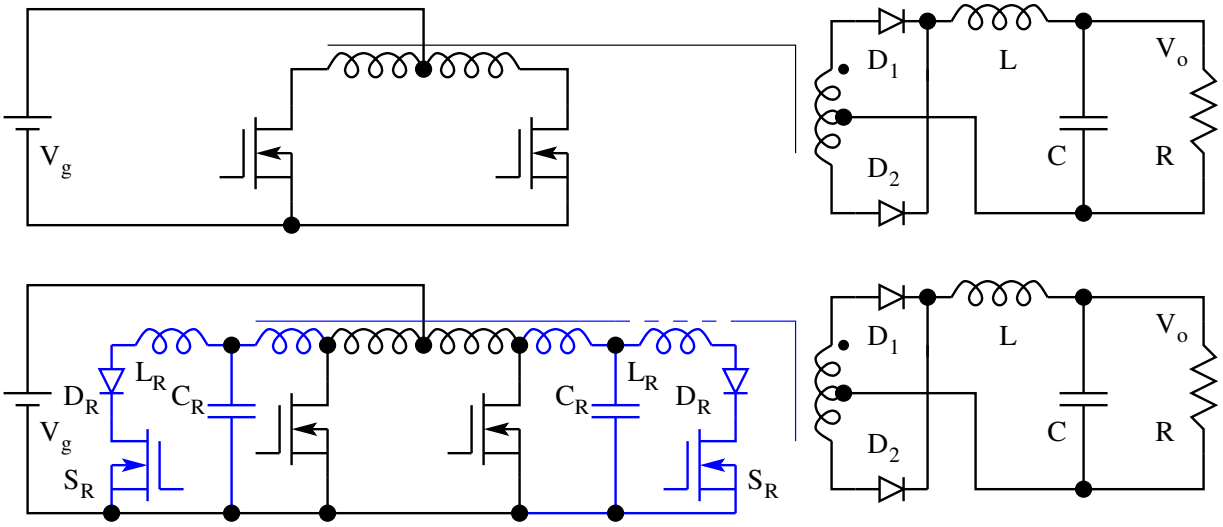

Figure K.16: Push-Pull Converter and its ZVS Variant

6. Cuk Converter

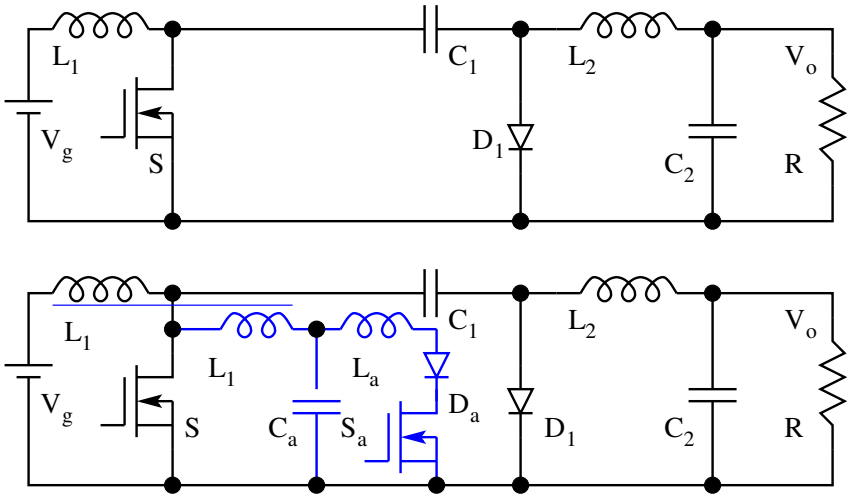

Figure K.17: Cuk Converter and its ZVS Variant

7. Two Switch Forward Converter

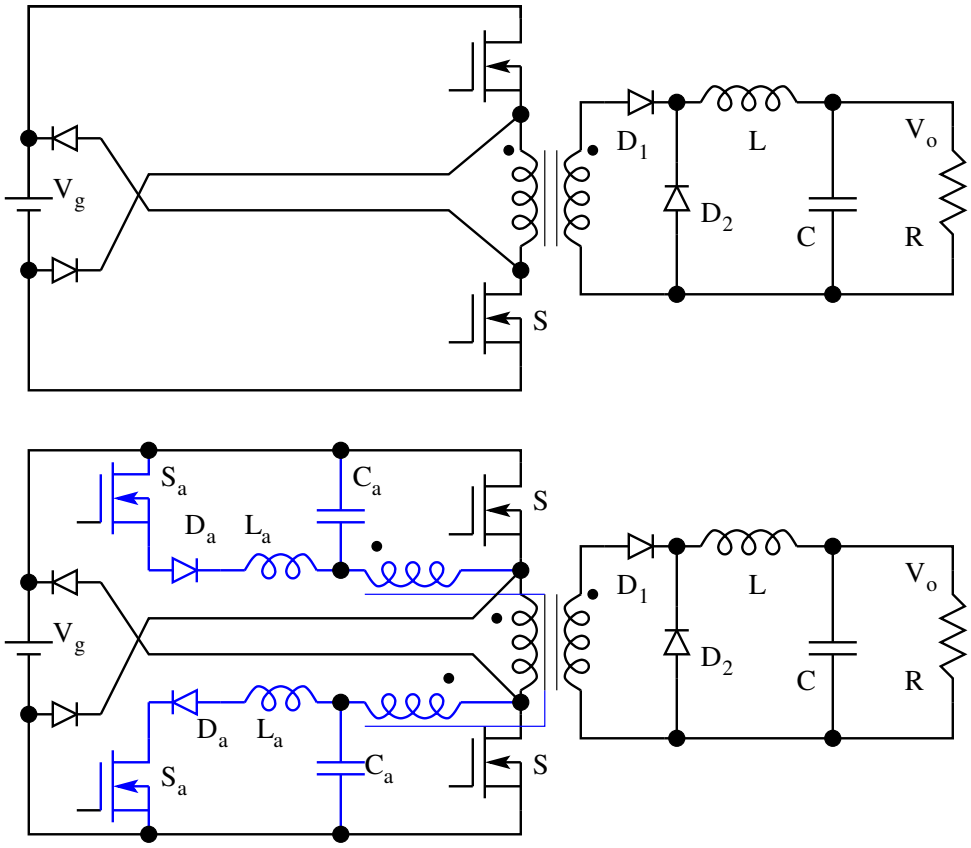

Figure K.18: Two Switch Forward Converter and its ZVS Variant

8. Sepic Converter

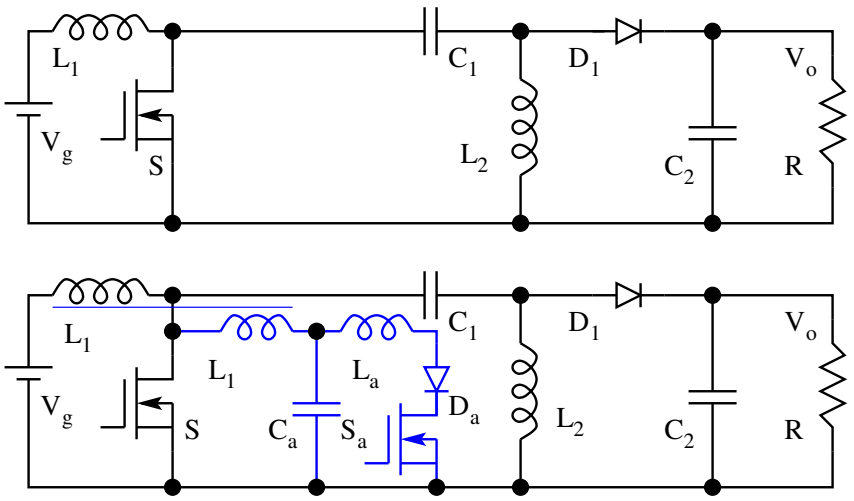

Figure K.19: Sepic Converter and its ZVS Variant

9. Half-Bridge Converter

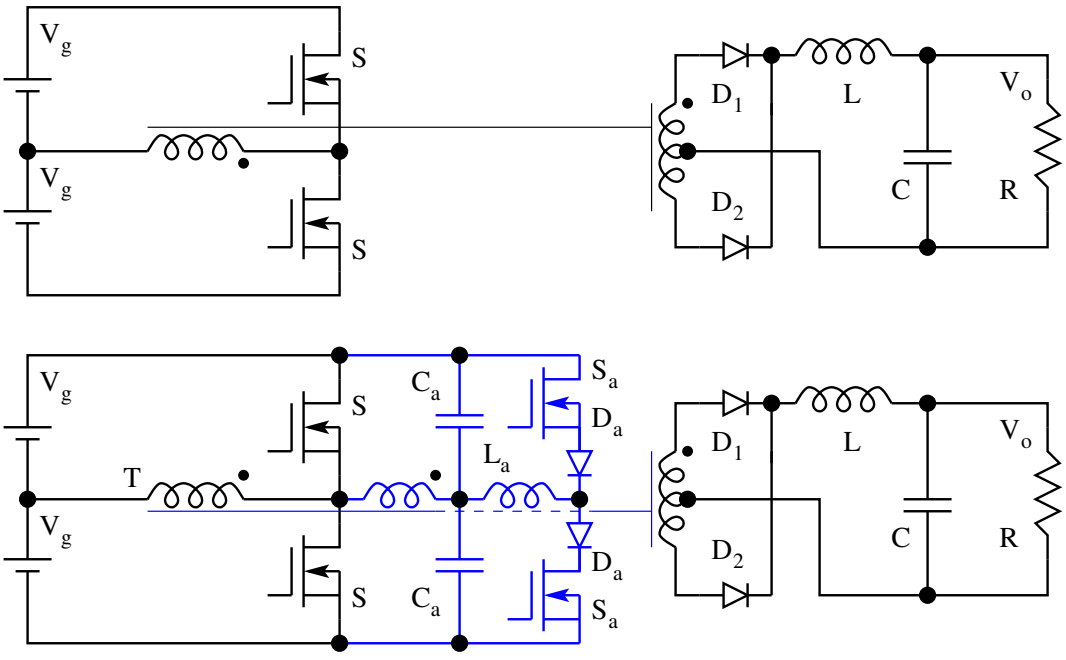

Figure K.20: Half-Bridge Converter and its ZVS Variant

10. Full-Bridge Converter

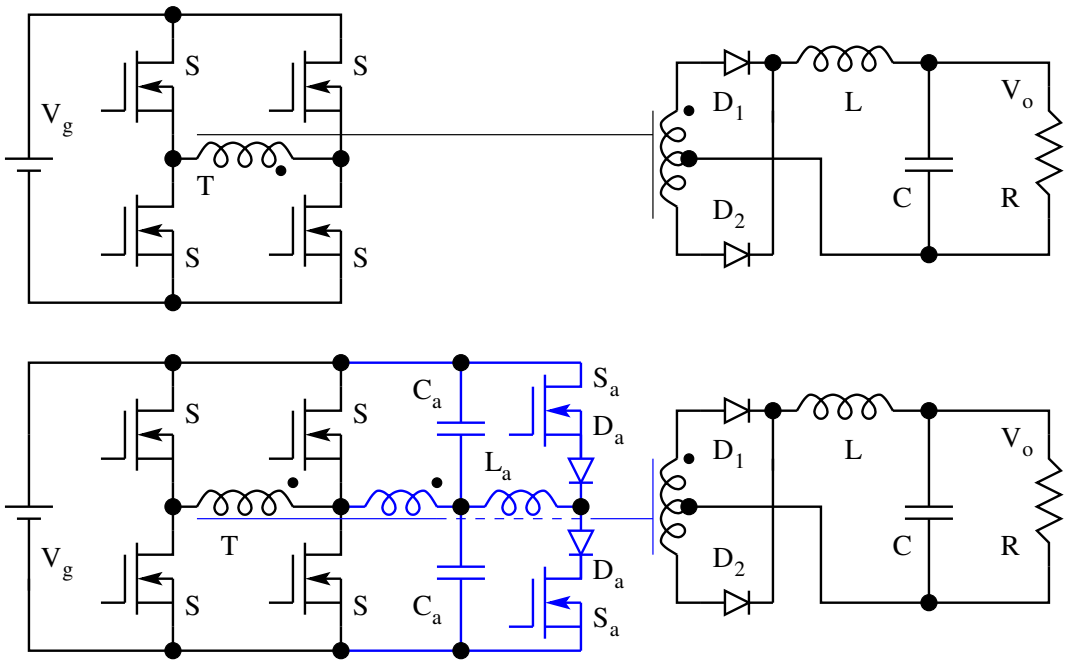

Figure K.21: Full-Bridge Converter and its ZVS Variant

11. Synchronous Rectifier

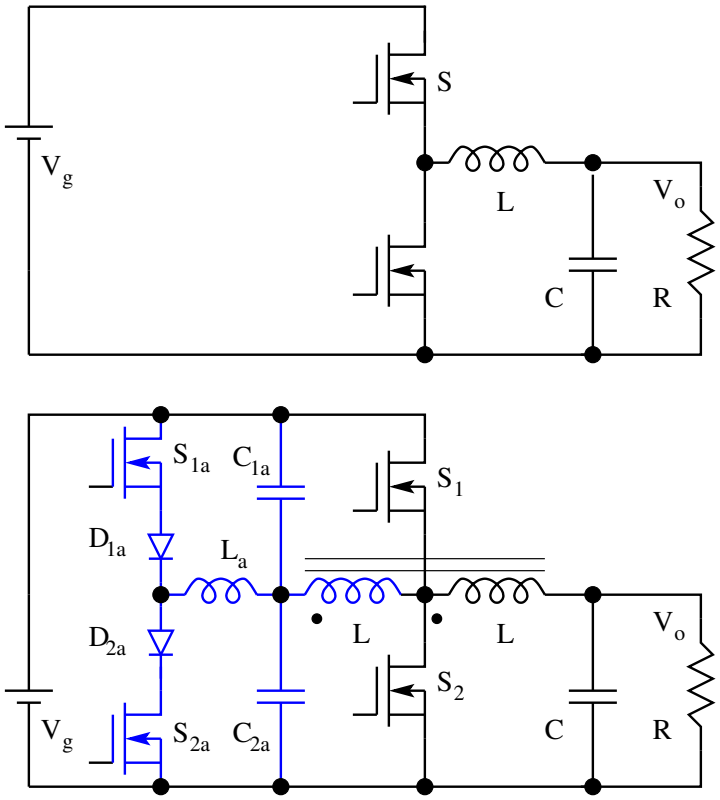

Figure K.22: A Synchronous Rectifier and its ZVS Variant

12. Bridge Arm of a Motor Drive

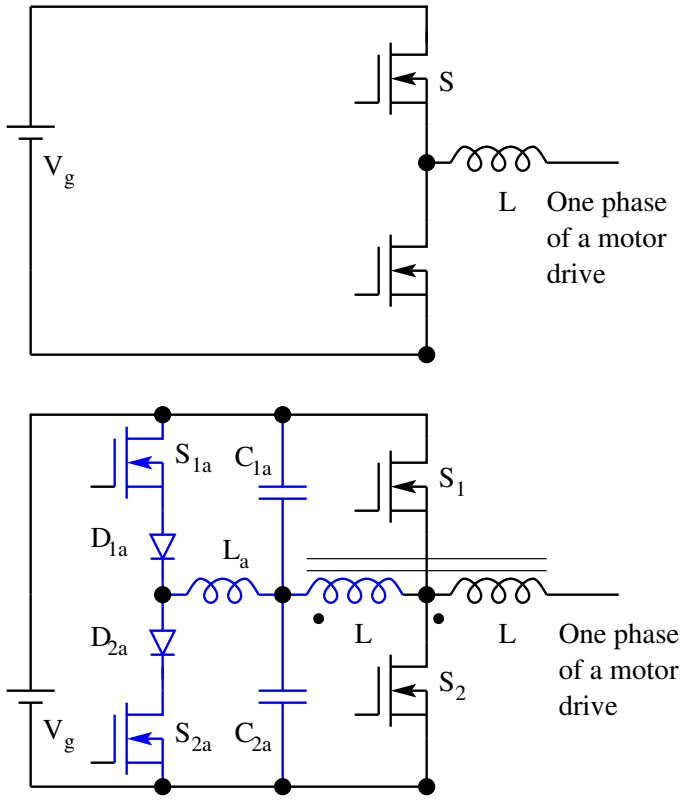

Figure K.23: A Motor Drive Arm and its ZVS Variant

It is seen that the new soft switching circuit is applicable to every hard switching converter. The performance is also identical in all the applications. We see the mathematical analysis of the performance for a sample (buck) converter.

Buck Converter (Commutation Process)

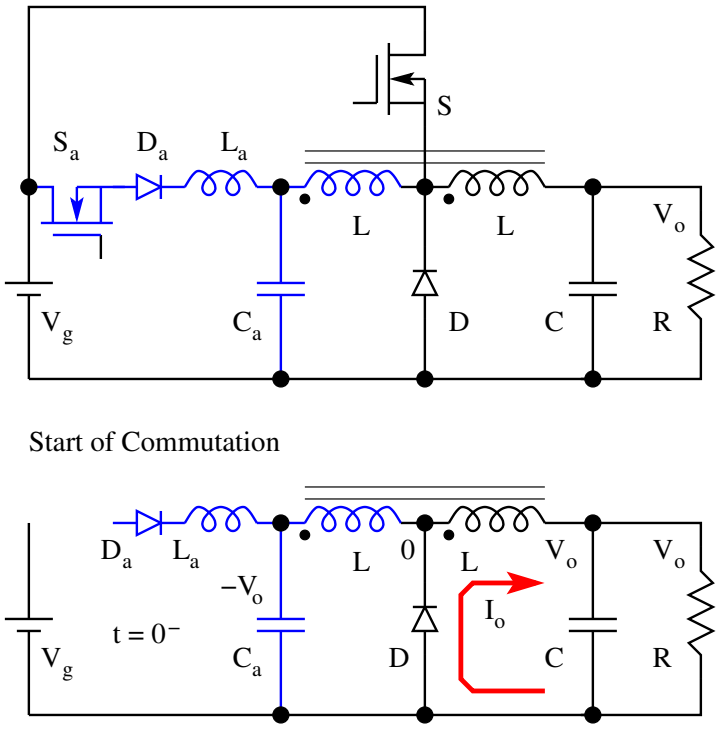

Figure K.24: ZVS Buck Converter - Start of Commutation

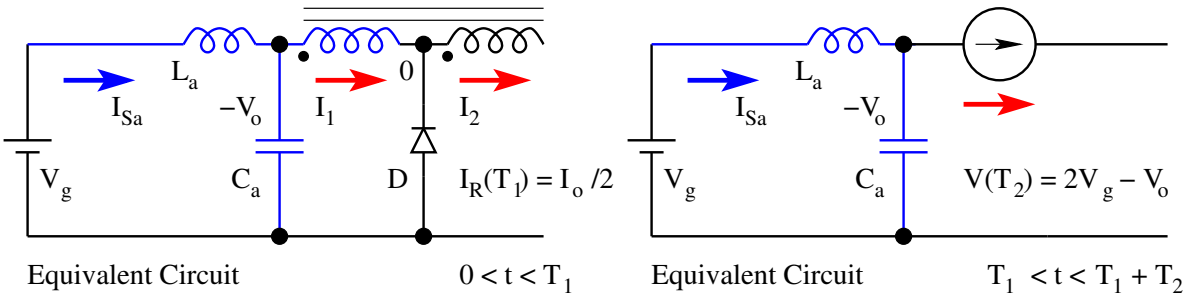

Figure K.25: Commutation Process - Intervals T_1 and T_2

Define Throw Voltage $V_T = V_g$; and Pole Current $I_P = I_o$;
The throw voltage V_T and pole current I_P will be different for different converters. For Buck converter, $V_T = V_g$; and $I_P = I_o$.

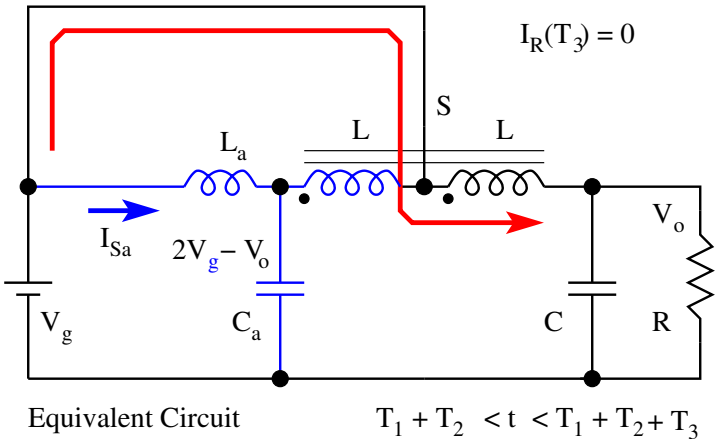

Figure K.26: Commutation Process - Interval T_3

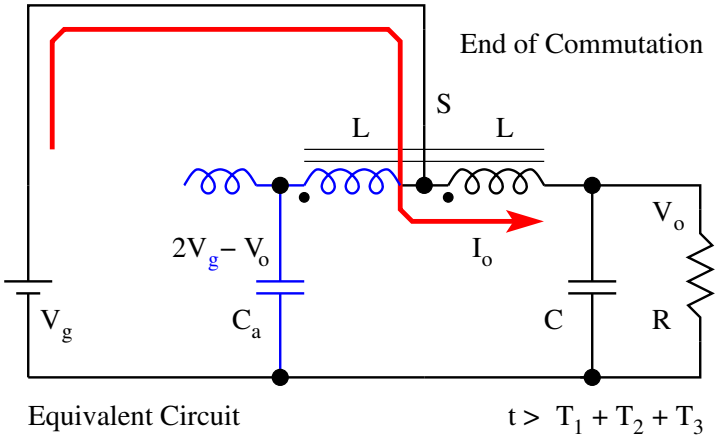

Figure K.27: Commutation Process - End of Commutation

Interval 1:

$$I_R(t) = \frac{(V_g + V_o)}{L_R} = \frac{V_T(1+d)}{L_R} \tag{K.14}$$

End of interval T_1 is when $I_R = I_P/2$

$$T_1 = \frac{I_P L_R}{2V_T(1+d)} \tag{K.15}$$

Interval 2:

$$i_{Sa}(t) = V_T(1+d)\sqrt{\frac{C_a}{L_a}}\,Sin(\omega t) + \frac{I_P}{2} \tag{K.16}$$

$$v_{Ca}(t) = V_T - V_T(1+d)\,Cos(\omega t) \tag{K.17}$$

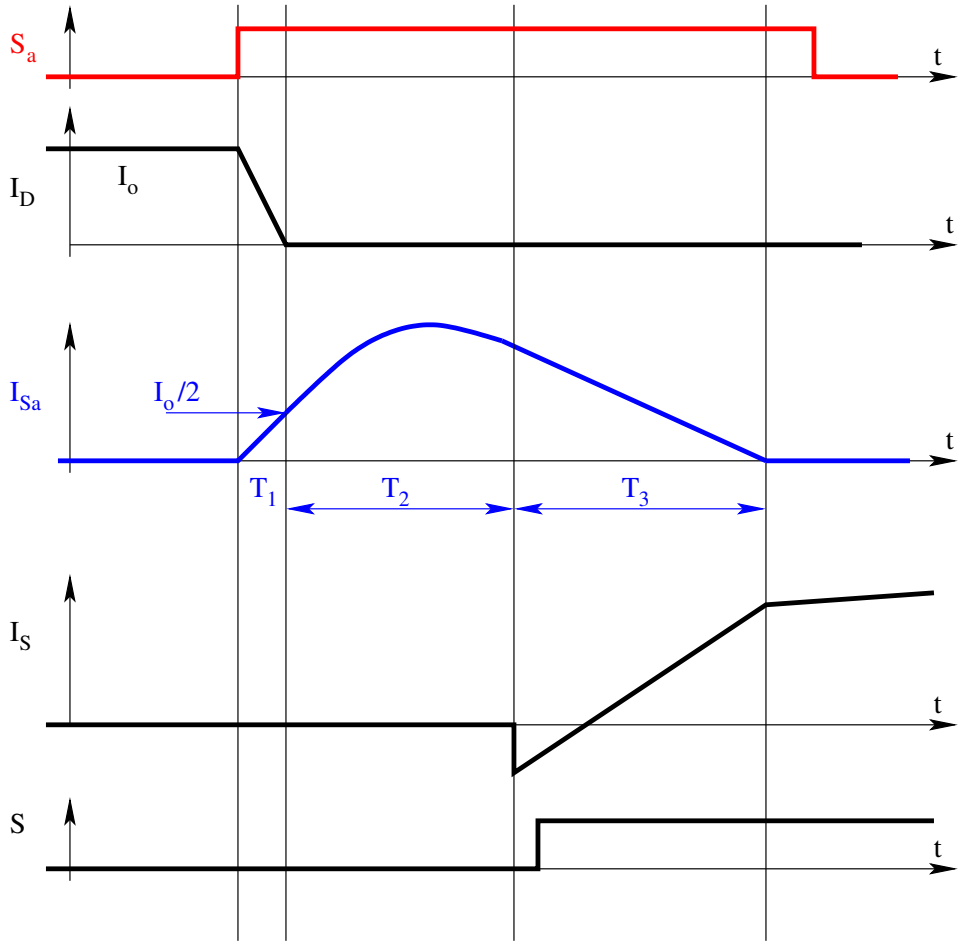

Figure K.28: Commutation Waveforms

End of interval T_2 is when $V_C = 2V_T - V_o$

$$\omega\, T_2 = Cos^{-1} - \frac{(1-d)}{(1+d)} \tag{K.18}$$

The valid solution for ωT_2 is from the second quadrant.

$$i_{Sa}(T_2) = 2\, V_T\, \sqrt{d}\sqrt{\frac{C_a}{L_a}} + \frac{I_P}{2} \tag{K.19}$$

Interval 3:

$$i_{Sa}(t) = \frac{V_T(1-d)}{L_a}\, t \tag{K.20}$$

End of interval T_3 is when $i_{Sa}(T_3) = 0$

$$T_3 = 2\,\sqrt{L_a C_a}\frac{\sqrt{d}}{(1-d)} + \frac{I_P L_a}{V_T(1-d)} \tag{K.21}$$

K.7 Exploitation of Circuit Parasitics

It is possible to realise the resonant elements in the circuit L_a and C_a out of the parasitic elements. Such a minimal circuit is shown in Fig. 29. Notice that the resonant inductor L_a is now the leakage inductance of the coupled winding and the resonant capacitor is the junction capacitance C_{DS} of the main switch S.

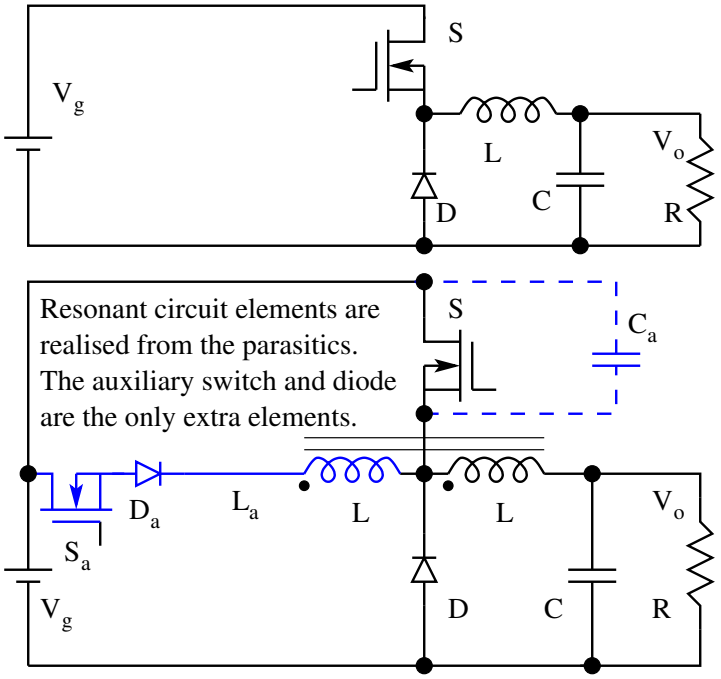

Figure K.29: A Minimal (Buck) Converter with ZVS Features

K.8 Additional Innovations

In several ZVS schemes, the delay to be incorporated between the auxiliary switch and the main switch is not constant and varies with load and other operating conditions. In the current invention, since the resonant capacitors are ground referenced or power supply referenced, it is possible to programme the delay between the auxiliary switch and the main active switch dependent on the capacitor voltage to sence the completion of the resonant process (T_2). The idea is illustrated for one of the converters in Fig. 30.

Another source of difficulty associated with ZVS is the recovery of the body diode of the main device. The body diode takes a long time to recover on account of the fact that the recovery takes place on almost zero voltage.

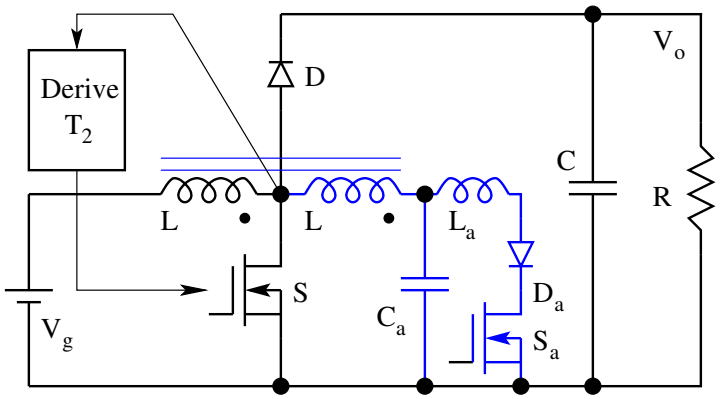

Figure K.30: Derivation of the Switch Delay based on Capacitor Voltage

This puts a minimum on period limit on the main switching device in any application. The control scheme shown in Fig. 30 may be used to overcome this problem. The delay T_2 may be set just before the instant the body diode starts conducting. This serves the dual purpose of reducing the switching loss close to zero and not getting the body diode of the main switch to conduct.

K.9 Salient Features

Now the salient features of the invention are listed.

1. An auxiliary circuit consisting of an electronic switch such as a diode, BJT, MOSFET, IGBT, or SCR, a resonant inductor, a resonant capacitor, and an auxiliary dependent or independent source to enable ZVS transitions of the main switch and ZCS transitions of the auxiliary switch.

2. An auxiliary dependent or independent source in the circuit to enable ZVS transitions of the main switch.

3. A coupled winding in the energy storage inductor or the energy transfer transformer or the energy conversion winding (in case of motor or generator type of load) of the power converter (acting as the said auxiliary source), enabling ZVS transitions of the main switch and ZCS transitions of the auxiliary switch.

4. A control strategy of sequentially turning on the auxiliary switch and main swith with appropriate delays to achieve ZVS transitions of the main switch and ZCS transitions of the auxiliary switch.

5. Combinations of the above auxiliary devices and the control strategy to all types of power converters, synchronous rectifiers, motor drives with and without input filter to achieve ZVS transitions of the main switch and ZCS transitions of the auxiliary switch.

6. Different ratios of coupling to obtain the auxiliary source so that the reset time of the auxiliary switch can be conveniently selected.

7. Different locations of the resonant capacitor (such as across the main switch) to obtain additional advantages of using the parasitics of the devices in place of the resonant elements.

8. Adaptive delay schemes based on the device voltage prior to being turned on. This makes the ZVS operation of circuit insensitive to operating parameters. Further it can be employed to prevent the body diode conduction prior to turn-on of the device.

9. Presence of ZVS at light loads and in discontinuous conduction mode (DCM) as well.

K.10 References

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Appendix L

Data Sheets

L.1 Chapter 1 - Power Switching Devices

20ETSxxx Recifier Diodes

RHRG30120CC Fast Rectifier Diode

MBRP30060CT Schottky Barrier Diode

MCR16 Silicon Controlled Rectifier

T2500FP Bidirectional Silicon Controlled Rectifier

BUX48 NPN Silicon Power Transistor

MJ10015 NPN Silicon Power Darlington Transistor

IRF540N Power MOSFET

HGTG30N120D2 IGBT

MCTX65P100F1 MOS Controlled Thyristor

CM50DY28H 50 A, 1400 V Half Bridge IGBT

PM75CVA120 75 A, 1200 V Six Pack IGBT IPM

L.2 Chapter 2 - Reactive Elements in SMPC

Ferrite Materials

E20/10/6 EE Core and Accessories

ETD 44/22/15 ETD Core and Accessories

EFD 30/15/9 EFD Core and accessories

Ferrite Data Book Siemen's Ferrite Catalogue

Electrolytic Capacitors Single Ended Electrolytic Capacitors

Electrolytic Capacitors Double Ended Electrolytic Capacitors

Bipolar Capacitors AC Capacitors

L.3 Chapter 3 - Control and Protection of Power Devices

HCPL3100/3101 IGBT/MOSFET Driver Optocoupler

EXB8xx IGBT Driver Hybrid Circuit

MC33153 Single IGBT Driver

SKHI Semikron Drivers

M57957L IGBT Driver Hybrid Circuit

M57915L Transistor Driver Hybrid Circuit

UCX706 Unitrode Dual Driver

L.4 Chapter 4 - DC to DC Converters

High Frequency Power Converters

L.5 Chapter 6 - Controller ICs

UC1524/2524/3524 Advanced Pulsewidth Modulators

UC494/495 Advanced Pulsewidth Modulators

UCC3570 Voltage Mode PWM Controller

TDA4605 General Purpose PWM Controller

L.6 Chapter 7 - Current Controlled Converters

UC3842/3/4/5 Current Mode Controllers

L.7 Chapter 8 - Resonant Power Converters

UC1875 Resonant transition converter controller

UC1861–68 Quasi-resonant converter controllers

L.8 Chapter 9 - Unity Power Rectifiers

UC3854 UPF Rectifier controller

UC3854 Application UPF Rectifier Controller Application Note

Appendix M

Test Papers

M.1 Switched Mode Power Conversion

2007 Switched Mode Power Conversion

2006 Switched Mode Power Conversion

2005 Switched Mode Power Conversion

2004 Switched Mode Power Conversion

2003 Switched Mode Power Conversion

2002 Switched Mode Power Conversion

2001 Switched Mode Power Conversion

2000 Switched Mode Power Conversion

1999 Switched Mode Power Conversion

1997 Switched Mode Power Conversion

M.2 Power Electronics

2007 Power Electronics

2006 Power Electronics

2005 Power Electronics

Appendix N

World-Wide Links

N.1 University Sites:

http://minchu.ee.iisc.ernet.in/people/faculty/vram/peg.htm
Power Electronics Group, Department of EE,
Indian Institute of Science
http://www.wempec.org
Wisconsin Electrical Machines and
Power Electronics Consortium
http://ece-www.colorado.edu/
University of Colorado at Boulder
http://www.ee.umn.edu/research/areas/energy/
University of Minnesota
http://www.cpes.vt.edu
Virginia Power Electronics Centre
http://fpec.cecs.ucf.edu/research.htm
University of Central Florida, Dr. Issa Batarseh
http://ece.colorado.edu/ maksimov/
University of Colorado, Dr. Dragan Maksimovic

N.2 Distributors of Power Devices, Control ICs & other Hardware:

http://www.arrow.com
Arrow Electronics
http://www.avnet.com
Avnet Electronics
http://www.digikey.com
Digikey Corporation

http://www.newark.com
Newark Electronics
http://www.mouser.com
Mouser Electronics

N.3 Semiconductor Devices & Controllers:

http://www.advancedpower.com
APT (Advanced Power Technology)
Power Semiconductor Devices
http://www.intersil.com
Intersil Corporation (also former Harris Semiconductors)
http://www.ti.com
Analog & Mixed signal (Former Unitrode)
http://www.onsemi.com
Former Motorola Semiconductors
http://www.agilent.com
Former HP semiconductors and optoelectronic devices
http://www.irf.com
International Rectifiers
http://www.mitsubishichips.com/Global/products/power/index.html
Mitsubishi Semiconductors for High Power Devices & Drivers
http://www.semikron.com
Semikron
http://www.infineon.com
Former Siemens Semiconductors
(Controllers and Power Devices)
http://www.epcos.com
Former Siemens Magnetics, Thermistors, and Capacitors
http://www.eupec.com
European Power Electronics Consortium
High Power Devices and Drivers
http://www.micrel.com
Micrel
http://www.maxim-ic.com
Maxim Analog and Mixed Signal ICs
http://www.microlinear.com
Microlinear ICs
http://www.powerint.com
Power Integration - Manufacturers of TopSwitch
http://www.semiconductors.philips.com/products/
Philips Semiconductors

http://www.vishay.com/power-ics/
: Vishay Semiconductors

http://www.fujielectric.co.jp/eng/fdt/scd/
: Fuji Electric

http://www.ixys.com/pinfo.html
: IXYS Power Device

http://www.semicon.toshiba.co.jp/eng/index.html
: Toshiba Semiconductors

http://www.st.com
: ST Microelectronics

N.4 Professional Societies:

http://www.ieee.org/
: IEEE

N.5 Power Supply Manufacturers:

http://www.ericsson.com/products/powermodules/
: Ericsson Power Modules

http://www.kepco.com/
: Kepco

http://www.lambdapower.com/
: Lambda

http://www.power-one.com
: Power-One

N.6 Measuring Instruments:

http://www.venable.biz/
: Venable Frequency Response Analyser

http://www.ridleyengineering.com/
: Ridley Frequency Response Analyser

http://www.solartronanalytical.com/fra/1250.php
: Solartron Frequency Response Analyser

http://www.clarke-hess.com/2505.html
: Clarke-hess Instruments

http://www.nfcorp.co.jp/english/products/a/a06/a06-1.html
: NF Corporation Japan - Frequency Response Analyser

N.7 Sensors:

http://www.lem.com
LEM Current Sensors & Power Analyser Products
http://www.telcon.co.uk
Telcon Current Sensors
http://www.telcon.co.uk/FrameSet2.html
Telcon Magnetic Products
http://www.micronas.com/products/overview/sensors/index.php
Raw Hall Sensors
http://www.lakeshore.com/mag/hs/hsm.html
Hall Sensors
http://www.semicon.toshiba.co.jp/eng/prd/sensor/index.html
Sensors (Hall, Image. Photo)

N.8 Simulation Software:

http://www.orcad.com
OrCAD Simulation Software
http://www.analogy.com/products/mixedsignal/saber/saber.html
Saber Simulation Software

N.9 SMPS Technology Base:

http://www.smpstech.com/
Knowledge Base on SMPS Technology
http://www.smpstech.com/books/booklist.htm
Power Electronics Book List
http://www.smpstech.com/vendors.htm
Worldwide Power Electronics Vendors
http://www.ridleyengineering.com/
Knowledge Base on SMPS Technology
http://www.darnell.com
Darnell Power Electronics Group -
Special Interest Group in Power Electronics
http://www.smps.us/Unitrode.html
Unitrode Seminar Topics -
Interesting Old Unitrode Design Reviews are located here.

http://www.geocities.com/CapeCanaveral/Lab/9643/TraceWidth.htm
PCB Track Width Calculator & Other Details of PCB Tracks

http://users.telenet.be/educypedia/electronics/powerelectronics.htm
A Rich Source of Resources Across Several
Related Disciplines
http://www.drivesurvey.com/index_home.html
An Internet Magazine for Industrial Drives

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