

RF circuit design: Basics

Akira Matsuzawa

Tokyo Institute of Technology

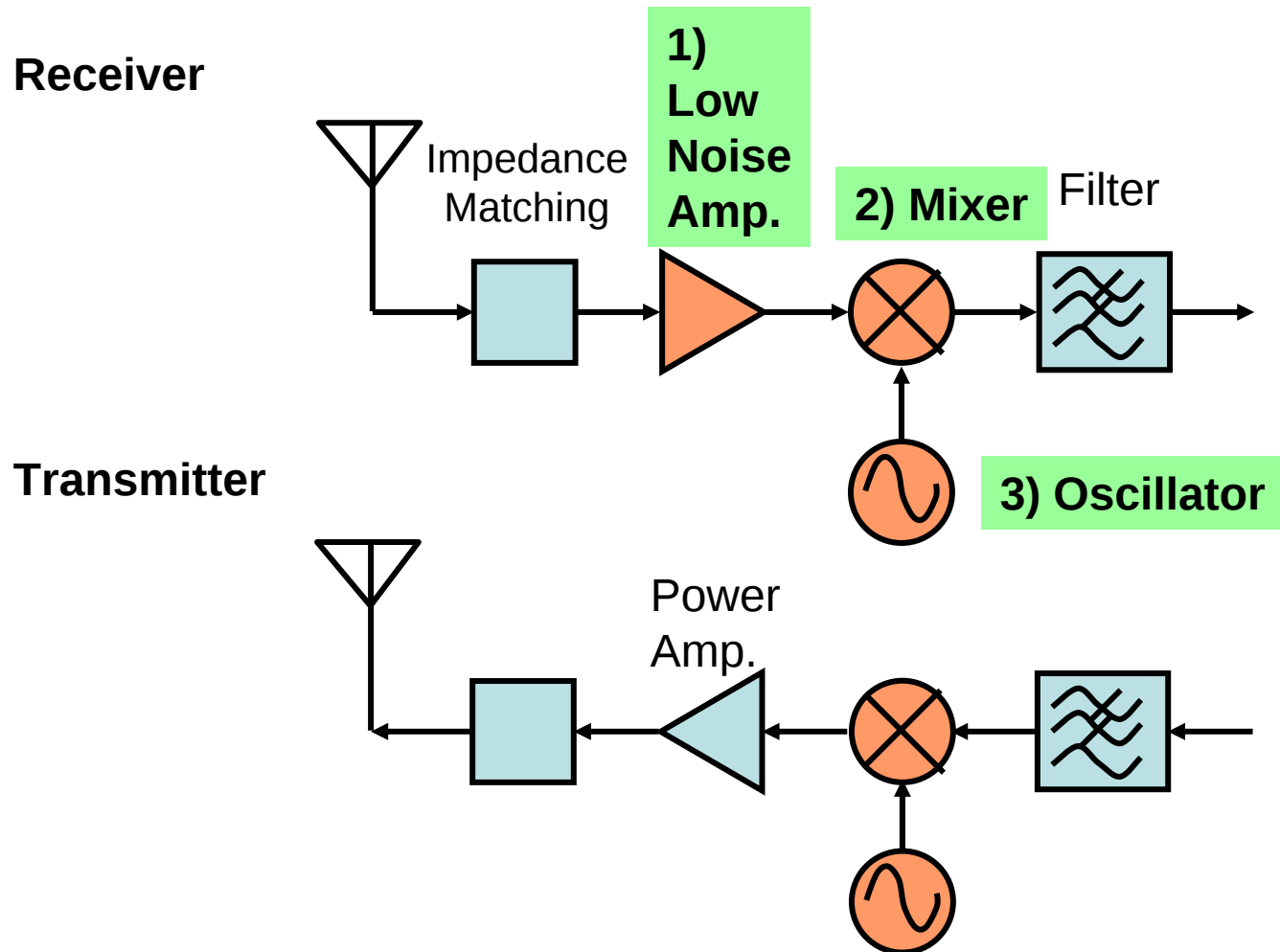
Contents

- Building blocks in RF system and basic performances
- Device characteristics in RF application
- Low noise amplifier design
- Mixer design
- Oscillator design

Basic RF circuit block

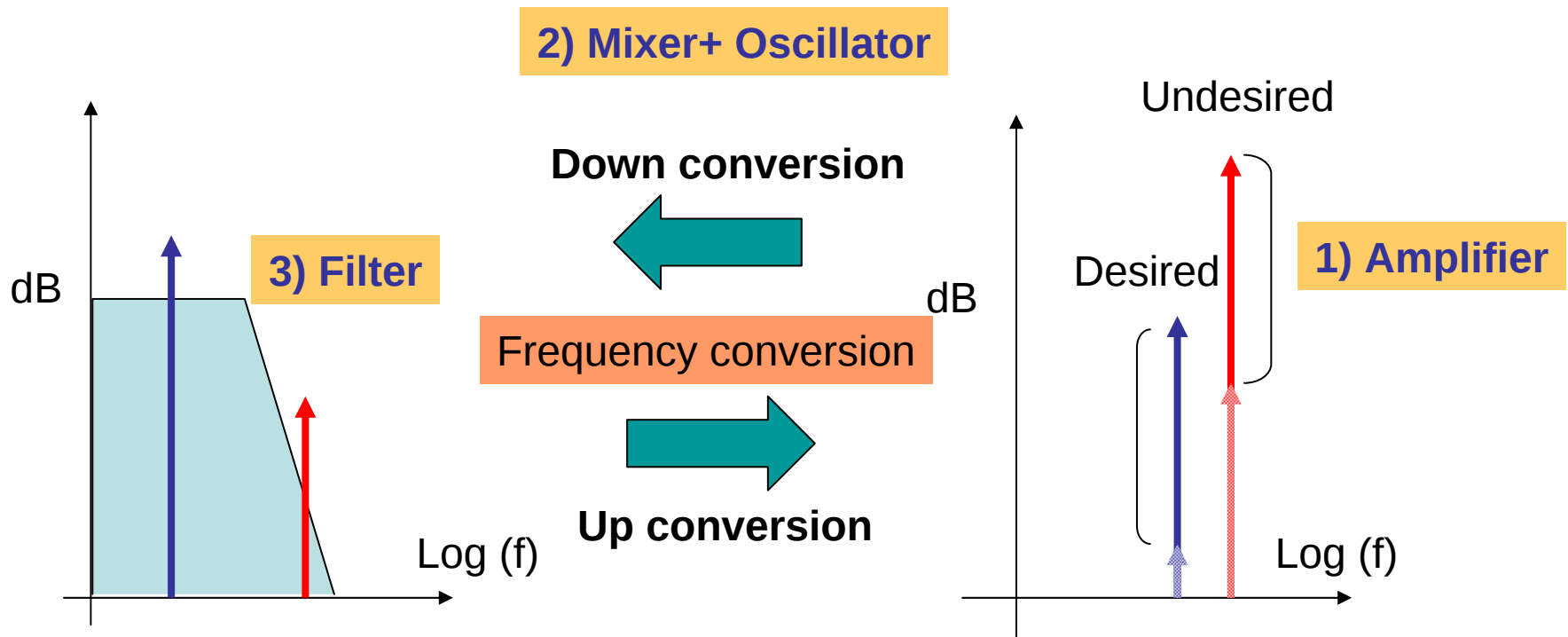
RF systems are composed of limited circuits blocks.

LNA, Mixer, and Oscillator will be discussed in my talk.



Basic functions of RF building blocks

Amplifier, frequency converter (mixer + oscillator), and filter are basic function blocks in RF system.



RF Amplifier

- **Gain:** Amplify small signal or generate large signal.
- **Noise:** Smaller noise and larger SNR.
- **Linearity:** Smaller non-linearity.

Non-linearity generates undesired frequency components.

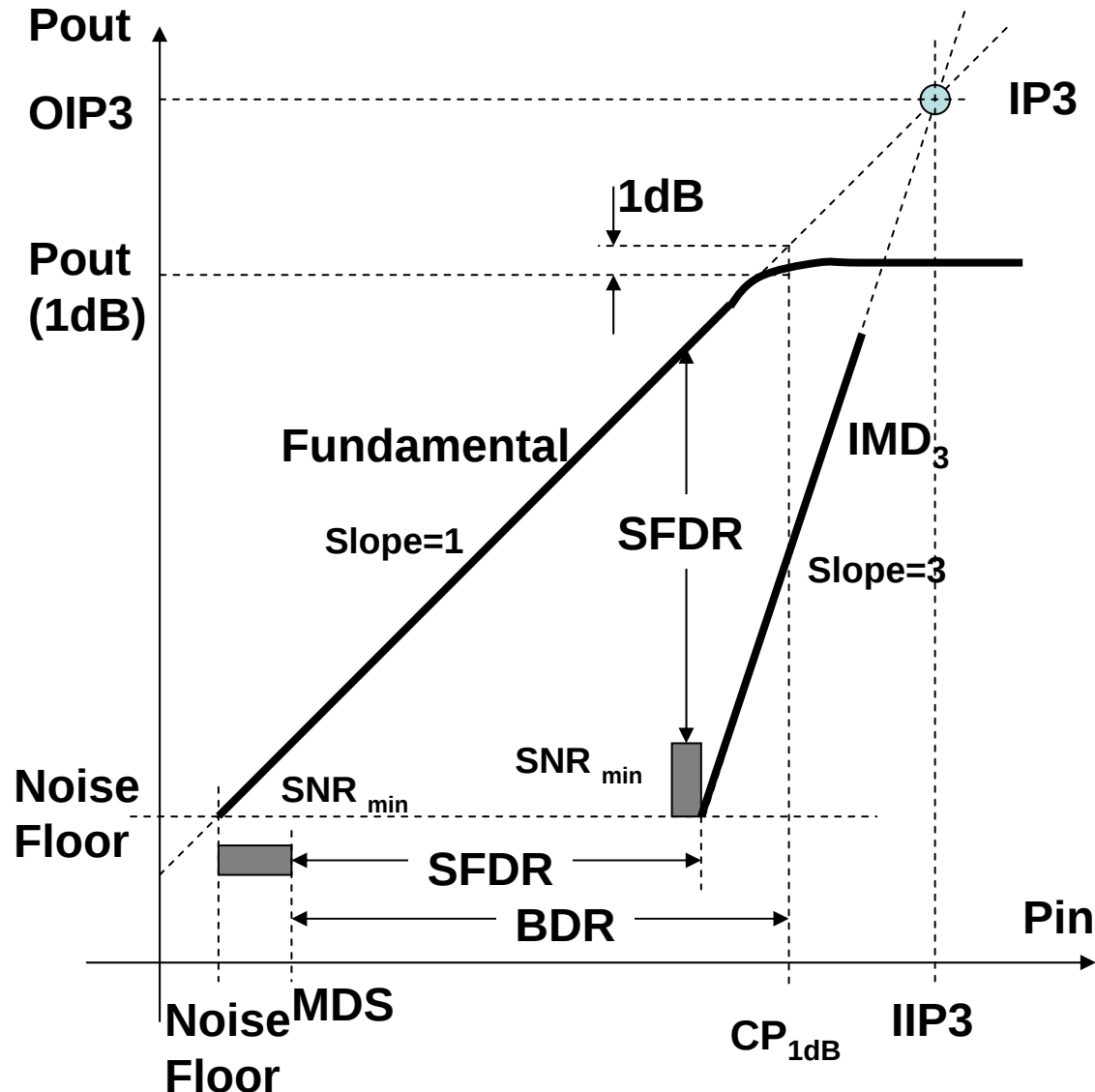
$$v_{out}(t) = \alpha_1 v_{in}(t) + \alpha_2 v_{in}^2(t) + \alpha_3 v_{in}^3(t) + \dots$$

$$(\cos(\omega_1 t) + \cos(\omega_2 t))^2 = 2 + \cos(2\omega_1 t) + \cos(2\omega_2 t) + \cos((\omega_1 - \omega_2)t) + \cos((\omega_1 + \omega_2)t)$$

$$(\cos(\omega_1 t) + \cos(\omega_2 t))^3 = \frac{1}{2} \cos((2\omega_1 - \omega_2)t) + \frac{1}{2} \cos((2\omega_2 - \omega_1)t) + \dots$$

Input and output characteristics

Distortion and noise are important factors in RF amplifier, as well as power and gain.



Dynamic range

$$\text{Noise Floor} = \underbrace{-174\text{dBm}}_{\text{kT limitation}} + NF + 10\log \underbrace{BW}_{\text{Bandwidth}}$$

SFDR: Spurious free dynamic range

The input power range over which third order inter-modulation products are below the minimum detectable signal level.

$$SFDR = \frac{2}{3}(IIP_3 - \text{Noise Floor}) - SNR_{\min}$$

BDR: Blocking dynamic range

$$BDR = P_{1dB} - \text{Noise Floor} - SNR_{\min}$$

MDS: Minimum detectable signal level = Noise Floor + $SNR_{\min}$

Non-linearity

CP_{1dB} : The input level at which the small signal gain has dropped by 1dB.

$$CP_{1dB} = \sqrt{0.145 \left| \frac{\alpha_1}{\alpha_3} \right|}$$

IMD3: The third order inter modulation term

IP3: The metric third order intercept point. It is the point where the amplitude of third order inter modulation is equal to the that of fundamental.

$$A_{IP3} = \sqrt{\frac{4}{3} \left| \frac{\alpha_1}{\alpha_3} \right|}$$

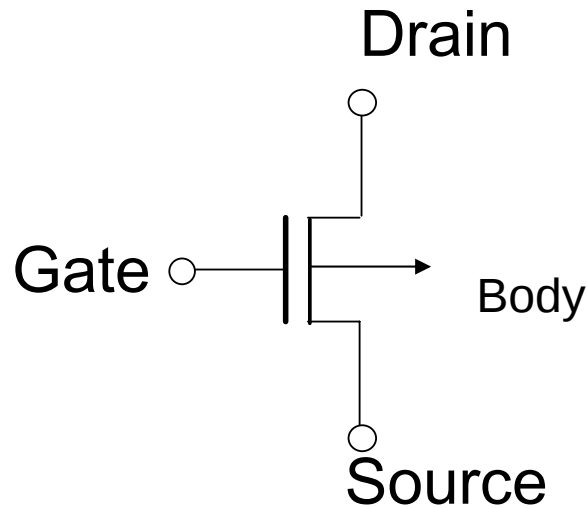
IIP3: Input referred intercept point

OIP3: Output referred intercept point

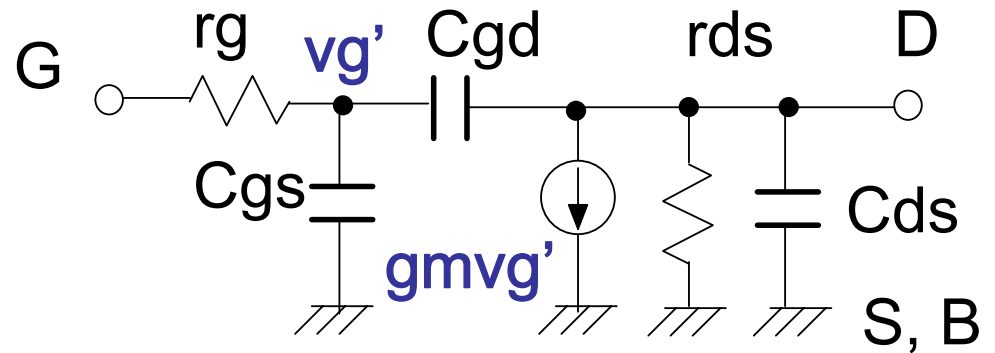
$$P_{out} - IMD_3 = 2 \cdot (IIP_3 - P_{in})$$

MOS transistor

Intrinsic gate voltage and g_m are the most important factors in RF CMOS.



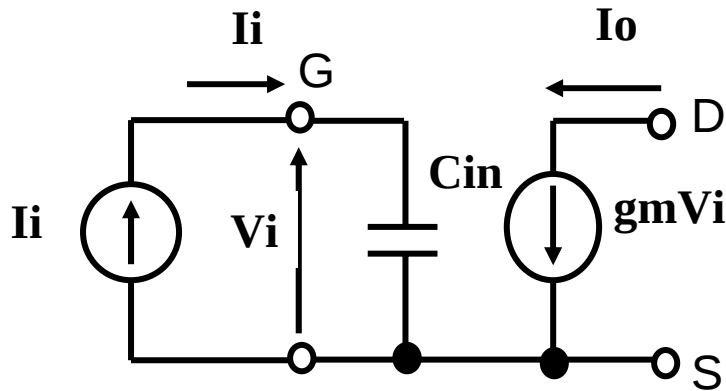
MOS Transistor



Equivalent Circuit

Cutoff frequency: f_T

For higher f_T , increase g_m and decrease C_{in} .



f_T : Frequency at which the current gain is unity.

$$I_i = I_o \sin(\omega t) \quad \text{Input current}$$

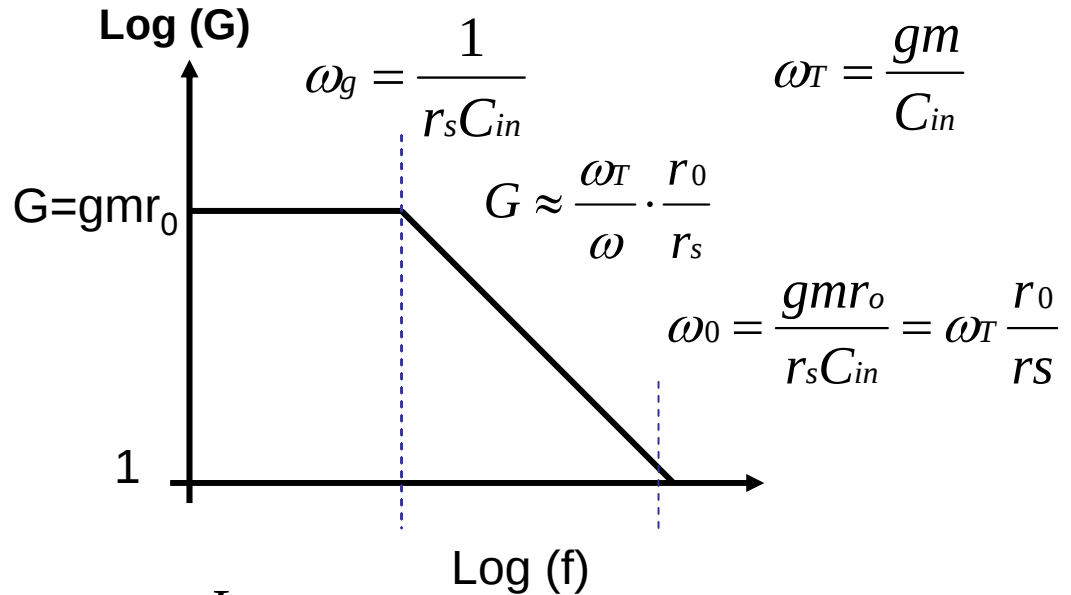
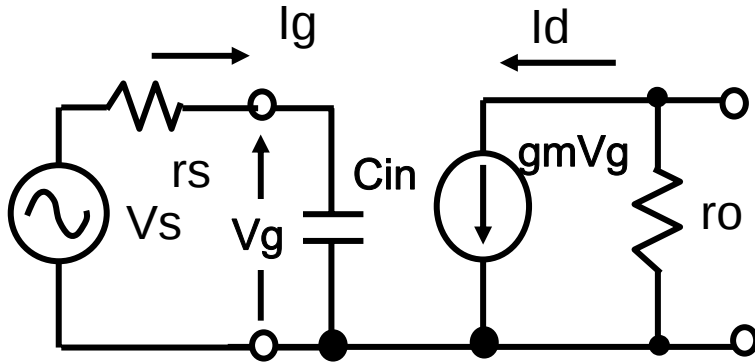
$$V_i = \frac{I_o}{\omega C_{in}} \cos(\omega t) \quad \text{Gate voltage}$$

$$I_o = g_m V_i = \frac{g_m I_o \cos(\omega t)}{\omega C_{in}} \quad \text{Output current}$$

$$\therefore f_T = \frac{g_m}{2\pi C_{in}} \quad \begin{array}{l} \text{Proportional to } g_m \\ \text{Inversely proportional to } C_{in} \end{array}$$

Amplifier gain

For higher voltage gain, increase g_m , f_T , r_o (Q), and decrease input and gate resistance



For the larger gain

Fundamentally larger $g_m r_o$ $G \approx g_m r_o \approx \frac{I_{ds}}{\left(\frac{V_{eff}}{2}\right)} \cdot r_o \rightarrow$ Larger I_{ds} or r_o
Larger Q

Higher f_T and lower r_s

V_{eff} is difficult to reduce

$$\therefore r_o = Q \omega L = \frac{Q}{\omega C}$$

$\rightarrow$ Distortion and C_{in} increase

Characteristics of gm (Basic)

Gm is proportional to the I_{ds} and inversely proportional to the V_{eff} .

V_{eff} is proportional to square root of I_{ds} and inversely proportional to square root of (W/L) ratio.

Square law region

$$I_{ds} = \frac{\mu C_{OX}}{2n} \left(\frac{W}{L} \right) (V_{gs} - V_T)^2 = \frac{\mu C_{OX}}{2n} \left(\frac{W}{L} \right) V_{eff}^2$$

$$gm \equiv \frac{dI_{ds}}{dV_{gs}} = \frac{\mu C_{OX}}{n} \left(\frac{W}{L} \right) V_{eff}$$

$$gm = \sqrt{\frac{2\mu C_{OX}}{n} \left(\frac{W}{L} \right) I_{ds}}$$

$$V_{eff} \propto \sqrt{L \frac{I_{ds}}{W}} = \sqrt{L \cdot J_{ds}}$$

$$gm = \frac{I_{ds}}{\left(\frac{V_{eff}}{2} \right)}, \quad \frac{gm}{I_{ds}} = \frac{1}{\left(\frac{V_{eff}}{2} \right)}$$

$$V_{eff} = \sqrt{\frac{2n}{\mu} \cdot \frac{1}{C_{ox}} \cdot \frac{L}{W} \cdot I_{ds}}$$

Scaling

W/L ratio

V_{eff} is proportional to square root of drain current density.

Non-ideal effects to square low region

At larger V_{eff} and lower V_{eff} , two non-ideal effects are not negligible .

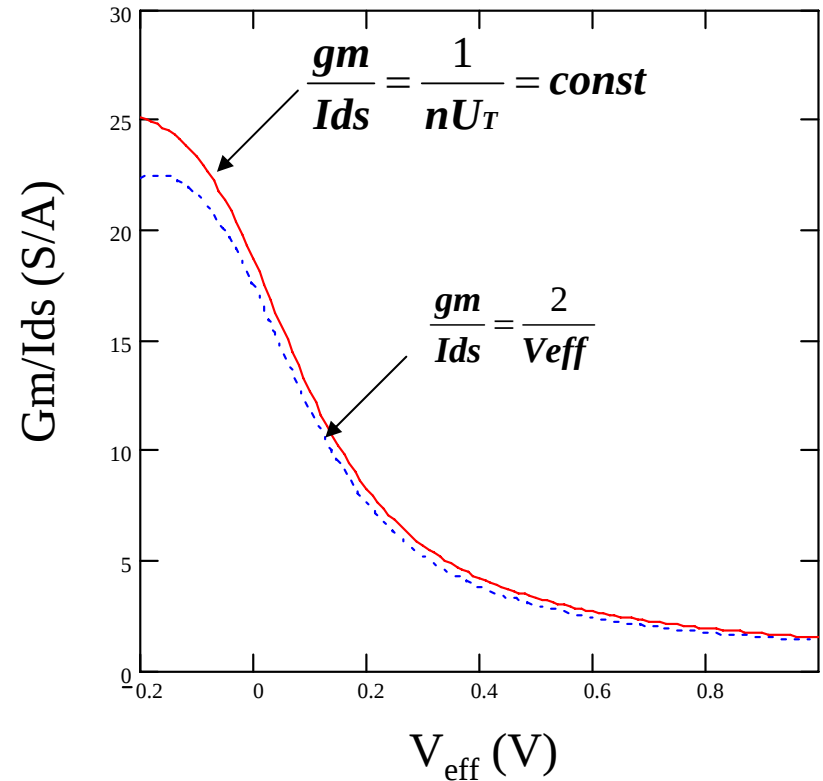
Low V_{eff} Sub-threshold region

$$I_{ds} = I_{so} \exp\left(\frac{V_{gs}}{nU_T}\right) \quad (\text{Weak inversion})$$

$$gm = \frac{I_{ds}}{nU_T} \quad \frac{gm}{I_{ds}} = \frac{1}{nU_T}$$

High V_{eff} Mobility degradation

$$\mu \approx \frac{\mu_0}{1 + \theta V_{\text{eff}}}, \quad \theta \approx \theta_0 + \frac{\mu_0}{v_c L}$$



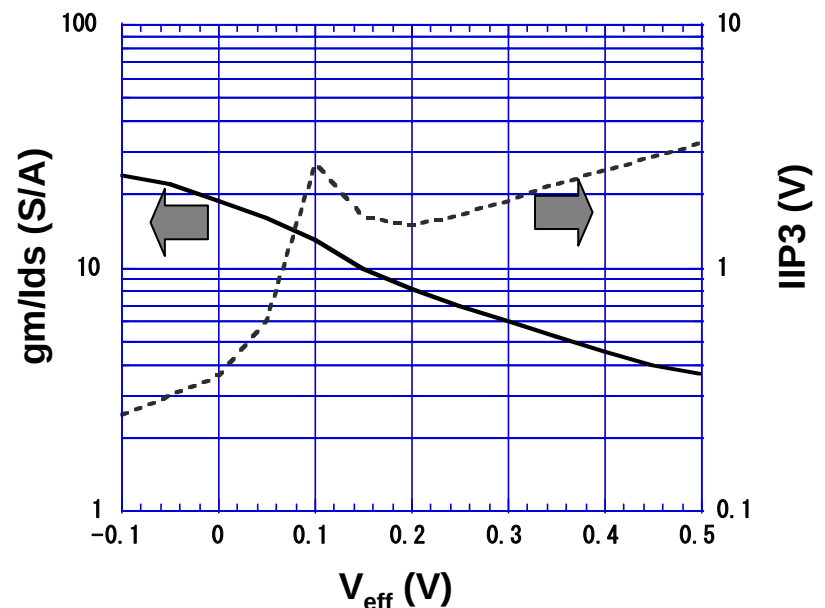
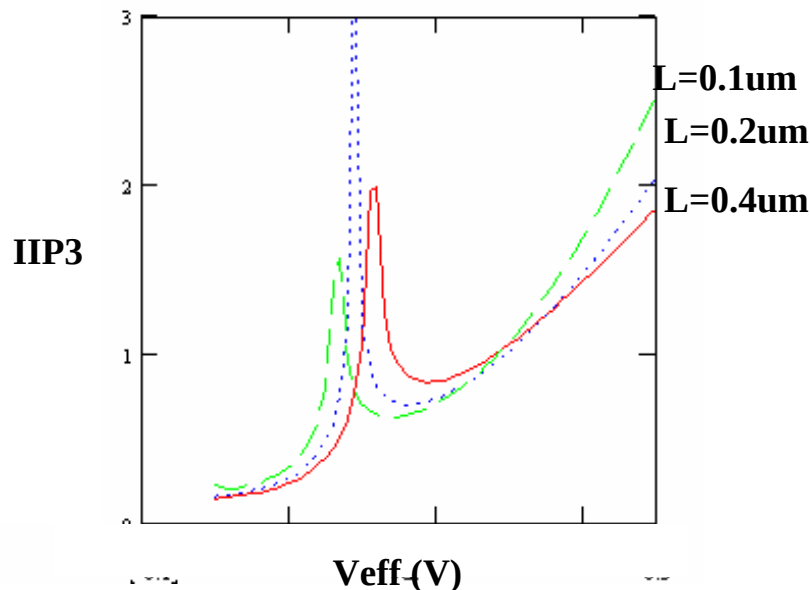
This effect becomes larger at large V_{eff} and short channel length.

Distortion

Lower V_{eff} gives higher g_m , but results in higher distortion.
To obtain lower distortion (higher IIP3), we must increase V_{eff} .

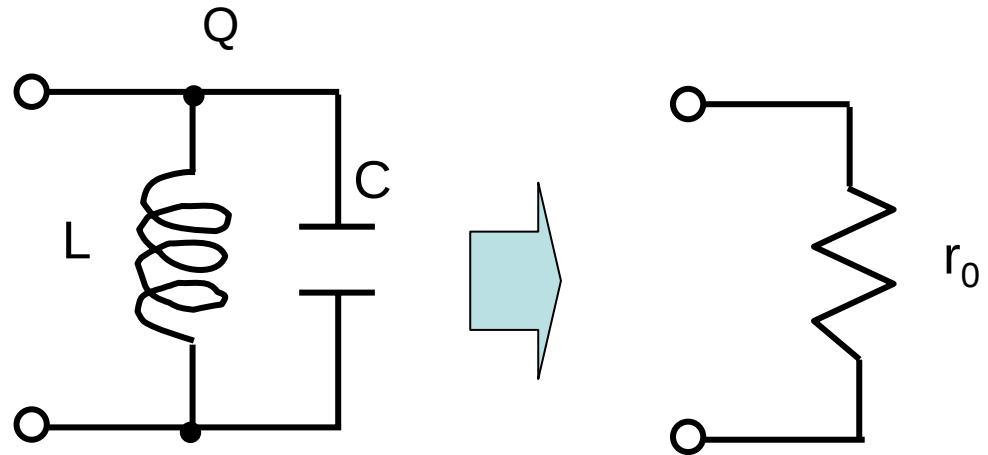
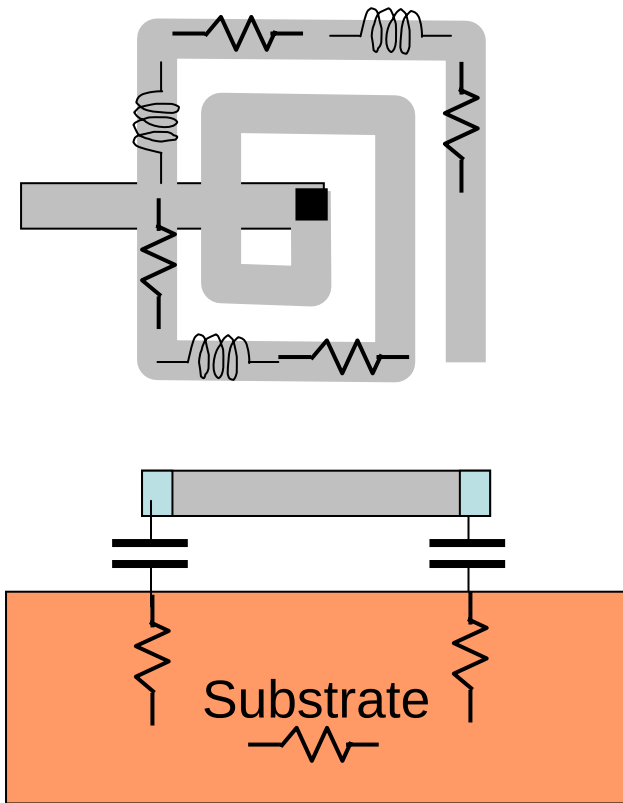
Higher g_m and lower distortion means higher I_{ds} .

$$I_{ds} = a_1 V_{eff} + a_2 V_{eff}^2 + a_3 V_{eff}^3 + \dots \quad a_3 \equiv \frac{1}{6} \frac{d^3 I_{ds}}{dV_{eff}^3} \quad I_{IP3} = \sqrt{\frac{4}{3} \left| \frac{a_1}{a_3} \right|}$$



LC resonator

LC resonator can be regarded as resistance at the resonance frequency.



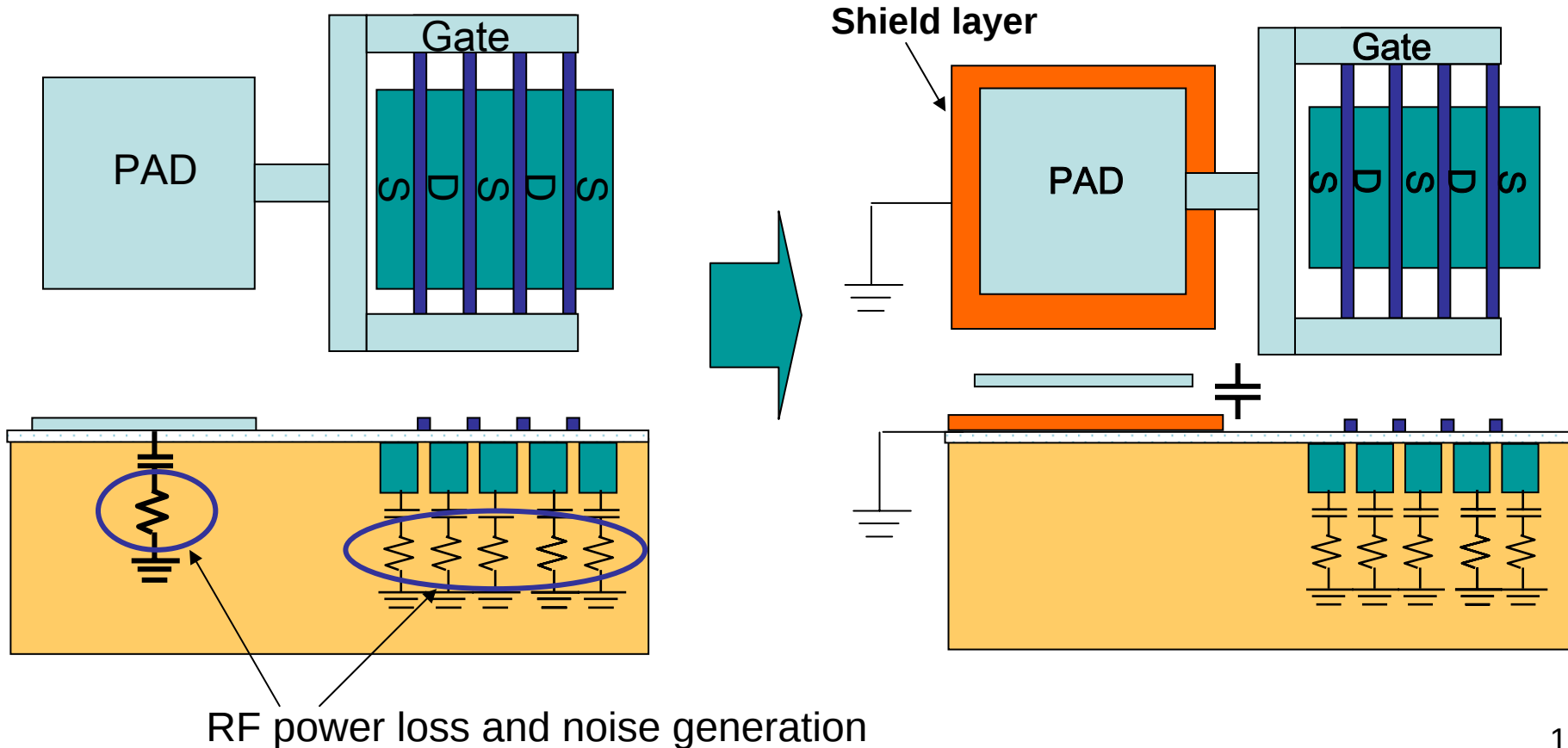
$$\omega_0 = \frac{1}{\sqrt{LC}} \quad r_0 = Q\omega_0 L = \frac{Q}{\omega_0 C}$$

Substrate effect

Substrate should be treated as resistive network.

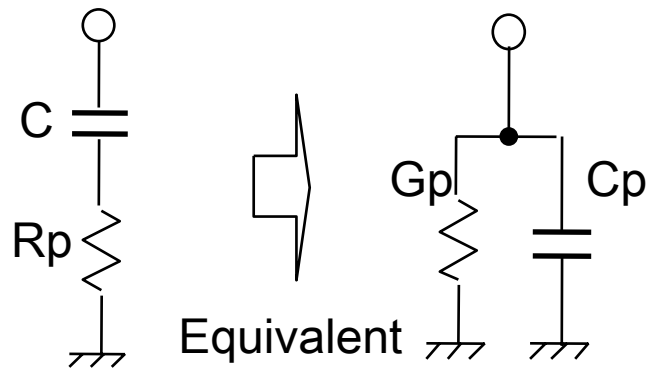
This substrate resistance causes RF power loss and noise generation.

Shielding can reduce this effect.



Power loss in substrate

Very low resistance or high resistance realizes low power loss.



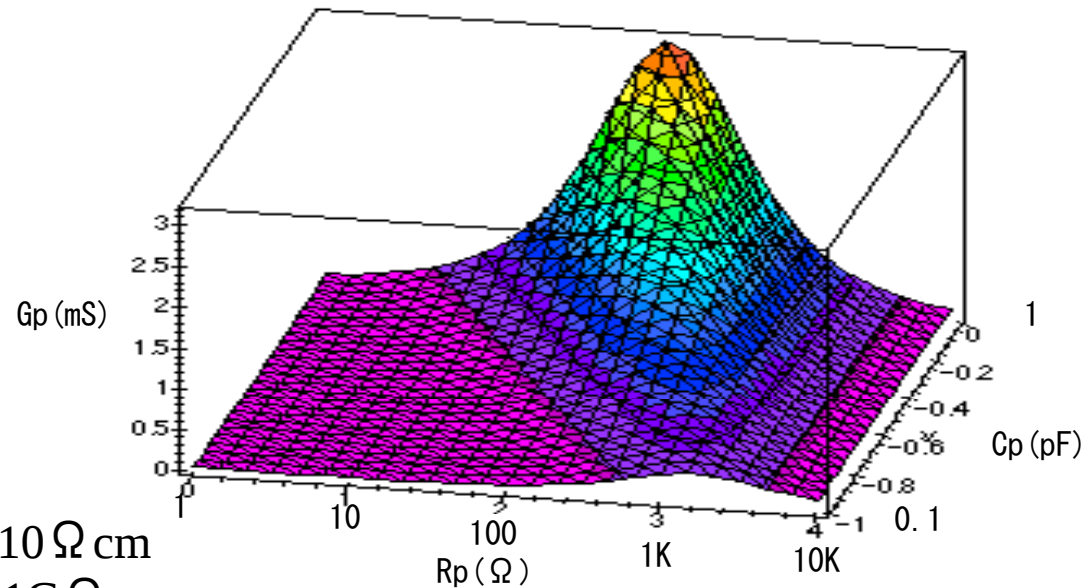
Higher C and moderate R_{sub} results in higher power loss.

$$G_p = \frac{1}{R_p} \cdot \frac{\left(\frac{\omega}{\omega_p} \right)^2}{1 + \left(\frac{\omega}{\omega_p} \right)^2}$$

$$C_p = C \cdot \frac{1}{1 + \left(\frac{\omega}{\omega_p} \right)^2}$$

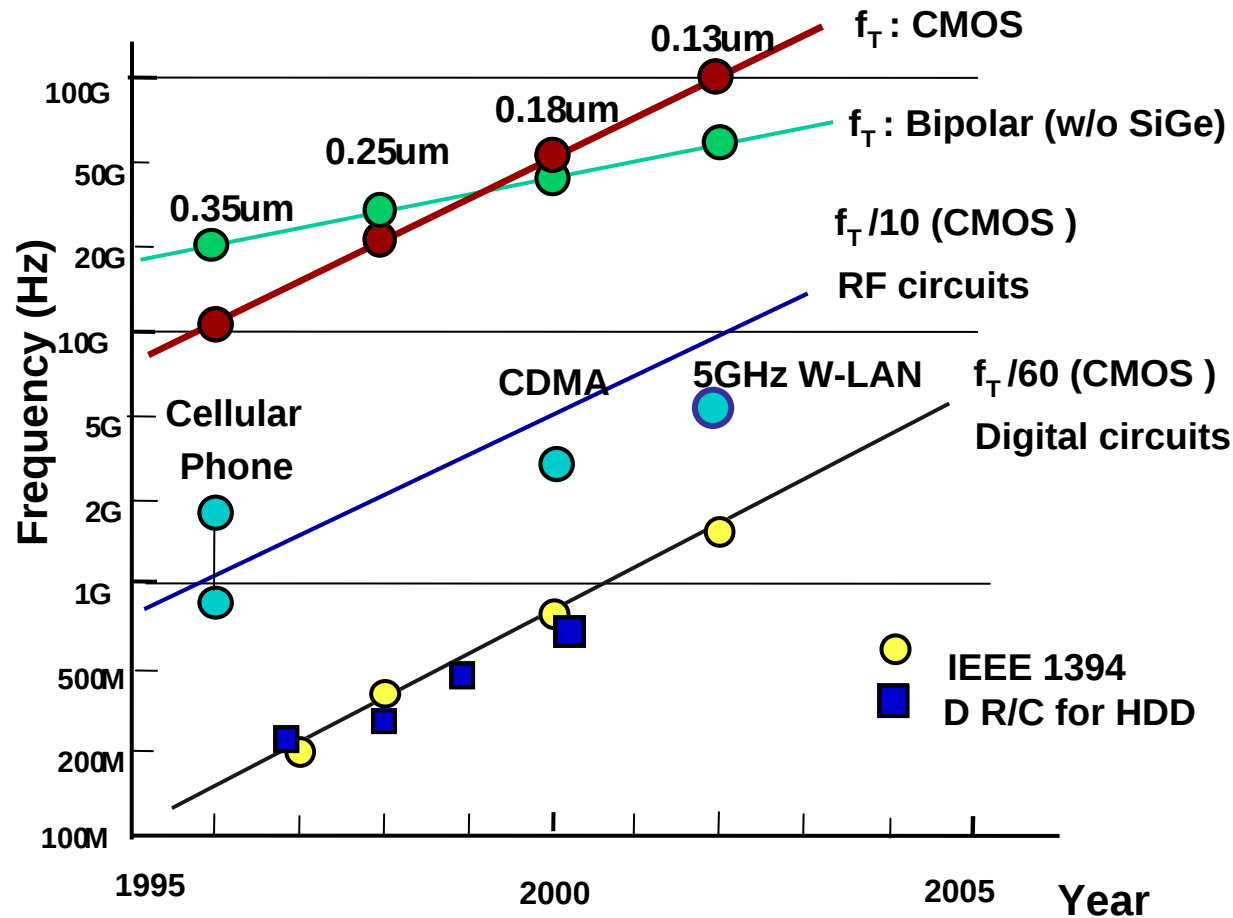
$$\omega_p = \frac{1}{R_p C}$$

MOS: $10 \Omega \text{ cm}$
GaAs: $1 \text{ G} \Omega \text{ cm}$



GHz operation by CMOS

The cutoff frequency of MOS becomes higher than that of Bipolar. Over several GHz operations have attained in CMOS technology

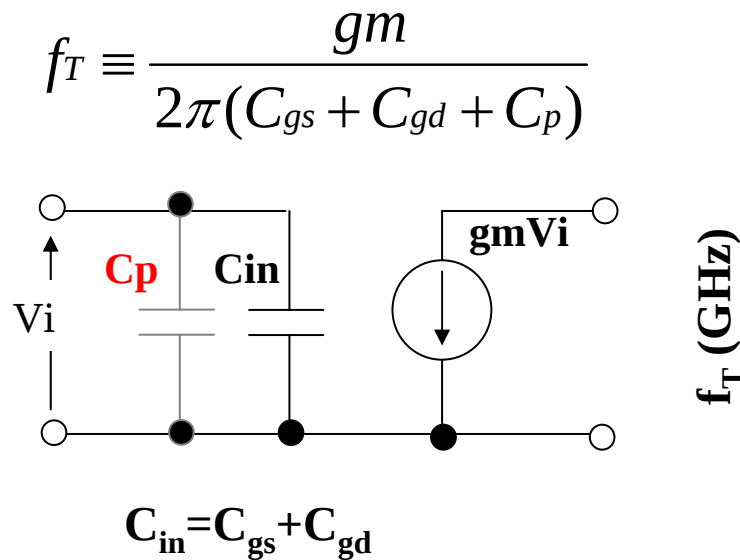


$$f_T \equiv \frac{gm}{2\pi C_{in}}$$

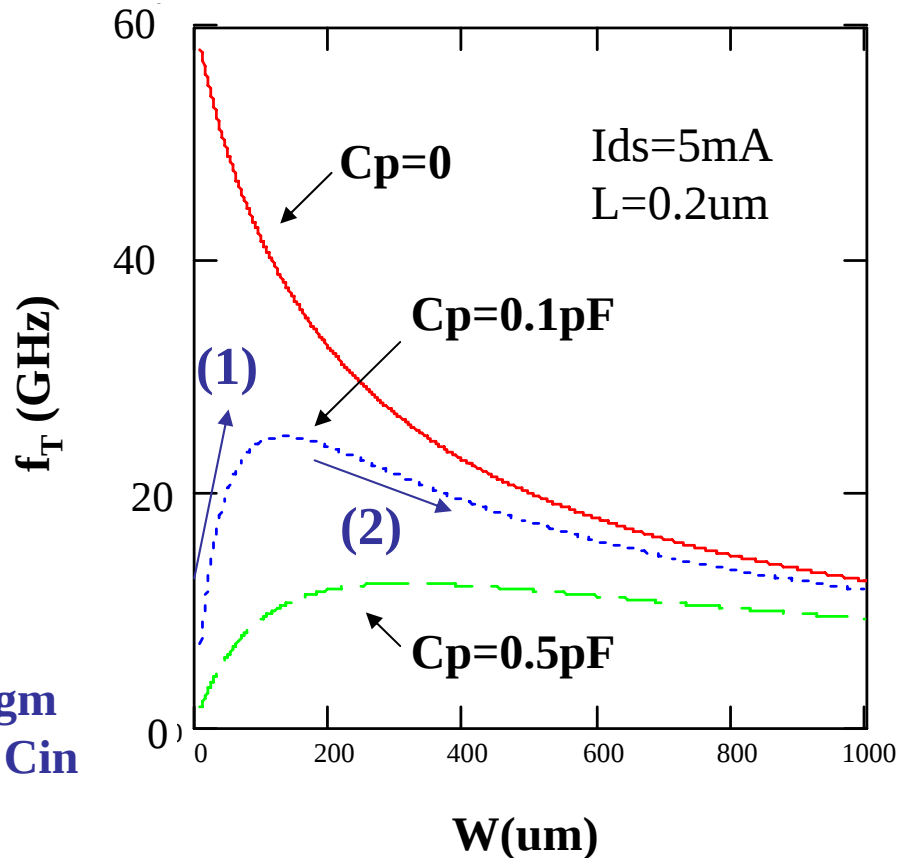
$$f_{Tpeak} \approx \frac{V_{sat}}{2\pi L_{eff}}$$

Effect of parasitic capacitance to f_T

f_T of actual circuit is reduced by a parasitic capacitance.
There is an optimum gate width to obtain highest f_T .



Region(1); Increased by increasing gm
Region(2); Decreased by increasing C_{in}



f_T : MOS vs. Bipolar

Even if f_T of MOS is the same as that of Bipolar,
 f_T of MOS is easily lowered by a parasitic capacitance.
Because, g_m of MOS is $\frac{1}{2}$ to $\frac{1}{4}$ of that of Bipolar at the same current.
Small parasitic capacitance is a key for RF CMOS design.

MOS

$$g_m \equiv \frac{I_{ds}}{\left(\frac{V_{eff}}{2}\right)}$$

$$V_{eff\ min} = 2nU_T \quad n: 1.4$$

$V_{eff}/2$: 50-100mV
(actual ckt.)

$$f_T \equiv \frac{g_m}{2\pi C_{in}}$$

Bipolar

$$g_m \equiv \frac{I_C}{U_T}$$

$$U_T \equiv \frac{kT}{q} \approx 26mV$$

$$g_{m_{CMOS}} < \frac{1}{2}, \frac{1}{4} g_{m_{Bip}}$$

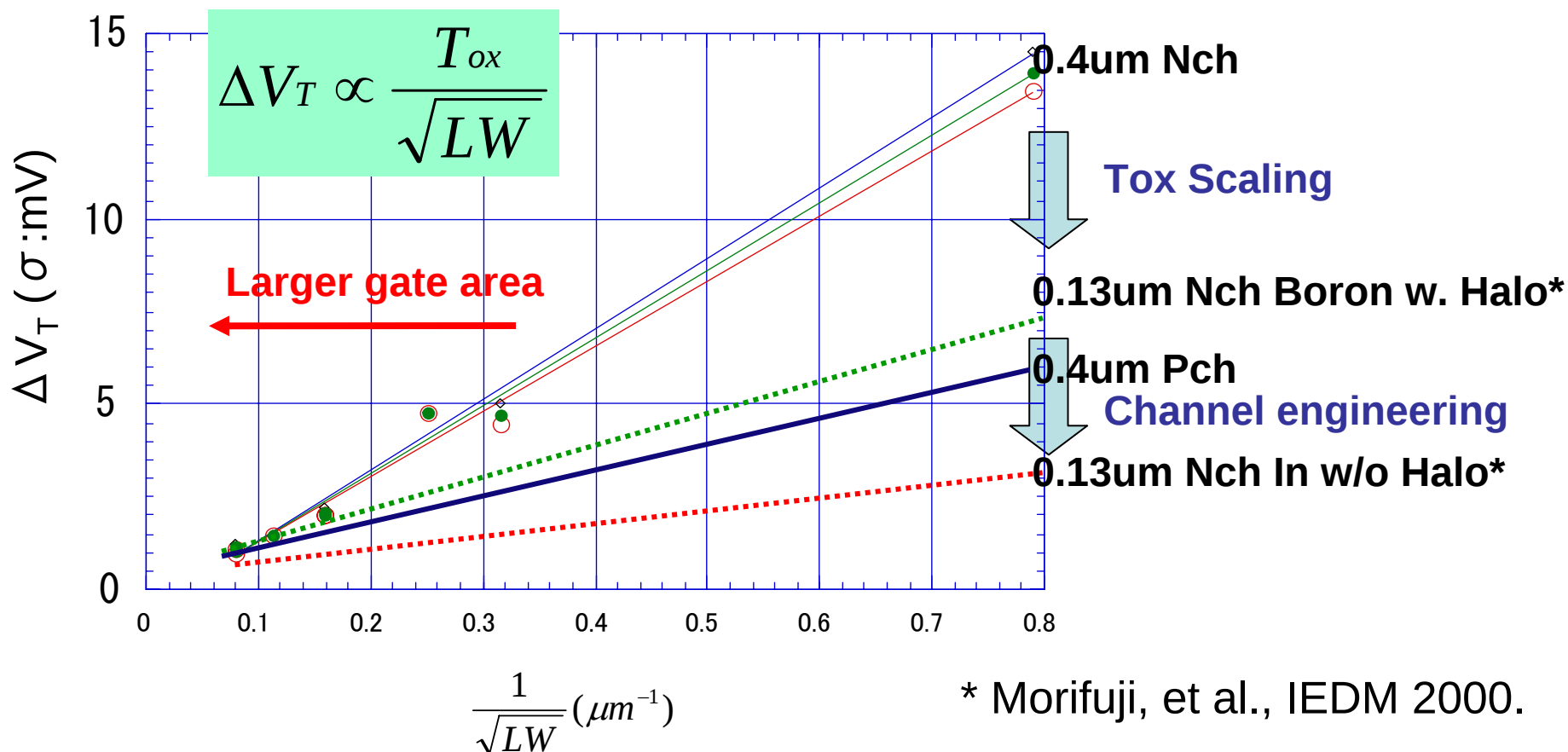
(Same operating current)

$$C_{in_{CMOS}} < \frac{1}{2}, \frac{1}{4} C_{in_{Bip}}$$

(Same f_T)

V_T mismatch

V_T mismatch degrades accuracy; ADC, OP amp, and Mixer.
Larger gate area is needed for small V_T mismatch.
Scaling and proper channel structure improves mismatch.

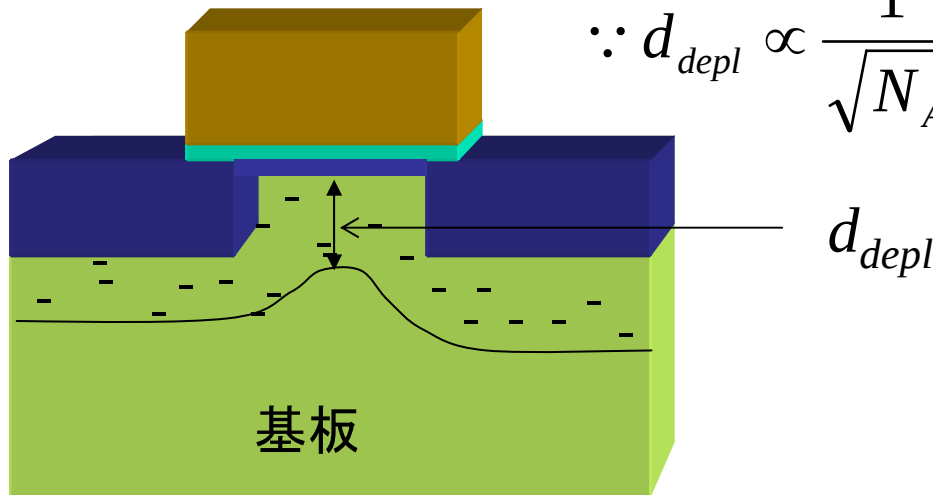


V_T mismatch: Fluctuation of doping

Courtesy of Prof. Taniguchi, Osaka Univ.

$$\Delta V_T = \frac{\Delta Q_{depl}}{C_{ox}} = At_{ox} \frac{\sqrt{LWd_{depl}N_A}}{LW} = A't_{ox} \frac{\sqrt[4]{N_A}}{\sqrt{LW}} \approx A_{VT} \frac{t_{ox}}{\sqrt{LW}}$$

$$\because d_{depl} \propto \frac{1}{\sqrt{N_A}}$$



$$A_{VT} = 1V$$



$$L = W = 0.25\mu m, \quad t_{ox} = 5nm$$

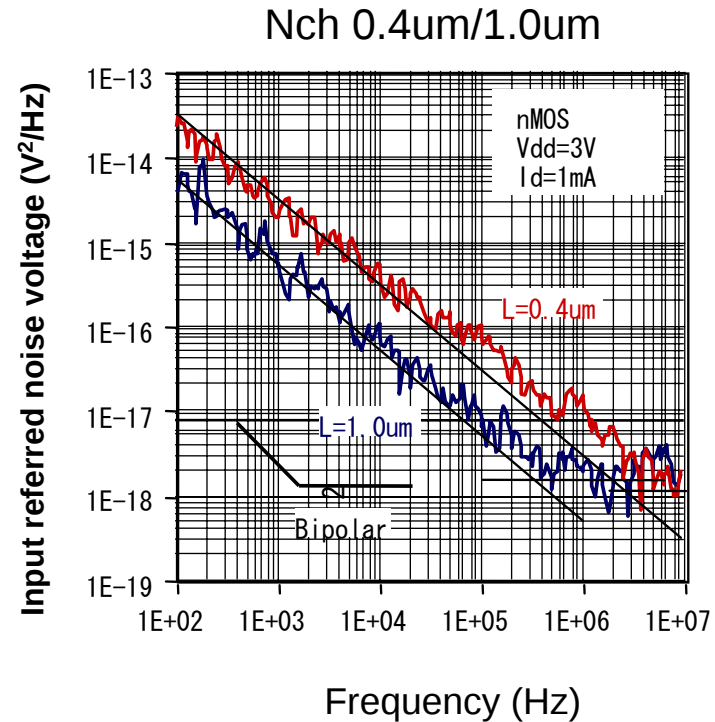
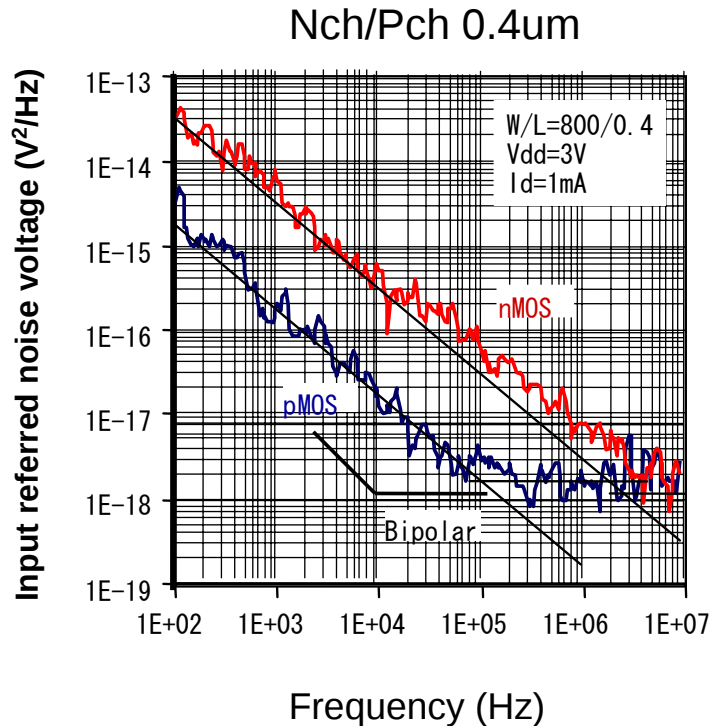
$$\underline{\Delta V_T = 20mV}$$

T.Mizuno, J.Okamura and A.Toriumi, "Experimental study of threshold voltage fluctuation due to statistical variation of channel dopant number in MOSFETs," IEEE Trans. On Electron Devices, ED-41, 2216 (1994)

1/f noise

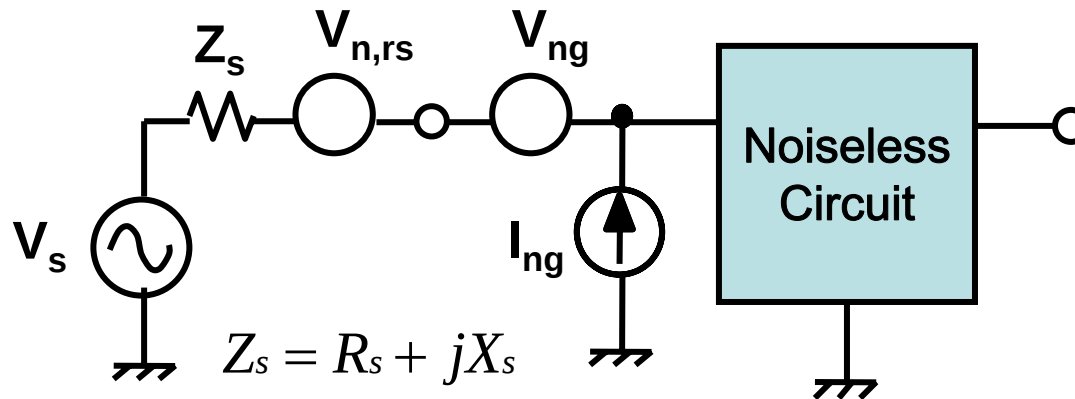
1/f noise of MOS is larger than that of bipolar.
For the lower 1/f noise, the larger gate area is needed.

$$V_{nf}^2 = \frac{S_{vf}}{LW} \frac{\Delta f}{f}, \quad S_{vf} \propto T_{ox}^2$$



Noise figure: General

The lower R_{nv} and G_{ni} realizes the better for a lower noise figure.



$$\overline{V_{ng}^2} = 4kTR_{nv}, \quad \overline{I_{ng}^2} = 4kTG_{ni}$$

$$F = \frac{\overline{V_{n,rs}^2} + \overline{(V_{ng} + Z_s I_{ng})^2}}{\overline{V_{n,rs}^2}} = 1 + \frac{R_{nv}}{R_s} + \frac{|Z_s|^2 G_{ni}}{R_s} \approx 1 + \frac{R_{nv}}{R_s} + R_s G_{ni}$$

$$R_{sopt} = \frac{\overline{V_{ng}}}{\overline{I_{ng}}} = \sqrt{\frac{R_{nv}}{G_{ni}}}$$

$$F_{\min} \approx 1 + 2\sqrt{R_{nv}G_{ni}}$$

Noise figure: MOS transistor

$$F \approx 1 + \frac{R_{nv}}{R_s} + R_s G_{ni}$$

$$R_{nv} = R_g + R_{gs} \quad R_g = R_{sr} \frac{W_{tot}}{L} \frac{1}{3N^2} \quad R_{gs} \approx \frac{1}{5gm} \quad G_{ni} \approx \frac{gm}{5} \left(\frac{\omega_0}{\omega_T} \right)^2$$

$$F \approx 1 + \frac{1}{R_s 5gm} + R_s \frac{gm}{5} \left(\frac{\omega_0}{\omega_T} \right)^2 \quad R_{sopt} \approx \frac{1}{gm} \left(\frac{\omega_T}{\omega_0} \right) = \frac{1}{C_{gs} \omega_0}$$

$$F_{min} \approx 1 + 2 \frac{\omega_0}{\omega_T}$$

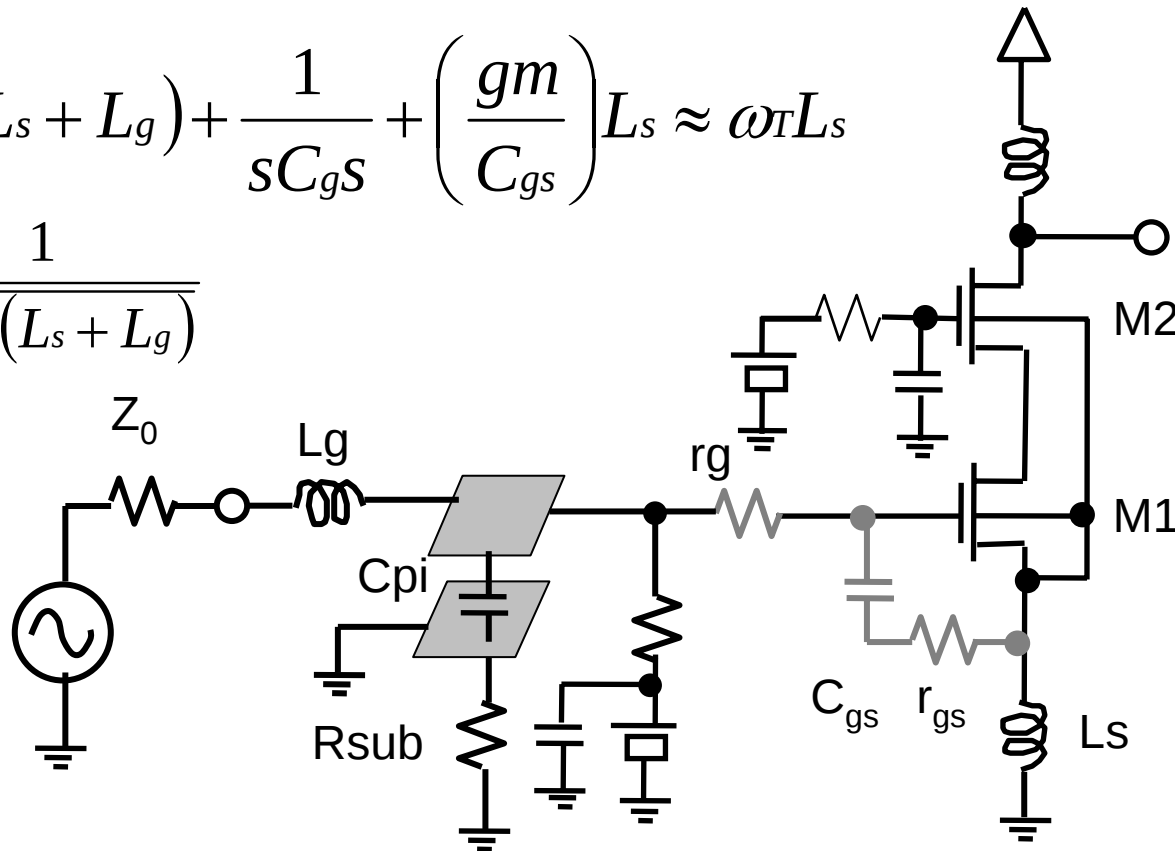
Low noise amplifier design

Narrowband LNA uses inductor degeneration for impedance matching.

Impedance matching

$$Z_{in} \approx s(L_s + L_g) + \frac{1}{sC_{gs}} + \left(\frac{gm}{C_{gs}} \right) L_s \approx \omega T L_s$$

$$\omega_0 = \frac{1}{\sqrt{C_{gs}(L_s + L_g)}}$$



Low NF design

$$F \approx 1 + \frac{r_{gs} + r_g}{Z_0} + 4\gamma gm Z_0 \left(\frac{\omega_0}{\omega_T} \right)^2 \approx 1 + \frac{r_{gs} + r_g}{Z_0}$$

$$r_{gs} \approx \frac{1}{5gm}$$

Low noise figure

1) Lower the gate resistance

Divide the gate or lower the gate sheet resistance

$$r_g = R_{sr} \frac{W_{tot}}{L} \frac{1}{3N^2}$$

2) Reduce substrate loss

Reduce parasitic capacitance

Use shield technique to the input bonding PAD.

Use high resistive substrate, if possible.

$$r_g = R_{sr} \frac{W_{tot}}{L}$$

R_{sr}: Sheet resistance

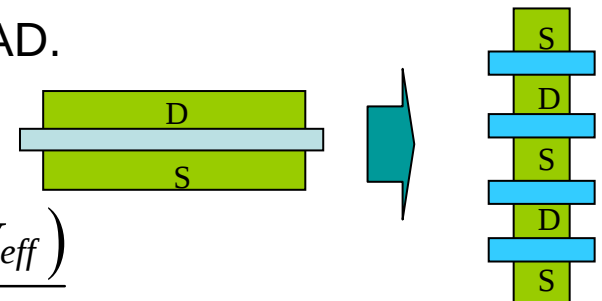
N: The # of division

Divide the gate

3) Increase drain current

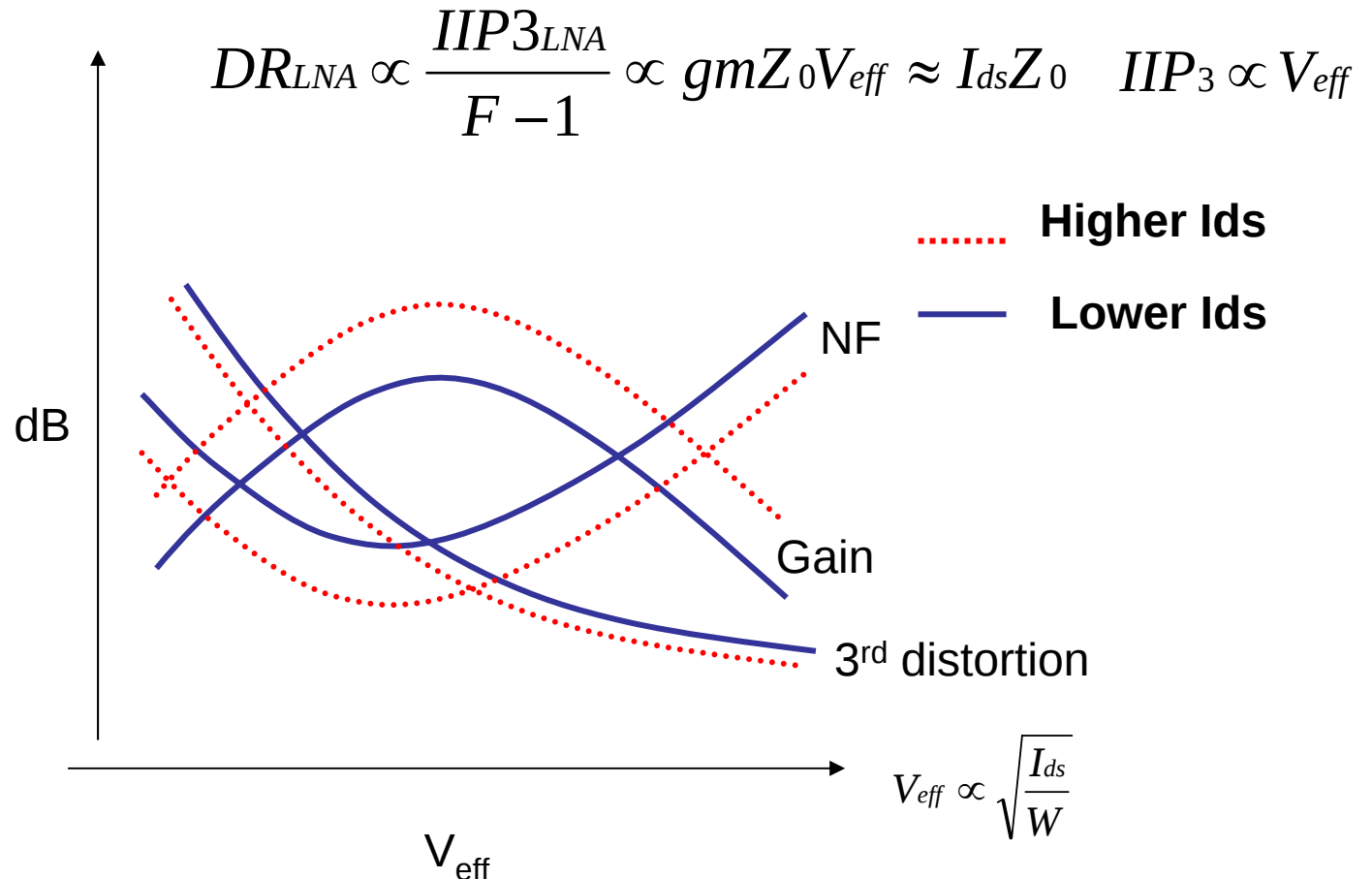
4) Increase Z_0 , if possible.

$$r_{gs} \approx \frac{1}{5gm} \approx \frac{(V_{eff})}{10I_{ds}}$$



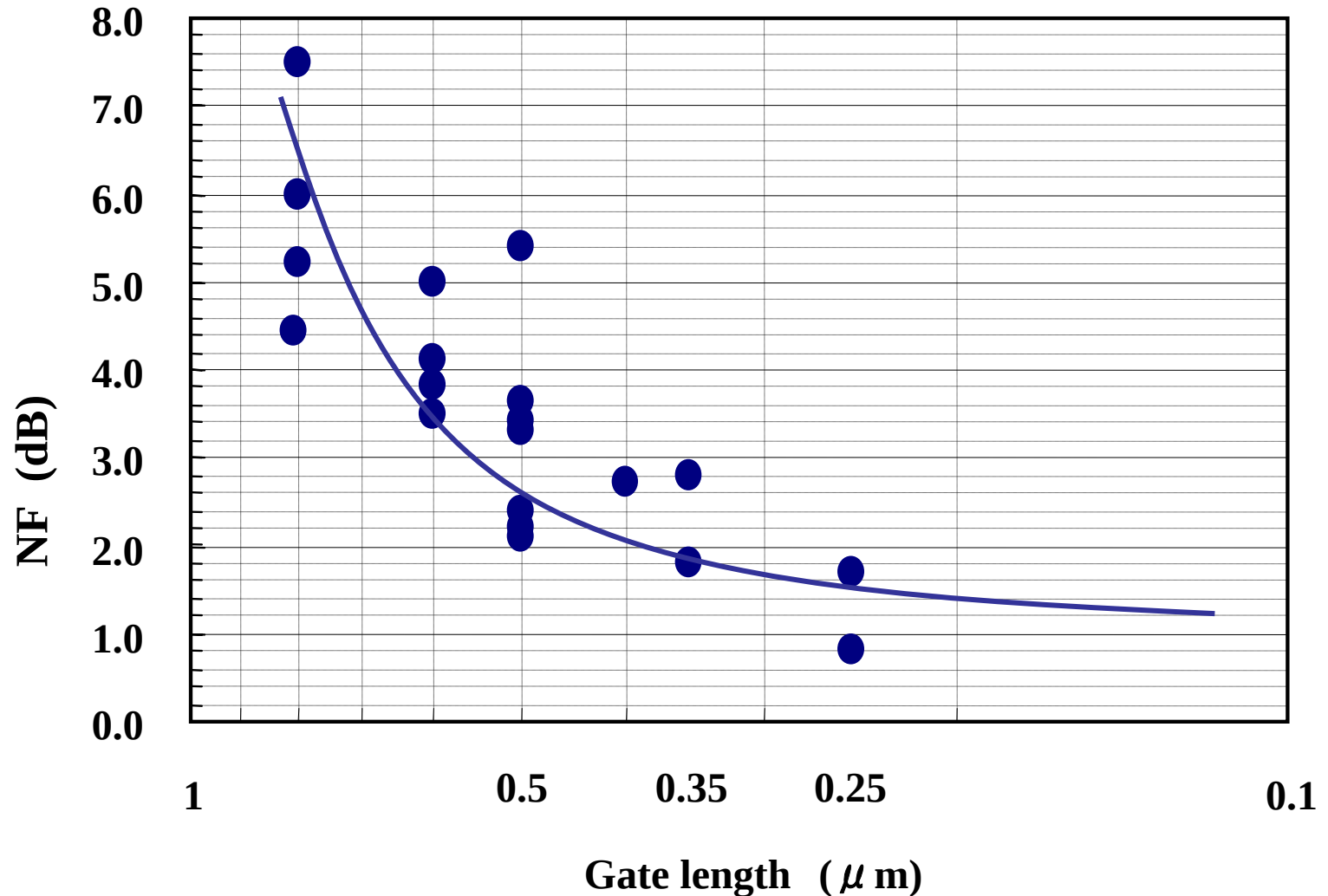
I_{ds} and V_{eff} optimization

Adjust the I_{ds} and V_{eff} for optimization of gain, noise and distortion.
Dynamic range of LNA is proportional to I_{ds} .



NF progress in MOS LNA

NF of MOS LNA is reaching 1dB.



Mixer

Mixer converts frequency, but image signal is converted to the same frequency.

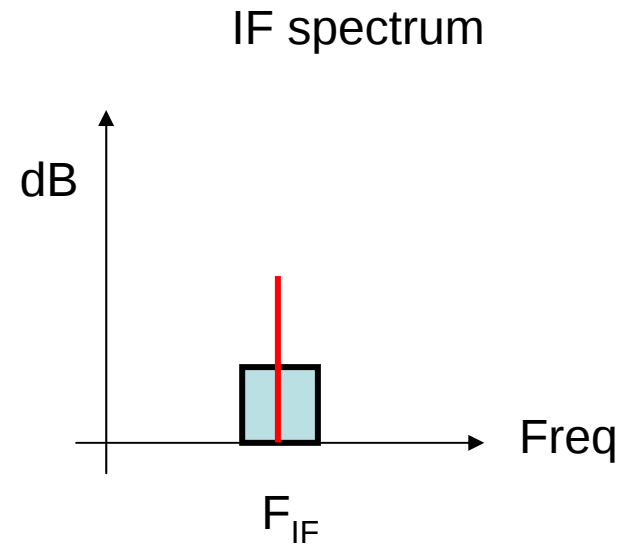
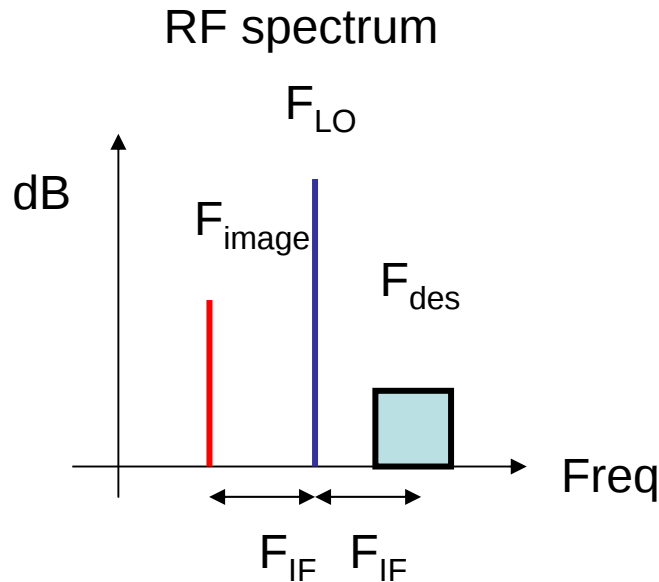
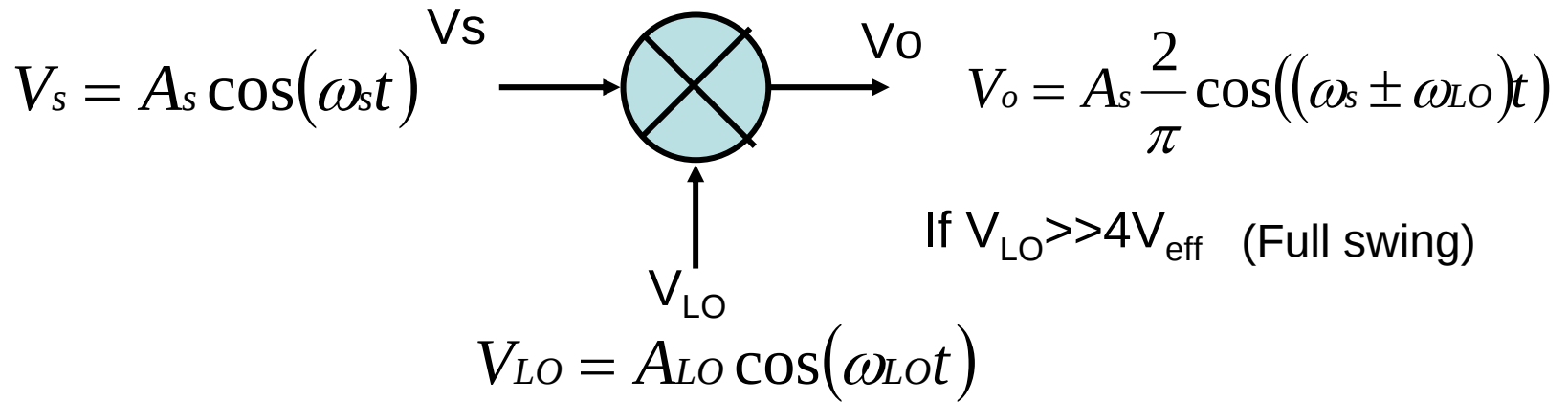
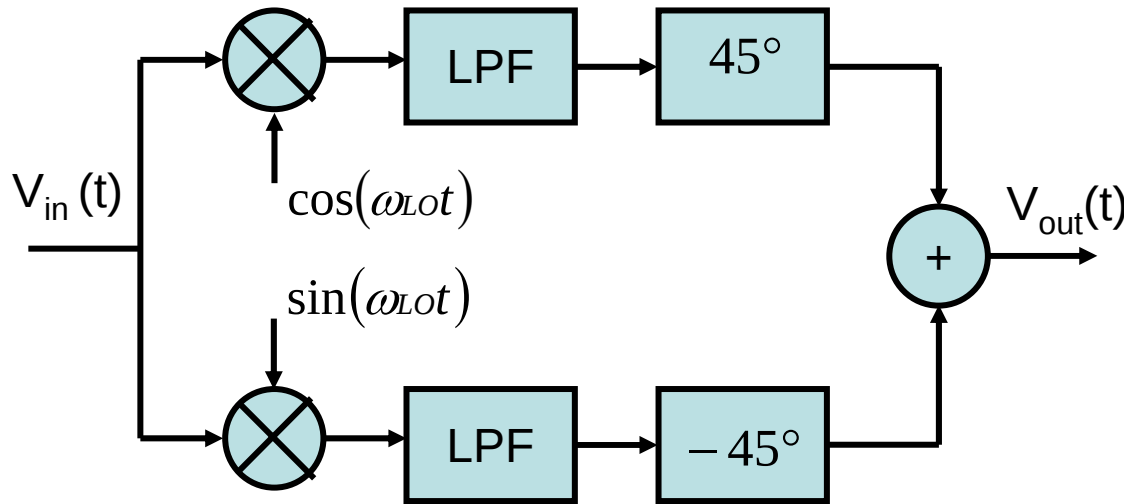


Image-reject mixers

The quadrature mixing realizes image-suppression.
Gain and phase matching is needed.



$$V_{in}(t) = A_{des} \cos(\omega_{dest}) + A_{im} \cos(\omega_{imt})$$

$$V_{out}(t) = A_{des} A_c \cos(\omega_{IFt}) + A_{im} A_c I_R \cos(\omega_{IFt})$$

A_c : Conversion gain, I_R : Image rejection

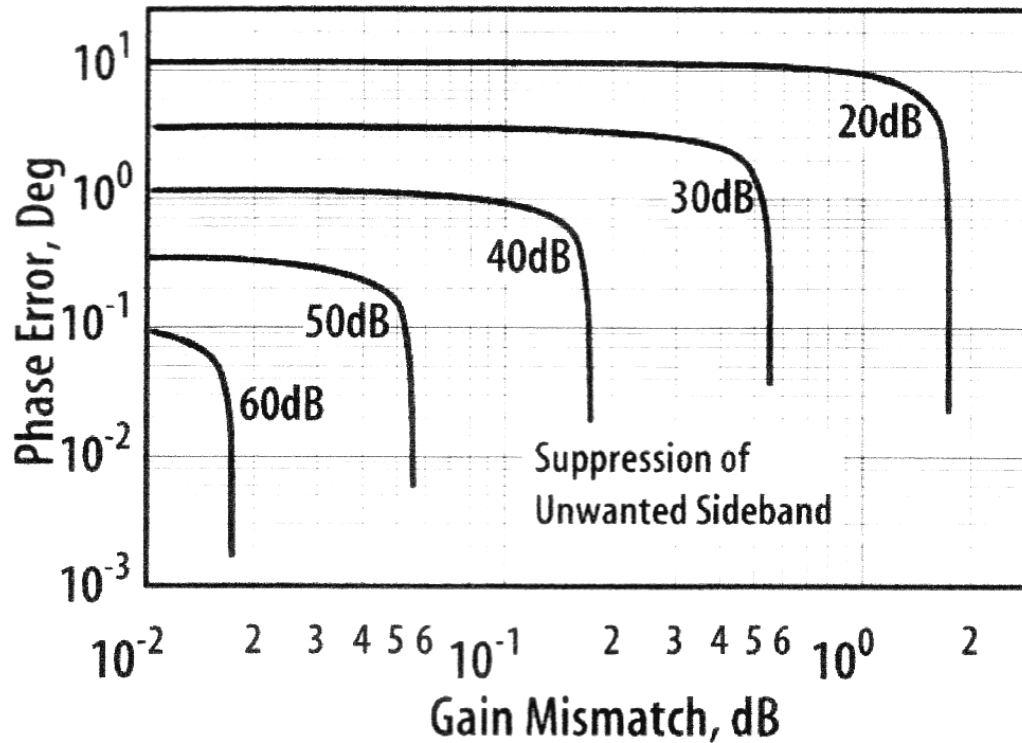
$I_R = 0$ if I/Q phase difference is 90° and Channel conversion gains are equal.

Gain mismatch and phase error

$$\frac{P_{spur}}{P_{desired}} = \frac{1 + \gamma^2 - 2\gamma \cos \phi}{1 + \gamma^2 + 2\gamma \cos \phi}$$

γ : Gain ratio

ϕ : Phase error



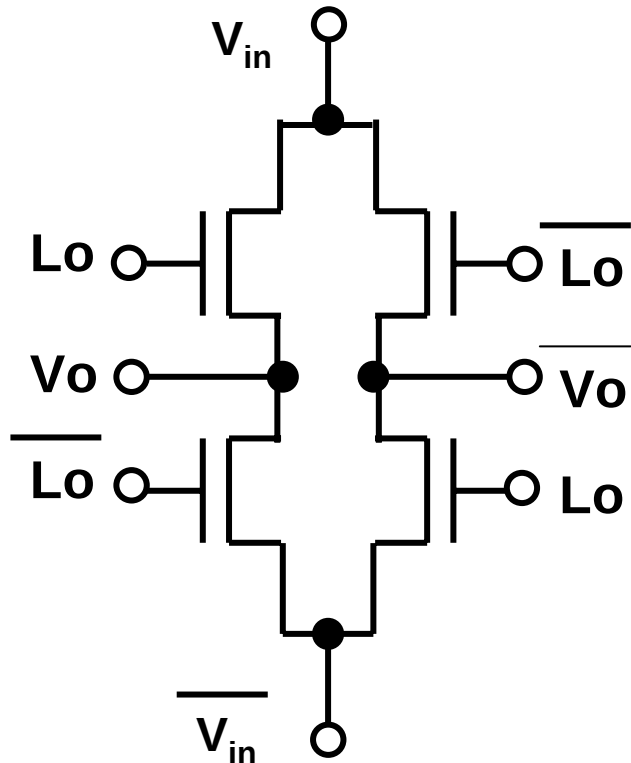
A. Rofougaran, et al.,
IEEE J.S.C. Vol.33, No.4,
April 1998. PP. 515-534.

Passive FET mixer

MOS can realize a passive mixer easily.

Ultimately low power, but take care of isolation.

Passive FET mixer

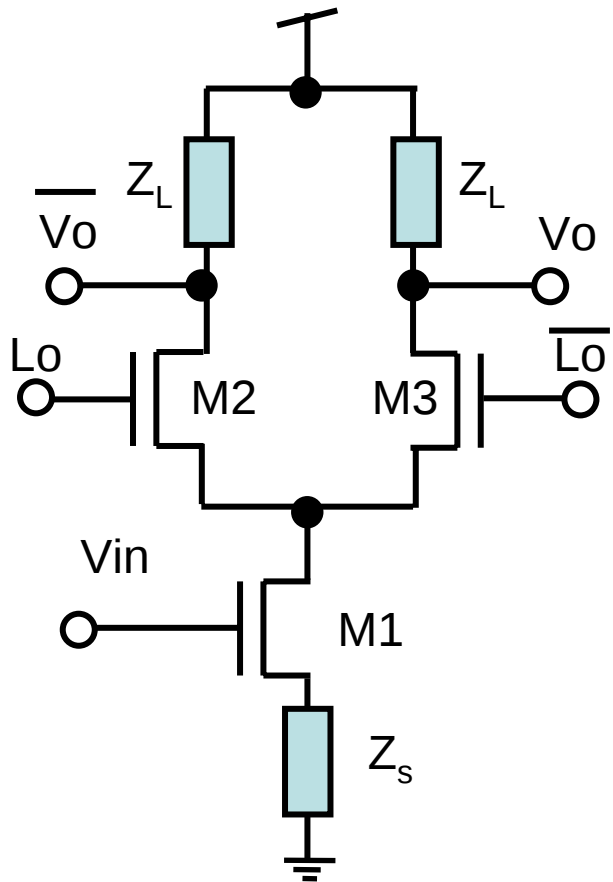


Low power
High linearity
No $1/f$ noise

No conversion gain
No isolation, Bi-directional

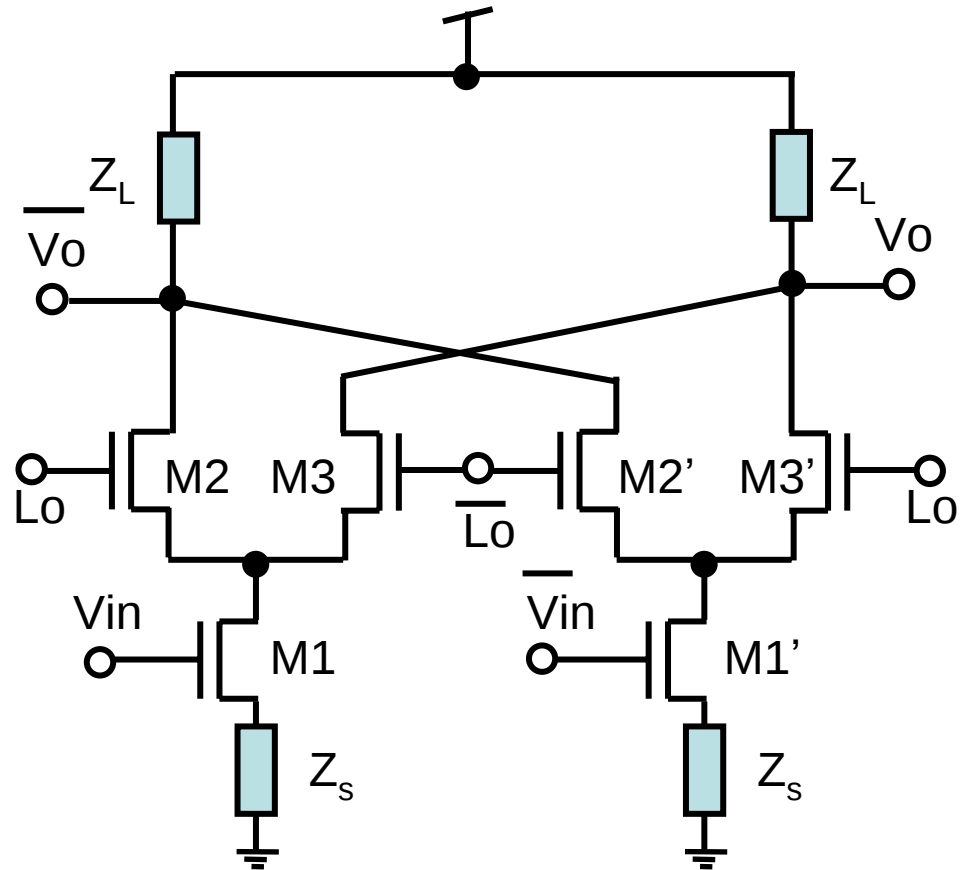
Active mixers

Single balanced mixer



Double balanced mixer

Very small direct feed through and even order distortion



Active mixer design

The larger I_{ds} is needed for high dynamic range and shorter switching time for low $1/f$ noise.

Mixer gain $G_{mix} = \frac{2}{\pi} gm_1 Z_L, \text{ or } = \frac{2}{\pi} \frac{Z_L}{Z_s}$ when Z_s is used

Thermal noise $v_{on}^2 = 8kTR_L \left(1 + \frac{2\gamma R_L}{\pi A_{LO}} + \gamma gm_1 R_L \right) \approx 8kTR_L^2 \gamma gm_1$ R_L : Resistive component in Z_L

$$SSBv_{in}^2 = \frac{v_{on}^2}{\left(\frac{2}{\pi} gm_1 R_L \right)^2} \approx 2\pi^2 kT \frac{\gamma}{gm_1} \cong \pi^2 kT \gamma \frac{V_{eff}}{I_{ds}}$$

$$IIP3 \approx V_{eff}$$

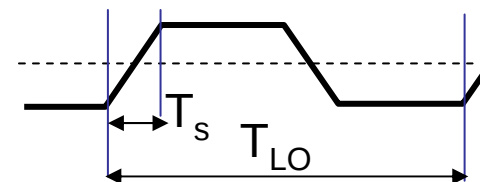
A larger dynamic range needs larger current

1/F noise

1) Switch transistor (M2, M3)

$$V_{n,o} = \frac{4Ts}{T_{LO}} V_{n,sw}$$

$$V_{n,sw}^2 \approx \frac{1}{WL} \propto \frac{1}{C_{gs}}$$



Phase modulation

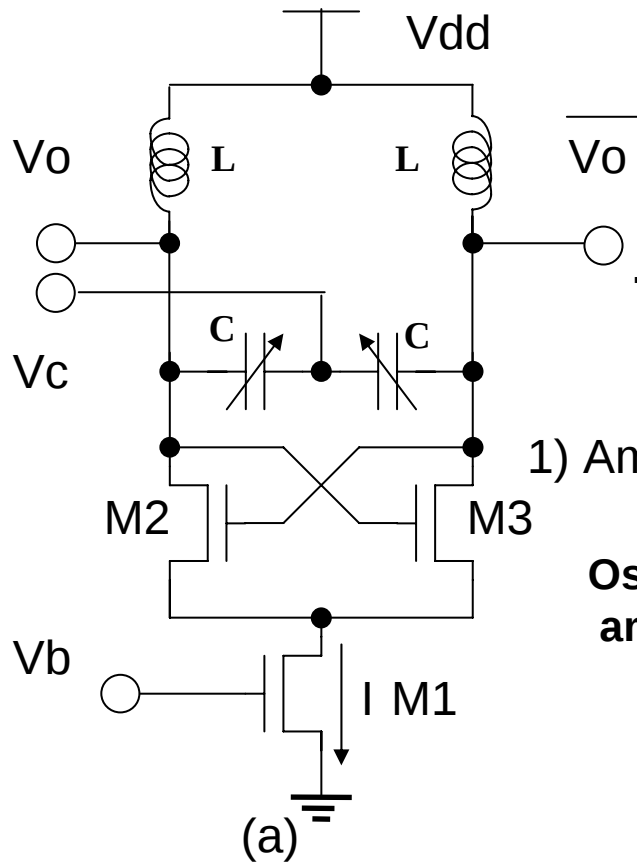
Shorter switching time or larger T_s/T_{LO} ratio

2) Load transistors

Directly produces

Oscillator

There is an optimum I_{ds} for low phase noise.



1) Amplitude condition

Oscillation
amplitude

$$V_{osc} = \frac{4I r_o}{\pi}$$

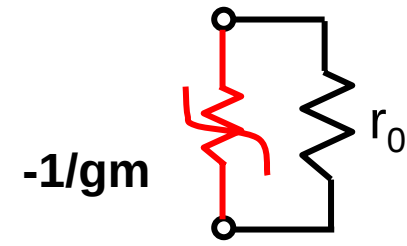
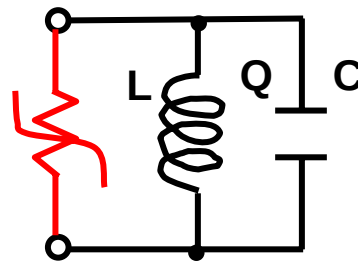
Headroom
limit

$2V_{dd}$

$$I_{opt} = \frac{\pi V_{dd}}{2r_o} = \frac{\pi V_{dd} \omega_o C}{Q}$$

2) Oscillation condition

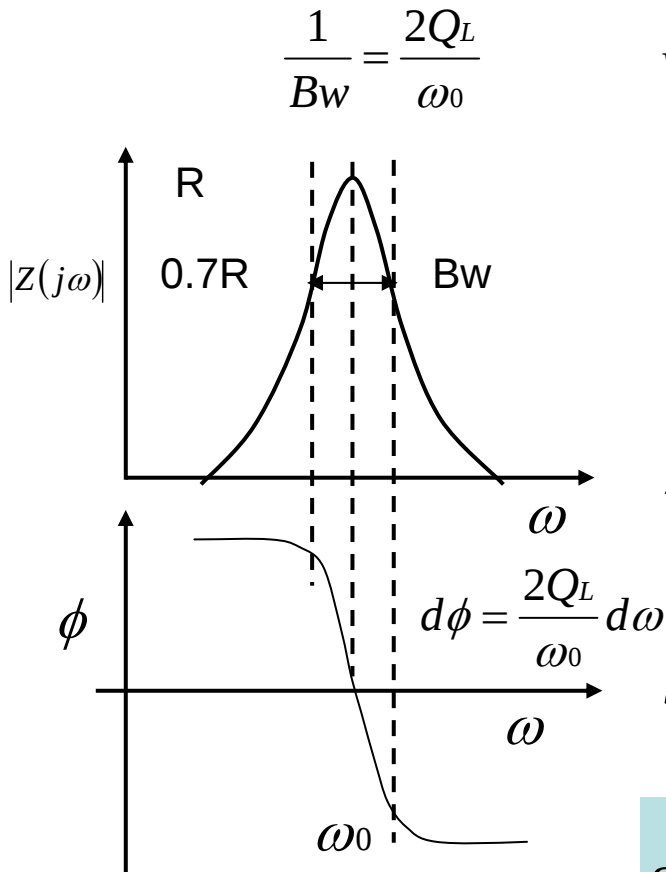
$$gm_{2,3} > \frac{2}{r_o}, \quad I > \frac{\omega_o C V_{eff,2,3}}{Q}$$



$$r_o = Q \omega_o L = \frac{Q}{\omega_o C}$$

Phase noise of oscillator

Phase-frequency relation and resonator characteristics determine phase noise.



$$v(t) = A \cos[\omega_0 t + \phi(t)]$$

$$\omega_m = \frac{d\phi}{dt} = j\omega\phi$$

$$S_\omega(\omega_m) = \omega_m^2 S_\phi(\omega_m)$$

$$\Delta\theta = \frac{\omega_m}{Bw} = \frac{2Q_L}{\omega_0} \omega_m$$

$$S_\omega(\omega_m) = \left(\frac{\omega_0}{2Q_L} \right)^2 S_{\Delta\theta}(\omega_m) \quad \omega_m < Bw$$

ω_m : Offset angular frequency

$S_\omega(\omega_m)$: Noise spectrum density on offset angular frequency

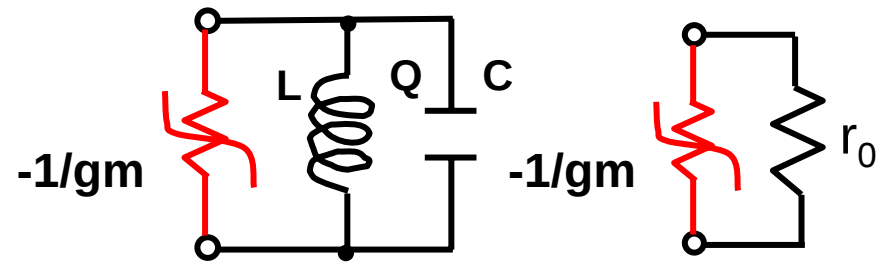
$S_\phi(\omega_m)$: Noise spectrum density on phase

$\Delta\theta$ Phase error between in and out

$S_{\Delta\theta}(\omega_m)$: Noise spectrum density on phase error

$$S_\phi(\omega_m) = \left(\frac{\omega_0}{2Q_L} \right)^2 \frac{1}{\omega_m^2} S_{\Delta\theta}(\omega_m) = \left(\frac{\omega_0}{2Q_L \omega_m} \right)^2 S_{\Delta\theta}(\omega_m)$$

Phase noise of oscillator

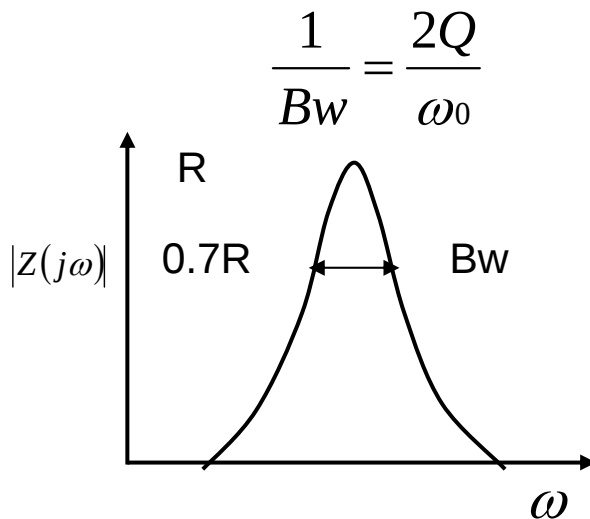


$$Z(\omega_0 + \omega_m) \approx j \frac{\omega_0 L}{2 \frac{\omega_m}{\omega_0}} \quad \omega_m \ll \omega_0$$

(Filter action)

$$Q = \frac{r_0}{\omega_0 L}$$

$$|Z(\omega_0 + \omega_m)| \approx \frac{r_0 \omega_0}{2Q \omega_m}$$



$$\frac{\overline{v_n^2}}{\Delta f} = \frac{\overline{i_n^2}}{\Delta f} \cdot |Z|^2 = 4kTr_0 \left(\frac{\omega_0}{2Q\omega_m} \right)^2$$

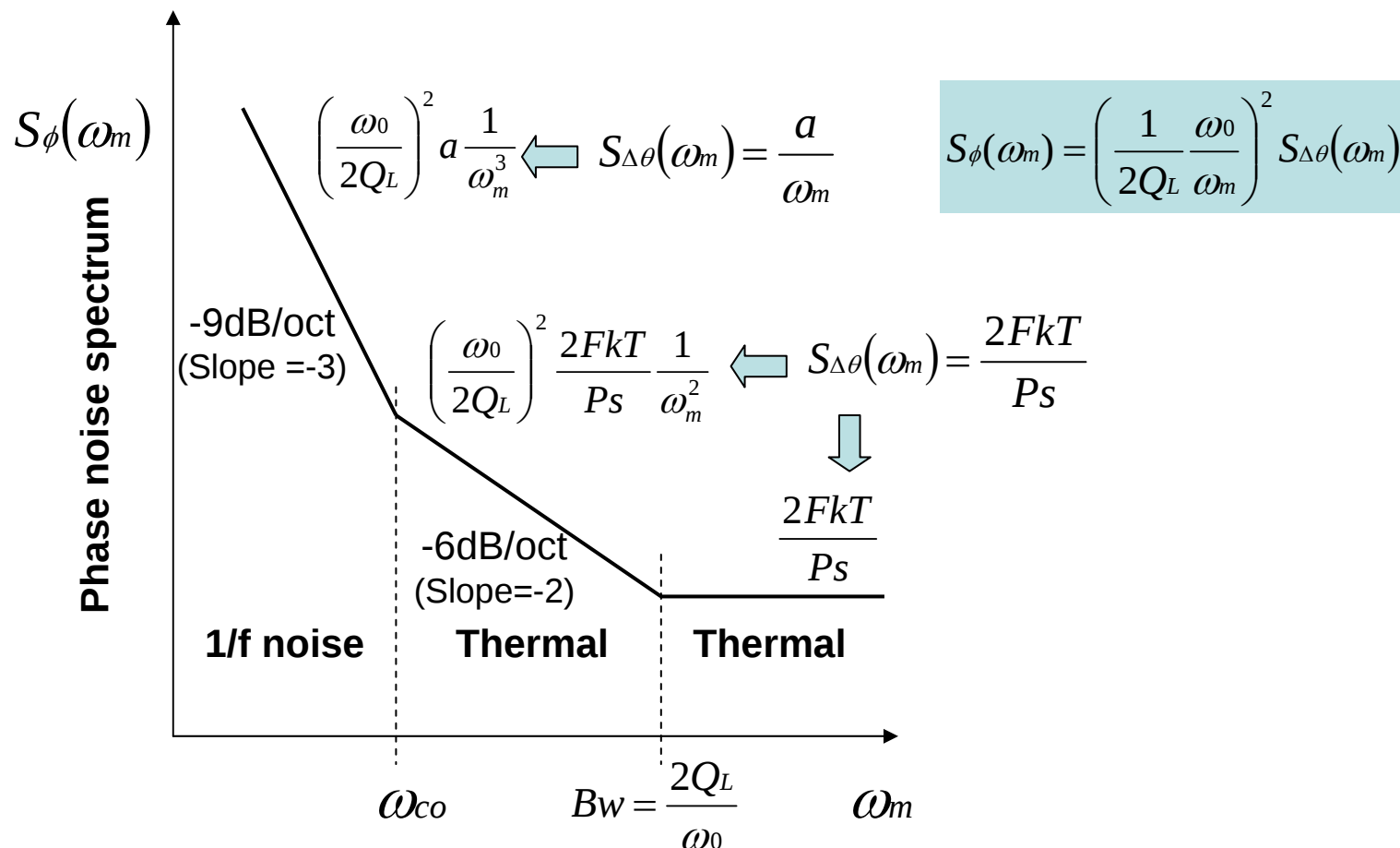
Noise spectrum density

$$L\{\omega_m\} = 10 \log \left[\frac{2kT}{P_{sig}} \cdot \left(\frac{\omega_0}{2Q\omega_m} \right)^2 \right]$$

Phase noise

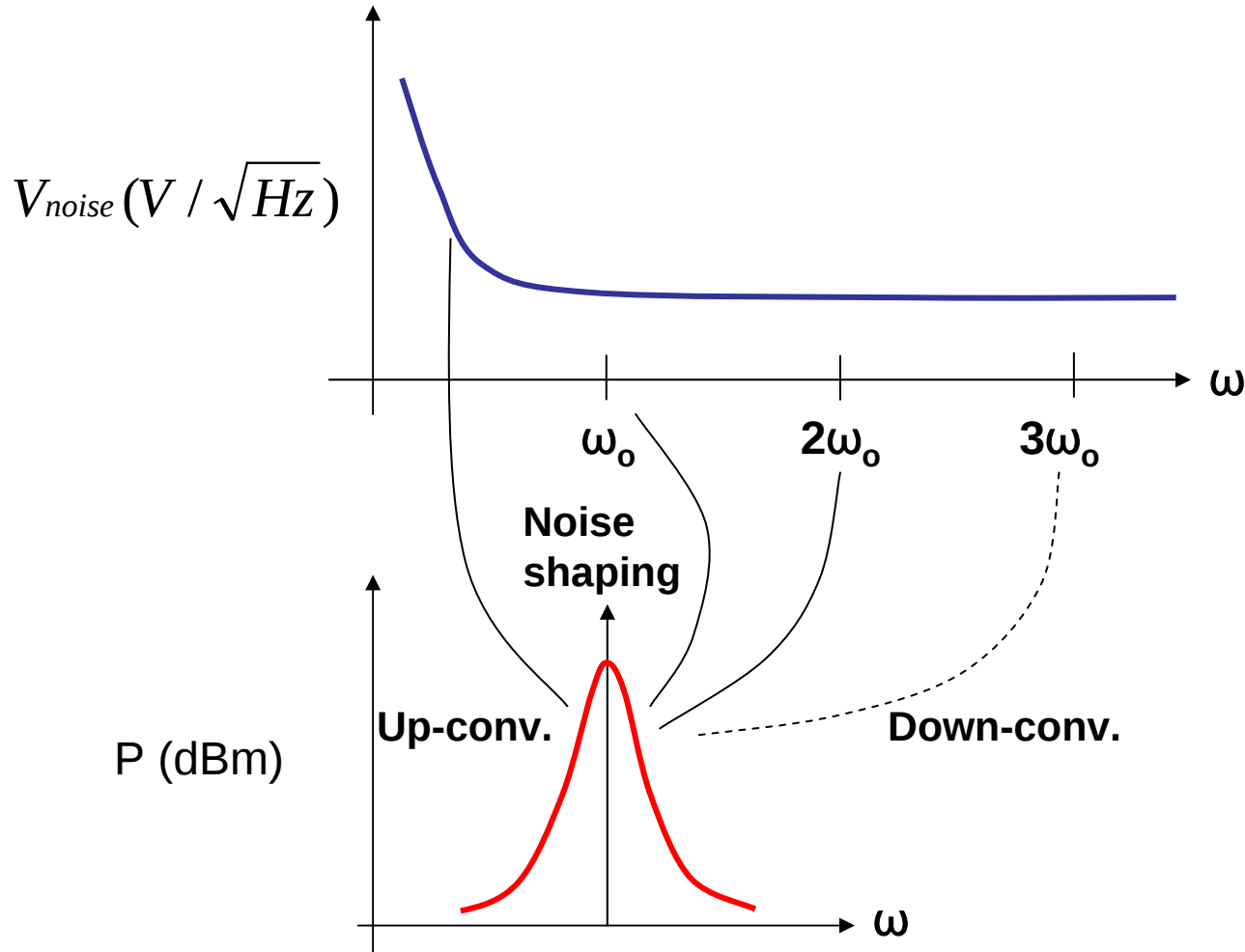
Frequency characteristics of Phase noise in oscillator

1/f noise and thermal noise is converted to 1/f³ and 1/f², respectively.



Up and down converted noise

Noises around $N \cdot f_o$ are up and down converted to f_o .



FoM and minimum phase noise

FoM is basically proportional to Q^2 .

$$FoM = \left(\frac{f_o}{f_m} \right)^2 \frac{1}{L(f_m) V_{dd} I}$$

Fm: Offset frequency
L(fm): Phase noise at offset freq.

$$L(f_m) = \frac{1}{2} \cdot \frac{1}{Q^2} \cdot \left(\frac{f_o}{f_m} \right)^2 \cdot \frac{FkT}{P_{RF}} = \frac{1}{2} \cdot \frac{1}{Q^2} \cdot \left(\frac{f_o}{f_m} \right)^2 \cdot \frac{FkT}{\left(\frac{V_o^2}{2r_o} \right)}$$

F: Noise factor

$$F = 2 + \frac{8\gamma r_o I}{\pi V_o} + \gamma \frac{8}{9} r_o \cdot g_{m1} \quad I_{opt} = \frac{\pi V_{dd}}{2r_o} = \frac{\pi V_{dd} \omega_o C}{Q} = \frac{\pi V_{dd}}{2Q \omega_o L_{ind}}$$

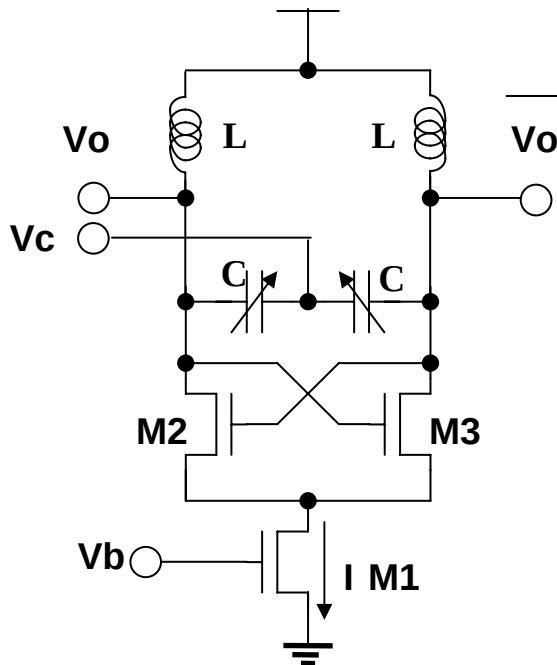
$$FoM = \frac{4}{\pi} \frac{Q^2}{kT} \frac{1}{2 + 4\gamma + \frac{32}{9} \gamma \pi \frac{V_{dd}}{V_{eff,1}}} \propto Q^2 \quad \text{at } I_{opt}$$

Oscillator design

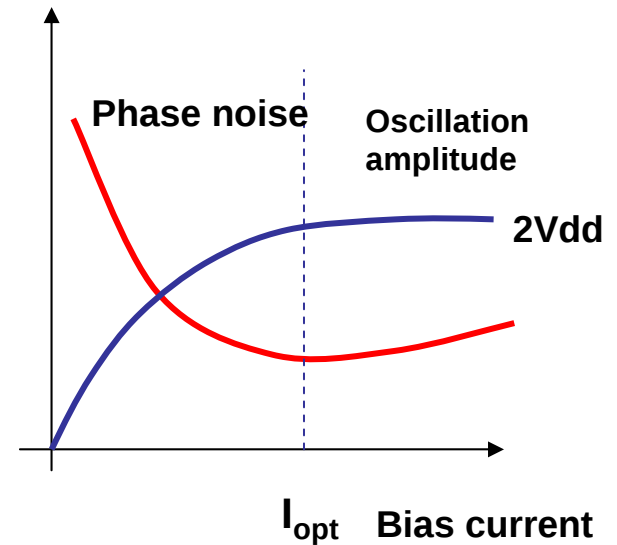
Careful optimization reduces the oscillator phase noise.

$$L_{\min}(f_m) = kT \cdot \frac{\gamma}{V_{dd}} \cdot \frac{\omega_o L_{ind}}{2Q} \cdot \left(\frac{1}{V_{dd}} + \frac{2}{V_{eff,1}} \right) \left(\frac{f_o}{f_m} \right)^2$$

$$L_{\min}(f_m) = kT \cdot \frac{\gamma}{2I_{opt}} \cdot \frac{1}{2Q^2} \cdot \left(\frac{1}{V_{dd}} + \frac{2}{V_{eff,1}} \right) \left(\frac{f_o}{f_m} \right)^2$$



$$I_{opt} = \frac{\pi V_{dd}}{2r_o} = \frac{\pi V_{dd} \omega_o C}{Q} = \frac{\pi V_{dd}}{2Q \omega_o L_{ind}}$$



Larger V_{dd}

Large V_{eff1} , but take care of V_o reduction

Large L_1 , W_1 to reduce $1/f$ noise

Enough W/L for M2, M3

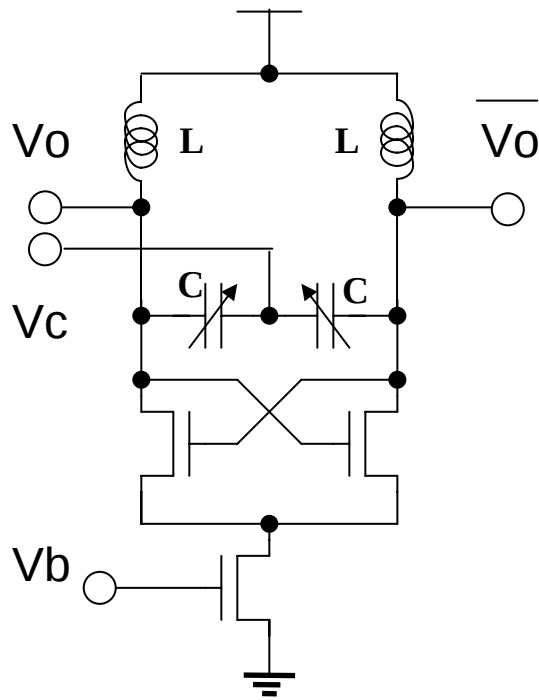
Higher Q

Larger QL_{ind} for Lower I_{opt}

CMOS oscillator circuits

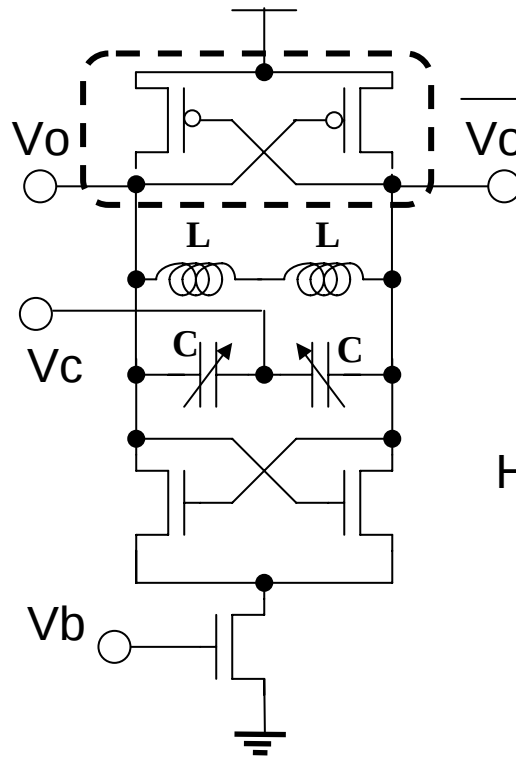
E. Hegazi, ISSCC 2001

Basic



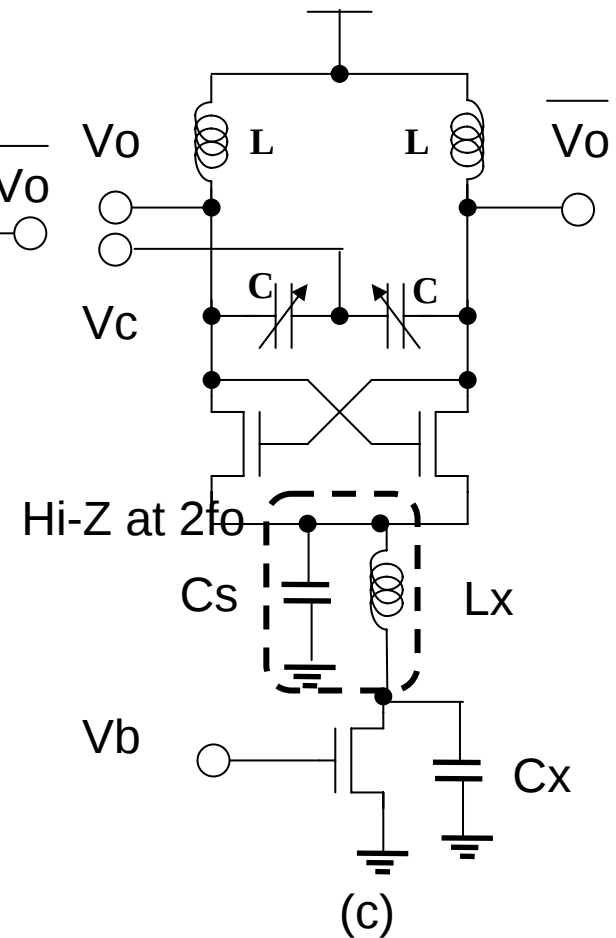
(a)

Low power (gm is higher)



(b)

Low noise by filtering



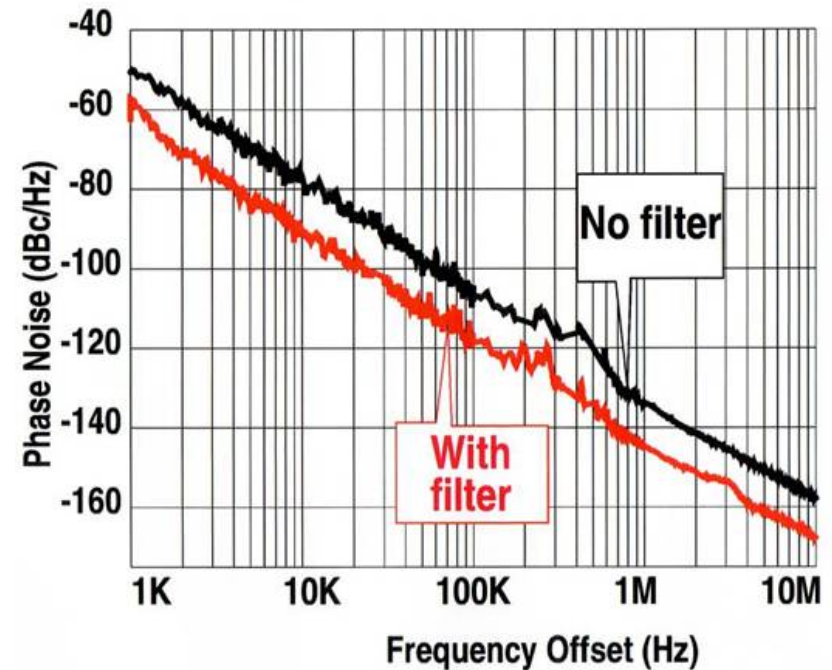
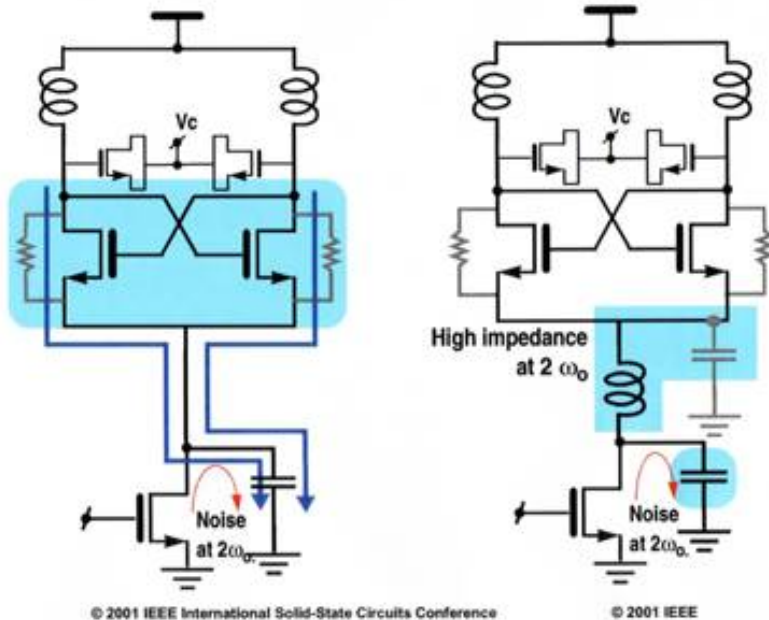
(c)

Filtering of $2f_o$ component in OSC.

Noise filtering of $2f_o$ component reduces the OSC phase noise to -10dB.

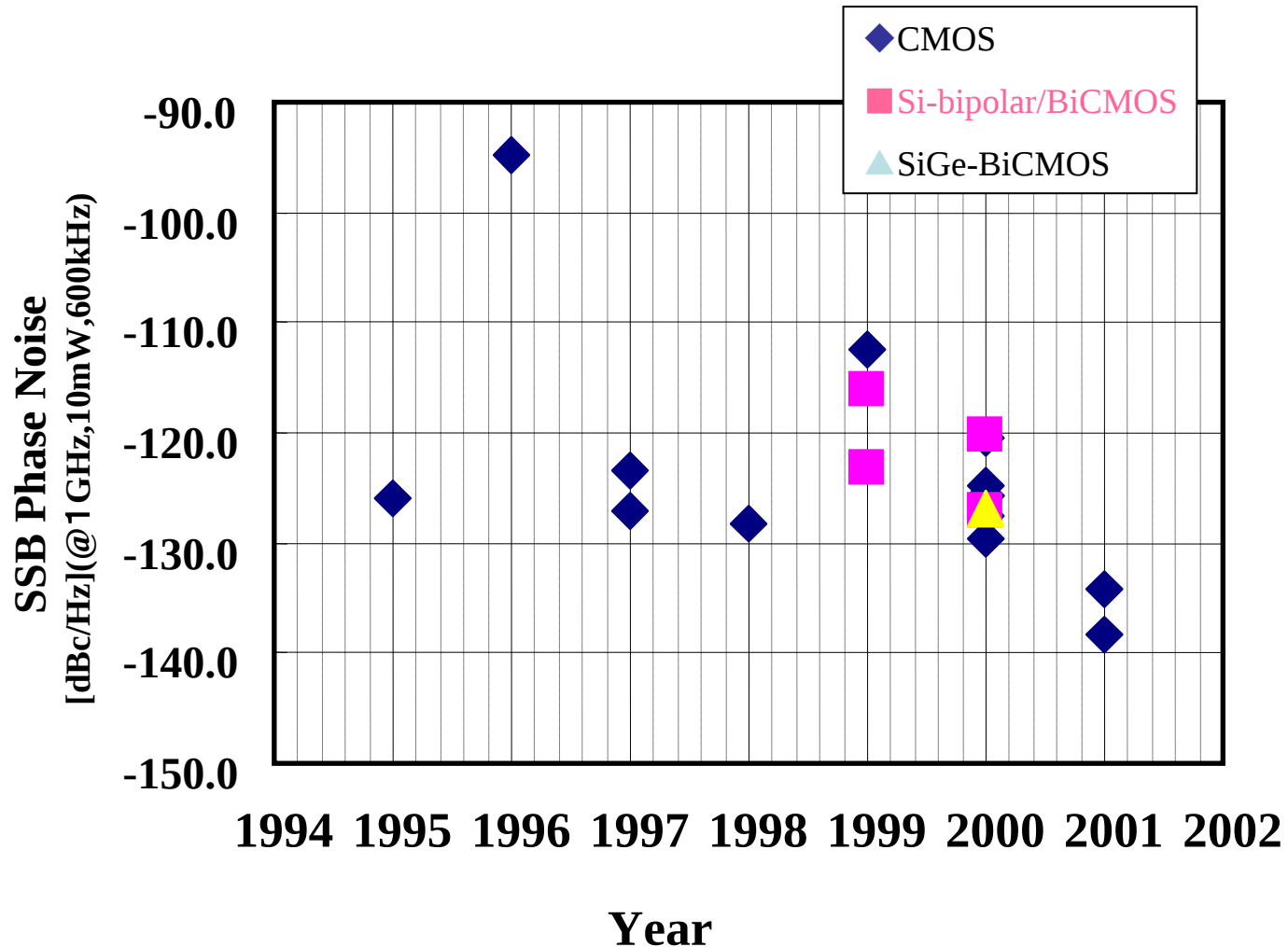
E. Hegazi, ISSCC 2001

Tail-Biased VCO with Noise Filtering



Oscillator phase noise progress

Phase noise in CMOS oscillator becomes lower than that of bipolar.



Acknowledgment and references

- **Acknowledgment**

I would like to thank Prof. Asad Abidi in UCLA for his advices.

- **References**

- Asad A. Abidi, "Power-Conscious design of Wireless circuits and systems," pp.665-695, "Trade-offs in Analog Circuit Design," Kluwer Academic Publishers, 2002. (Edited by Chris Toumanzou, George Moschytz, and Barrie Gilbert)
- Thomas. H. Lee, "The design of CMOS RF ICs," Cambridge University Press, Jan. 1998.
- Bezaad, Razavi, "RF micro-electronics," Prentice Hall, Nov. 1999.
- Domine Leenaerts, Johan van der Tang, and Ciero Vaucher, "Circuit Design for RF Transceivers," Kluwer Academic Publishers, 2001.
- Charles Chien, "Digital Radio Systems on A chip," Kluwer Academic Publishers, 2001.
- E. Hegazi, et. Al., "A Filtering Technique to Lower Oscillator Phase Noise," ISSCC 2001, 23.4, Feb. 2001.