ELG 2135

ELECTRONICS I

FOURTH CHAPTER :

BIPOLAR JUNCTION TRANSISTORS

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Having studied the junction diode, which is the most basic two-terminal semiconductor device, we now turn our attention to three-terminal semiconductor devices. Three-terminal devices are far more useful than two-terminal ones because they can be used in a multitude of applications.

There are two major types of three-terminal semiconductor devices: **the bipolar junction transistor** or BJT, which is the subject of this chapter, and **the field-effect transistor** or FET, which we shall study in next chapter.

The bipolar junction transistor consists of two PN junctions constructed in a special way and connected in series, back to back. Current is conducted by both electrons and holes, hence the name **bipolar**.

The simplified structure of a BJT consists of three semiconductors regions:

→ **Emitter** (E)

→ **Base** (B) which **always** refers to the **center** region

→ **Collector** (C)

We should distinguish between two possible structures of a BJT:

- A region of P type between two regions of N type (Figure IV-1) :

  → Such a transistor is called a **NPN transistor**.

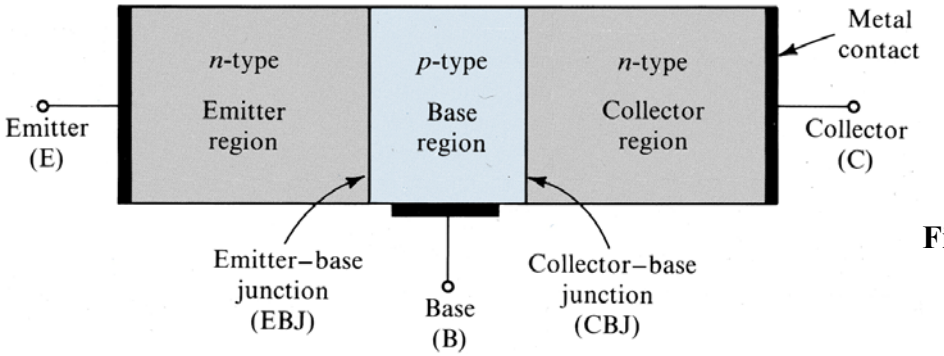


Figure IV-1

- A region of N type between two regions of P type (Figure IV-2) :

  → Such a transistor is called a **PNP transistor**.

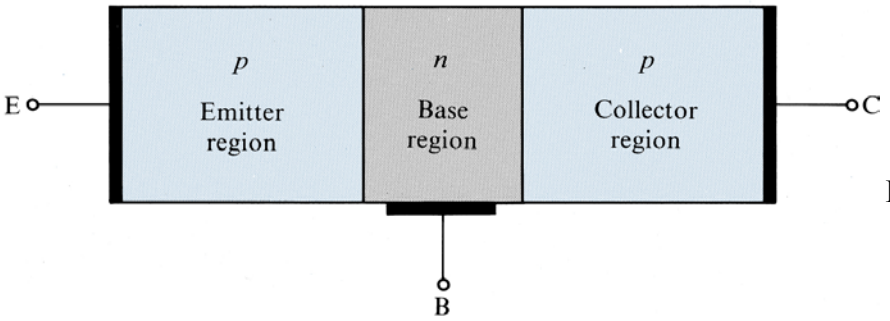


Figure IV-2

The transistor consists of two PN junctions:

- The Emitter-Base junction (E-B)
- The Collector-Base junction (C-B)

Depending on the bias condition (forward or reverse) of each of these junctions, different modes of operation of the BJT are obtained:

Mode	E-B Junction	C-B Junction
Cutoff	Reverse	Reverse
Active	Forward	Reverse
Saturation	Forward	Forward

The **active mode** is the one used if the transistor is to operate as an amplifier. Switching applications utilize both the **cutoff** and the **saturation modes**.

A – NPN TRANSISTOR

I – NPN transistor in the active mode

The physical operation of a NPN BJT in the active mode is shown in Figure IV-3. Two external voltage sources (batteries) are used to establish the required bias conditions for active-mode operation:

- The base-emitter voltage V_{BE} causes the *p*-type base to be higher in potential than the *n*-type emitter, thus forward-biasing the emitter-base junction.
- The collector-base voltage V_{CB} causes the *n*-type collector to be higher in potential than the *p*-type base, thus reverse-biasing the collector-base junction.

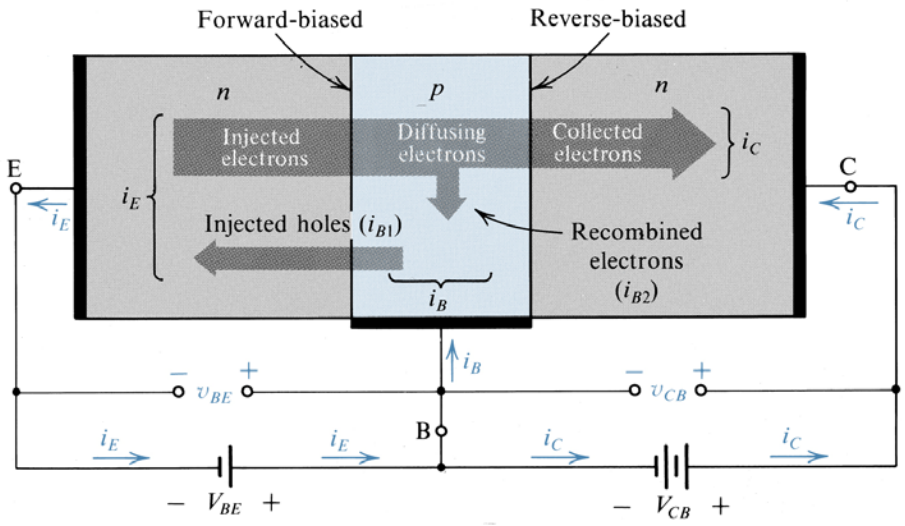


Figure IV-3

II – Current flow

As indicated in Figure IV-3, the forward bias of the emitter-base junction will cause two components of the current to flow across this junction: electrons injected from the emitter into the base, and holes injected from the base into the emitter. As it is highly desirable to have the first component (electrons) at a much higher level than the second component (holes) the device is designed to have a high density of electrons in the emitter and a low density of holes in the base. The sum of the two currents gives a current that is dominated by the electron component. It is called the **emitter current i_E** (direction is out of the emitter lead).

As base is a *p*-region, electrons injected from the emitter into the base will be minority carriers in the base. Because the base is usually very thin, the excess minority carriers (electron) concentration n_{po} in the base will have an almost straight-line profile (Figure IV-4) :

$$n_{po}(0) = n_{po}(0)e^{v_{BE}/V_T} \qquad (1)$$

Most of these diffusion electrons will reach the boundary of the collector-base depletion region. Because the collector is more positive than the base (by v_{CB} volts) these successful electrons will be swept across the CB junction depletion region into the collector. They will thus get “collected” to constitute the **collector current** i_C.

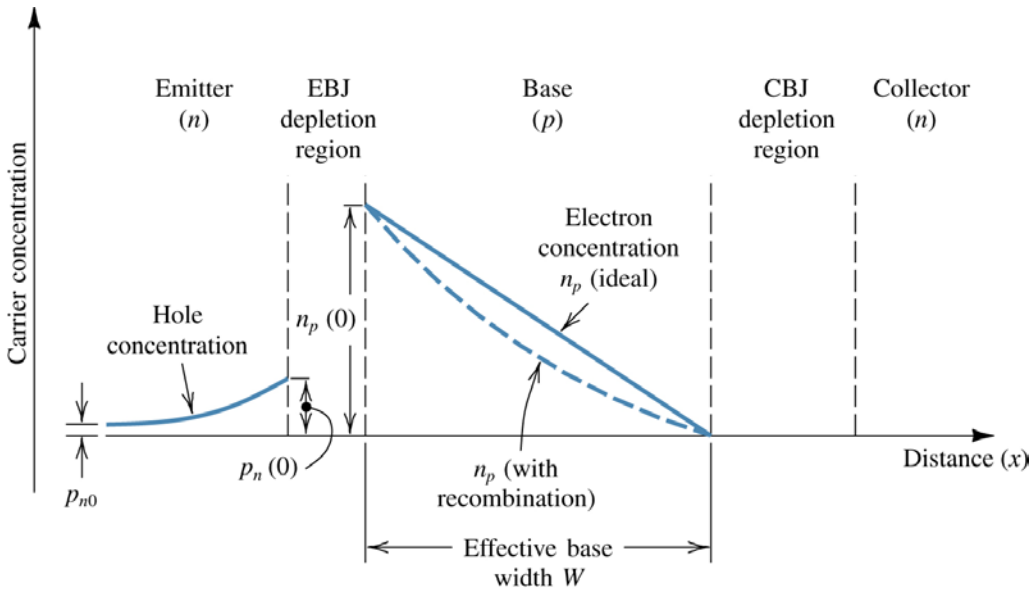


Figure IV-4

III – Collector current

By convention, the direction of the collector current will be opposite to that of electron flow. Thus i_c will flow into the collector terminal and can be expressed as:

$$i_C = I_S \, e^{v_{BE} / V_T} \tag{2}$$

where I_s is the **saturation current**.

IV – Base current

The current base is composed of two components. The first, i_{B1}, is due to the holes injected from the base region into the emitter region. The second component, i_{B2}, is due to holes that have to be supplied by the external circuit in order to replace the holes lost from the base through the recombination process.

Combining the two components, we obtain the total base current which is proportional to e^{v_{BE} / V_T}. We can show that this current can be expressed as a fraction of the collector current as follows:

$$i_C = \beta \, i_B \tag{3}$$

where β is a constant for the particular transistor. It is called the **common-emitter current gain**.

V – Emitter current

Since the current that enters a transistor should leave it, the emitter current is equal to the sum of the collector current and the base current:

$$i_E = i_C + i_B = (1+\beta) i_B \tag{4}$$

or

$$i_E = \frac{1+\beta}{\beta} i_C = \frac{1+\beta}{\beta} I_S \, e^{v_{BE}/V_T} \tag{5}$$

$$\rightarrow \quad i_C = \alpha \, i_E \tag{6}$$

where α is a constant for the particular transistor. It is called the **common-base current gain**. Usually, β is large (50 to 500 for usual transistors), so α is close to unity.

VI – Equivalent circuit models

The first-order model of transistor operation described above can be represented by the equivalent circuit shown in Figure IV-5-a. The EB junction is replaced by a diode: in fact, it is a nonlinear current source (collector current) controlled by a voltage (v_{BE}). It can be replaced by a current-controlled current-source (Figure IV-5-b).

Note that in this model the transistor is used as a two-port network with the input port between E and B and the output port between C and B. Base is the common terminal and then the current gain between the input current (i_E) and the output current (i_C) is α. Thus we can understand why α is called the common-base current gain.

Two other equivalent circuit models may be used to represent the large-signal operation of BJT. The model of Figure IV-5-c is a voltage-controlled current source. Here diode D_E is replaced by diode D_B which conducts the base current and thus the current scale factor is not { I_S/α } (diode D_E) but { I_S/β }. By simply expressing the collector current as { βI_B } we obtain the current-controlled current-source model shown in Figure IV-5-d.

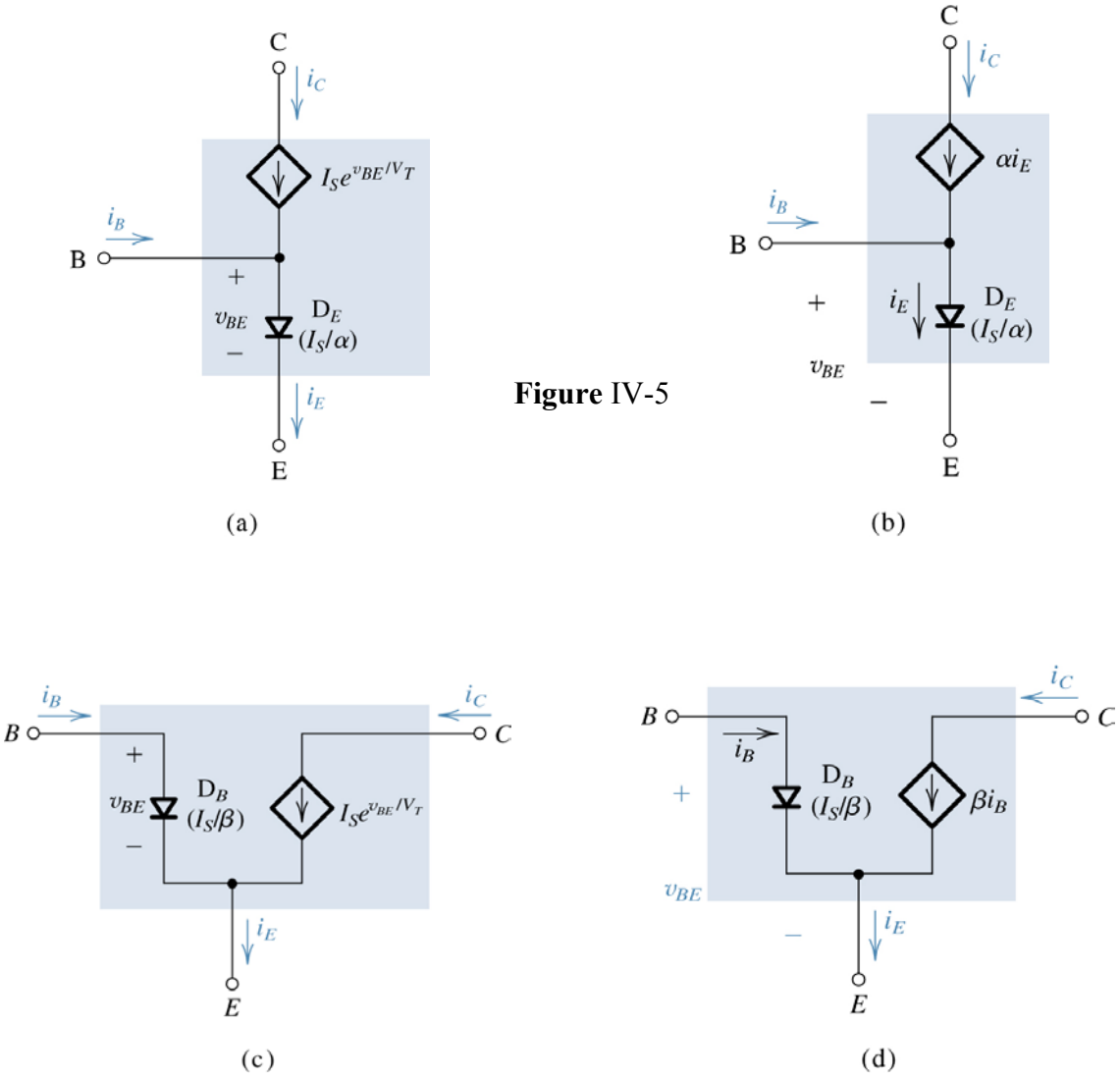


Figure IV-5

In this last model, if the transistor is used as a two-port network with the input port between base and emitter and the output port between collector and emitter, the emitter is the common terminal. Thus, we can understand why β is called the common-emitter gain.

B – PNP TRANSISTOR

The PNP transistor operates in a manner similar to that of the NPN device. Unlike the NPN transistor, current in the PNP device is mainly conducted by holes injected from the emitter into the base as a result of the forward-bias voltage V_{EB}. Here, the voltage V_{EB} causes the *p*-type emitter to be higher in potential than the n-type base, thus forward-biasing the base-emitter junction. The collector-base junction is reverse-biased by the voltage V_{BC} (Figure IV-6).

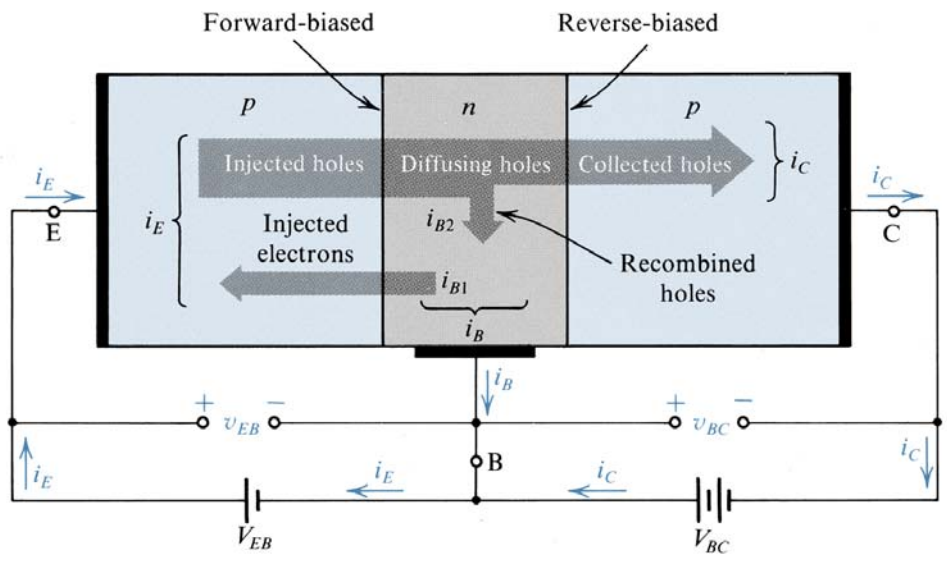


Figure IV-6

Since their behavior is similar, the PNP transistor models can be derived from the NPN transistor models. As an illustration, Figure IV-7 shows two PNP models.

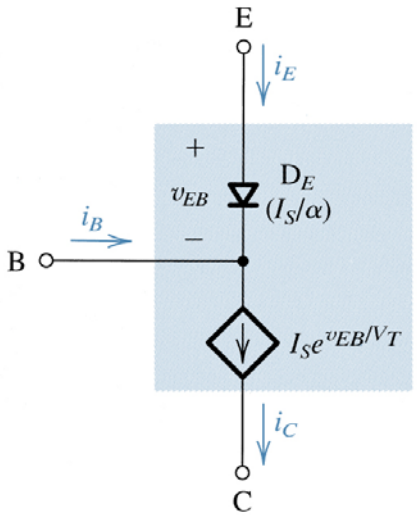
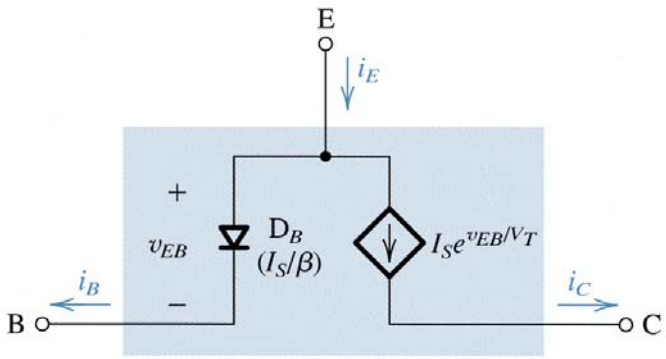


Figure IV-7



Since the current in the PNP model is mainly conducted by holes injected from the emitter into the base as a result of the forward-bias voltage V_{EB}, ALL equations and current-voltage relationships of the **PNP** *transistor will be identical to those of the* **NPN** *transistor except that the voltage* $\boldsymbol{v_{BE}}$ *has to be replaced by the voltage* $\boldsymbol{v_{EB}}$.

C – SYMBOLS AND CONVENTIONS

I – Symbols for transistors

A very descriptive and convenient circuit symbol exits for the BJT. In Figure IV-8, we noticed that the PNP has only **one** configuration since the second one is deduced from the first by a simple rotation.

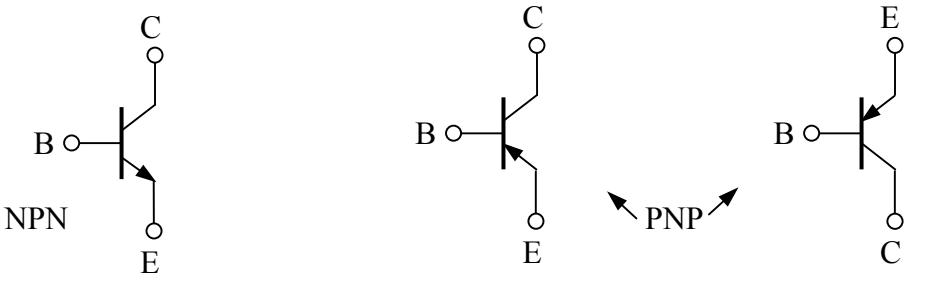


Figure IV-8

II – Bias voltages

Figure IV-9 shows NPN and PNP transistors biased to operate in the active mode. Note that currents flow from top to bottom and that voltages are higher at the top and lower at the bottom. Thus, an NPN transistor whose EB junction is forward-biased will operate in the active mode *as long as the collector is higher in potential than the base*. Similarly, an PNP transistor will operate in the active region *if the potential of the collector is lower than that of the base.*

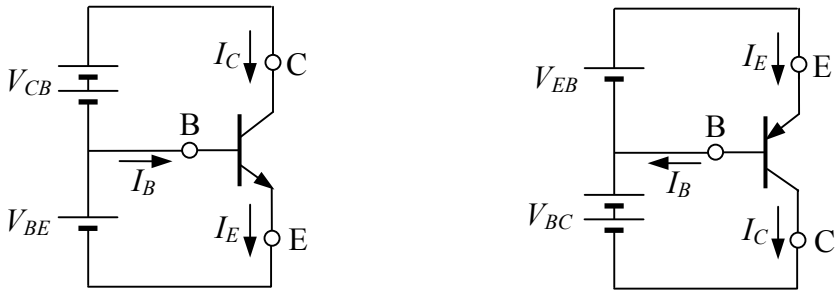


Figure IV-9

D – TRANSISTOR CHARACTERISTICS

Like for diodes, it is sometimes useful to describe the transistor *i-v* characteristics graphically. Since we have two ports, we have to consider both input and output currents and voltages.

I – i_C - v_{BE} characteristic

According to equation (2), we see that the i_C-v_{BE} is an exponential characteristic that is identical to the diode *i-v* relationship.

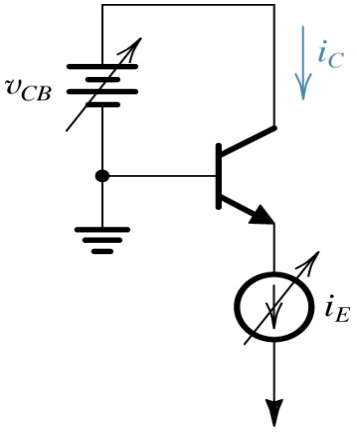
II – i_E - v_{BE} and i_B - v_{BE} characteristics

The i_E - v_{BE} and i_B - v_{BE} characteristics are also exponential but with different scale currents. Moreover, for v_{BE} smaller than about 0.5V, the current is negligibly small.

Also, over most of the normal range v_{BE} lies in the range 0.6 to 0.8V. In performing rapid first-order dc calculations we normally will assume that V_{BE} = 0.7V, which is similar to the approach used in the analysis of diode circuits.

III – Early Effect

Figure IV-10 shows the i_C versus v_{CB} characteristics of an NPN transistor for various values of the emitter current i_E. Only active-mode operation is shown, since only the portion of the characteristics for $v_{CB} > 0$ is drawn.



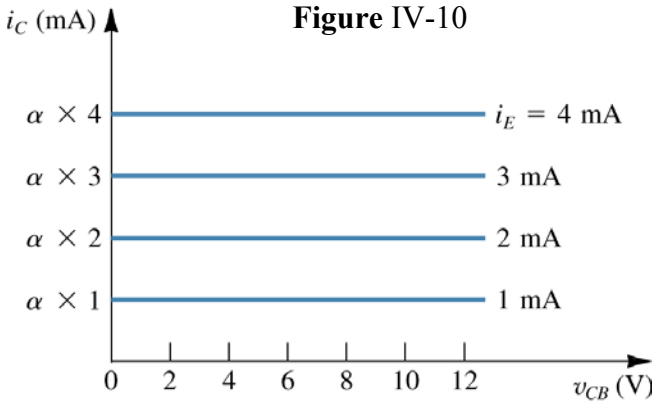


Figure IV-10

When operated in the active region, practical BJTs show some dependence of the collector current on the collector voltage, with the result that their i_C-v_{CB} characteristics are not perfectly horizontal straight lines. In Figure IV-11, the transistor is connected in the common emitter configuration, and its V_{BE} can be set to any desired value by adjusting the dc source connected between base and emitter. At each value of V_{BE}, the corresponding i_C - v_{CE} characteristic curve can be obtained point-by-point by varying the dc source connected between collector and emitter. The result is the family of i_C - v_{CE} characteristic curves shown in Figure IV-11.

We observe that the characteristic curves, though still straight lines, have finite slope. In fact, when extrapolated, the characteristic lines meet at a point on the negative v_{CE} axis at $\{v_{CE} = -V_A\}$. This voltage V_A, a positive number, is a parameter for the particular BJT, with typical values in the range of 50 to 100V. It is called the **Early voltage**. At a given value of v_{BE}, increasing v_{CE} increases the reverse-bias voltage on the collector-base junction and thus increases the width W of the depletion region of this junction. This in turn results in a decrease in the effective base width W. Recalling that I_S is inversely proportional to W, we see that I_S will increase and i_C increases proportionally.

→ **This is the Early effect**.

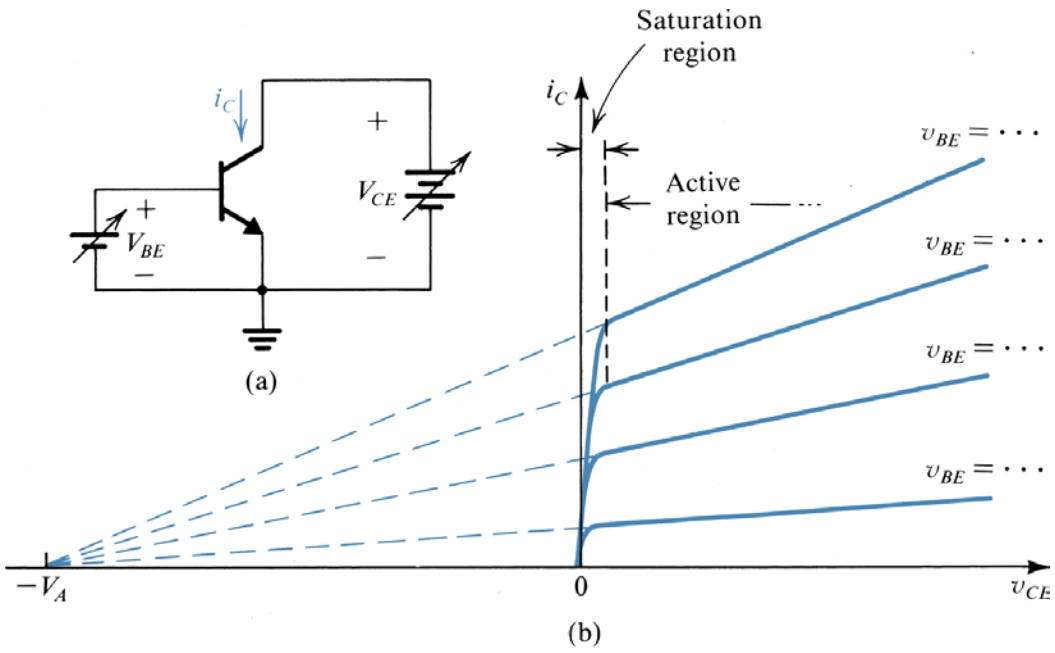


Figure IV-11

The linear dependence of i_C on v_{CE} can be accounted for by assuming that

$$i_C = I_S\, e^{v_{BE}/V_T}\left(1+\frac{v_{CE}}{V_A}\right) \tag{7}$$

The nonzero slope of the i_C-v_{CE} lines indicates that the **output resistance of the transistor** looking into the collector is not infinite:

$$r_o = \left[\left(\frac{\partial i_C}{\partial v_{CE}}\right)_{v_{BE}=constant}\right]^{-1} \approx \frac{V_A}{I_C} \tag{8}$$

where I_C is the current level corresponding to the constant value of v_{BE} near the boundary of the active region.

E – ANALYSIS OF TRANSISTOR CIRCUITS AT DC

For the dc analysis of transistor circuits, we use the simple constant voltage junction model {i.e., V_{BE} = 0.7V }. This approximation can be refined using transistor measurements or simulations.

To emphasize this analysis, we will solve some examples.

Example I

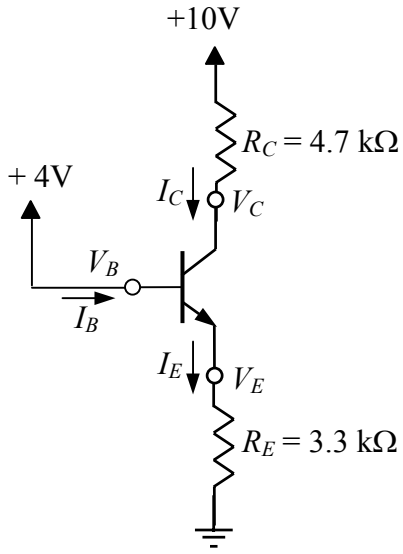


Figure IV-12

In this first example (Figure IV-12), we wish to determine the dc voltages. Glancing at the circuit, we note that the base is connected to +4V and the emitter is grounded through a resistance R_E. It therefore is safe to conclude that the base-emitter junction is forward-biased (active mode) and then

$$V_E = 4 - V_{BE} = 4 - 0.7 = 3.3\,\text{V} \tag{9}$$

Thus,

$$I_E = (V_E - 0)/R_E = 1\,\text{mA} \tag{10}$$

Assuming $\beta = 100$, we obtain

$$I_C = \alpha I_E = \frac{\beta I_E}{\beta + 1} = 0.99\,\text{mA} \qquad \rightarrow \qquad I_B = \frac{I_E}{\beta + 1} = 0.01\,\text{mA} \tag{11}$$

Note: **Verify if the relation (4) between i_B, i_C and i_E is satisfied**.

We can now determine the collector voltage:

$$V_C = 10 - I_C R_C = 10 - 0.99 * 4.7 = 5.3\,\text{V} \tag{12}$$

Since the collector-base junction is reverse-biased (5.3V > 4V), the assumption that the transistor is in **the active mode is verified**.

Example II

Here, we used the same circuit except that the base is biased at +6V. We have:

$$V_E = 6 - V_{BE} = 6 - 0.7 = 5.3\,\text{V} \tag{13}$$

Thus,

$$I_E = (V_E - 0)/R_E = 1.6\,\text{mA} \tag{14}$$

and

$$V_C = 10 - I_C R_C = 10 - 7.52 = 2.48\,\text{V} \tag{15}$$

Since the collector-base junction is forward biased (2.48V < 6V), the transistor is in **the saturation mode.**

Example III

In this example, the circuit remains identical except that the voltage is zero. Thus, the emitter-base junction cannot conduct and the emitter current is zero. Since the current base is zero, the current collector has to be zero. Note that in this case, the collector-base junction cannot conduct. The transistor is in the **cutoff mode of operation**.

Example IV

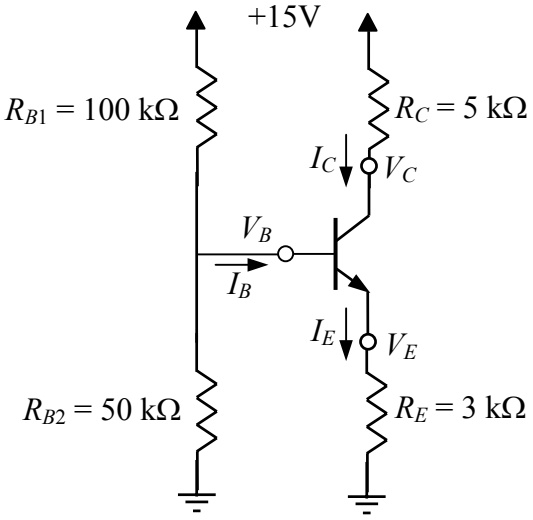


Figure IV-13

In this example (Figure IV-13), we note the inclusion of two resistances R_{B1} and R_{B2} that are used for transistor bias (here, only **one** dc source is required). We assume that β = 100. The first step consists to use Thevenin's theorem to simplify the circuit (Figure IV-14).

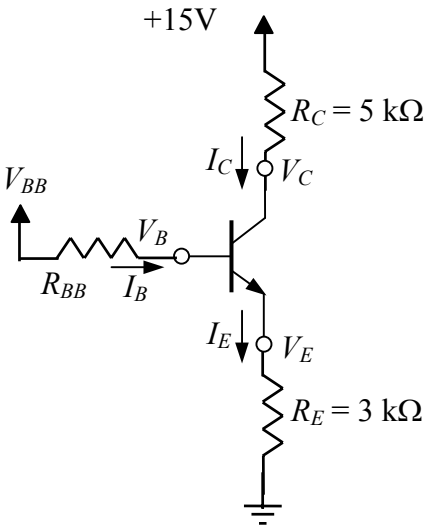


Figure IV-14

Thevenin's voltage is:

$$V_{BB} = 15\frac{R_{B2}}{R_{B1} + R_{B2}} = 5\,\text{V} \tag{16}$$

and Thevenin's resistance is equal to:

$$R_{BB} = R_{B1} \,//\, R_{B2} = 100 \,//\, 50 = 33.3\,\text{k}\Omega \tag{17}$$

Thus, the base loop equation gives

$$V_{BB} = I_B R_{BB} + V_{BE} + R_E I_E \tag{18}$$

Substituting for I_B by

$$I_B = \frac{I_E}{\beta + 1}$$

$$\rightarrow \qquad I_E = \frac{V_{BB} - V_{BE}}{R_E + \left[R_{BB} / (\beta + 1)\right]} = \frac{5 - 0.7}{3 + \left[33.3 / 101\right]} = 1.29\,\text{mA} \tag{19}$$

Then

$$I_B = \frac{I_E}{\beta + 1} = 0.0128\,\text{mA} \tag{20}$$

The base voltage is given by

$$V_B = V_{BE} + R_E I_E = 0.7 + 1.29 * 3 = 4.57\,\text{V} \tag{21}$$

Assuming that the transistor is in the active mode, we have:

$$I_C = \alpha I_E = 0.99 * 1.29 = 1.28\,\text{mA} \tag{22}$$

Thus, the collector voltage is

$$V_C = 15 - I_C R_C = 15 - 1.28 * 5 = 8.6\,\text{V} \tag{23}$$

It follows that the collector is higher in potential than the base, which means that the transistor is in the active mode, **as had been assumed**.

F – AC ANALYSIS: THE TRANSISTOR AS AN AMPLIFIER

Since the transistor is a current amplifier in the active region, we usually refer to the transistor in the ac analysis as an amplifier. The biasing problem is that of establishing a **constant dc current in the emitter** (or the collector). This **current should be predictable and insensitive to variations** in temperature, value of β, …. To understand how the transistor operates as an amplifier, consider the conceptual circuit shown in Figure IV-15-a. Here the base-emitter junction is forward-biased by a dc voltage V_{BE} (battery). The reverse bias of the collector-base junction is established by connecting the collector to another power supply of voltage V_{CC} through a resistor R_C.

I – DC conditions

In dc, the circuit reduces to that in Figure IV-15-b. The relationships for the dc currents and voltages give

$$I_B = \frac{I_E}{\beta + 1} = \frac{I_C}{\beta} \tag{24}$$

$$I_C = \alpha I_E = I_s e^{V_{BE}/V_T} \tag{25}$$

and

$$V_C = V_{CE} = V_{CC} - R_C I_C \tag{26}$$

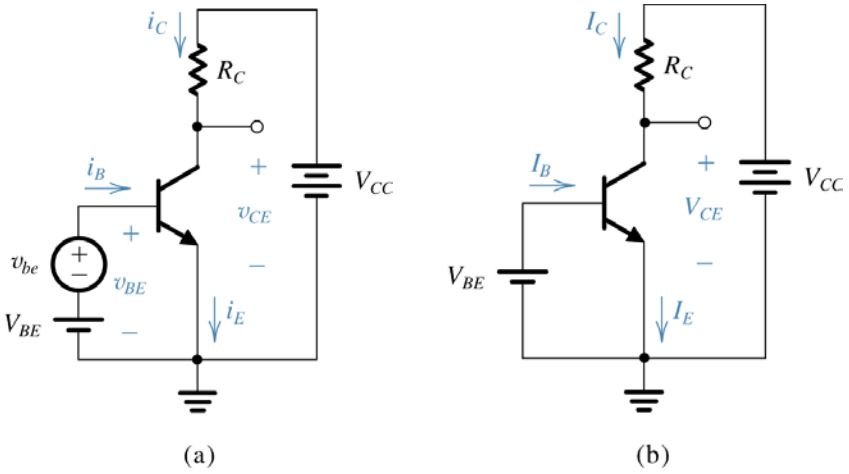


Figure IV-15

II – AC analysis - Transconductance

If a signal v_{be} is applied, the total instantaneous base-emitter voltage becomes

$$v_{BE} = V_{BE} + v_{be} \tag{27}$$

Correspondingly, the collector current becomes (using equation (25)):

$$i_C = \alpha i_E = I_S e^{v_{BE}/V_T} = I_S e^{V_{BE}/V_T} e^{v_{be}/V_T} = I_C e^{v_{be}/V_T} \tag{28}$$

With the **small-signal approximation**, we can write:

$$V_{BE} << V_T \tag{29}$$

Then,

$$i_C \approx I_C \left(1 + \frac{v_{be}}{V_T}\right) = I_C + \frac{I_C}{V_T} v_{be} \tag{30}$$

Thus the collector current is composed of the dc bias value I_C and a signal component

$$i_c = \frac{I_C}{V_T} v_{be} \tag{31}$$

We then introduce a new parameter, the **transconductance** g_m that is equal to:

$$i_c = g_m v_{be} \tag{32}$$

$$\rightarrow \qquad g_m = \frac{I_C}{V_T} \tag{33}$$

A graphical interpretation for gm is given in Figure IV-16, where it is shown that gm is equal to the slope of the i_C-v_{BE} characteristic curve at $i_C = I_C$ (i.e., at the bias point Q):

$$g_m = \frac{I_C}{V_T} = \left.\frac{\partial i_C}{\partial v_{BE}}\right|_{i_C = I_C} \tag{34}$$

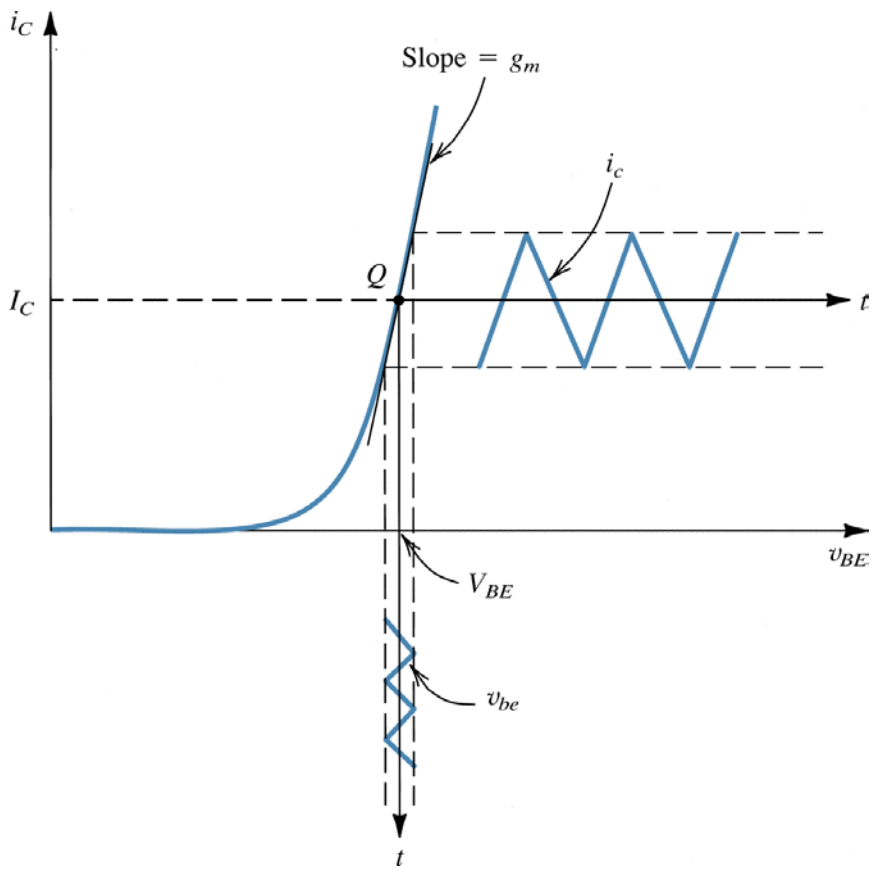


Figure IV-16

III – AC analysis – Input resistance at the base

To determine the resistance seen by the source v_{be}, we first evaluate the total base current:

$$i_B = \frac{i_C}{\beta} = \frac{I_C}{\beta} + \frac{1}{\beta}\frac{I_C}{V_T}v_{be} = I_B + i_b \tag{35}$$

We can then deduce a relationship between the ac quantities

$$i_b = \frac{1}{\beta}\frac{I_C}{V_T}v_{be} = \frac{g_m}{\beta}v_{be} \tag{36}$$

This ratio, equivalent to a resistance, is the small-signal input resistance between base and emitter, looking into the base

$$r_\pi = \frac{v_{be}}{i_b} = \frac{\beta}{g_m} = \frac{\beta I_B}{g_m I_B} = \frac{V_T}{I_B} \tag{37}$$

IV – AC analysis – Input resistance at the emitter

The total emitter current i_E can be determined from

$$i_E = \frac{i_C}{\alpha} = \frac{I_C}{\alpha} + \frac{i_c}{\alpha} = I_E + i_e \tag{38}$$

Thus

$$i_e = \frac{I_C}{\alpha V_T} v_{be} = \frac{I_E}{V_T} v_{be} \tag{39}$$

This ratio, equivalent to a resistance, is the small-signal input resistance between base and emitter, looking into the emitter

$$r_e = \frac{v_{be}}{i_e} = \frac{V_T}{I_E} = \frac{\alpha}{g_m} \approx \frac{1}{g_m} \tag{40}$$

We can then deduce a relationship between the two input resistances

$$r_\pi = (1+\beta) r_e \tag{41}$$

V – Voltage gain

To establish the voltage gain, we have to determine the collector voltage

$$v_C = V_{CC} - R_C i_C = V_{CC} - R_C (I_C + i_c) = (V_{CC} - R_C I_C) - i_c R_C = V_C - i_c R_C \tag{42}$$

Hence, the voltage signal is given by

$$v_c = -i_c R_C = -g_m R_C v_{be} \tag{43}$$

Thus the voltage gain of the amplifier is

$$\frac{v_c}{v_{be}} = -g_m R_C \tag{44}$$

G – SMALL-SIGNAL EQUIVALENT CIRCUIT MODELS

From the previous results, the amplifier circuit in Figure IV-17-a will be equivalent to the circuit shown in Figure IV-17-b.

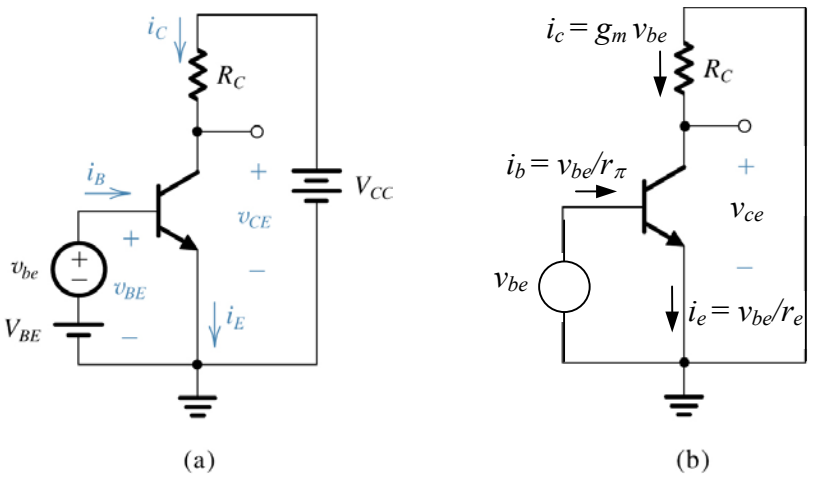


Figure IV-17

Thus, the small-signal equivalent circuit can be modeled by two different topologies, namely the **hybrid-π models** (Figure IV-18) or **the T models** (Figure IV-19).

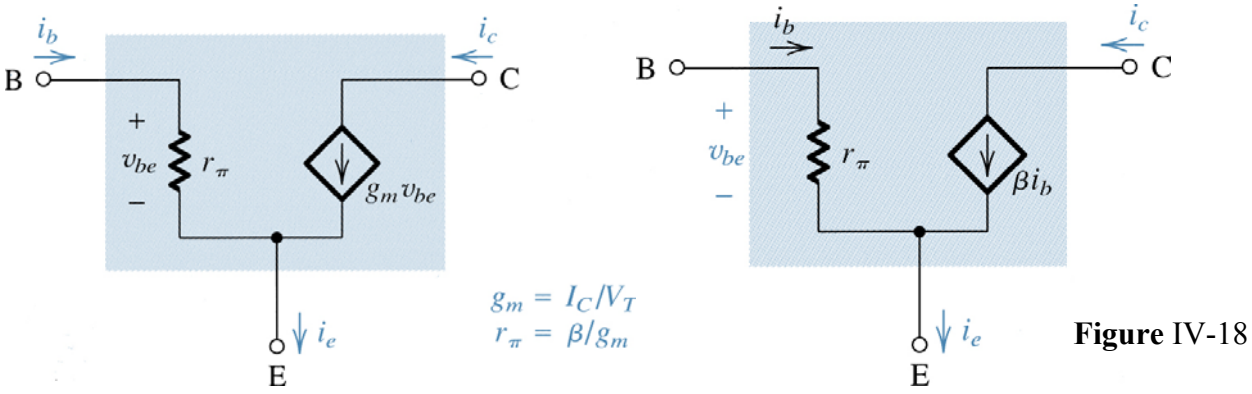


Figure IV-18

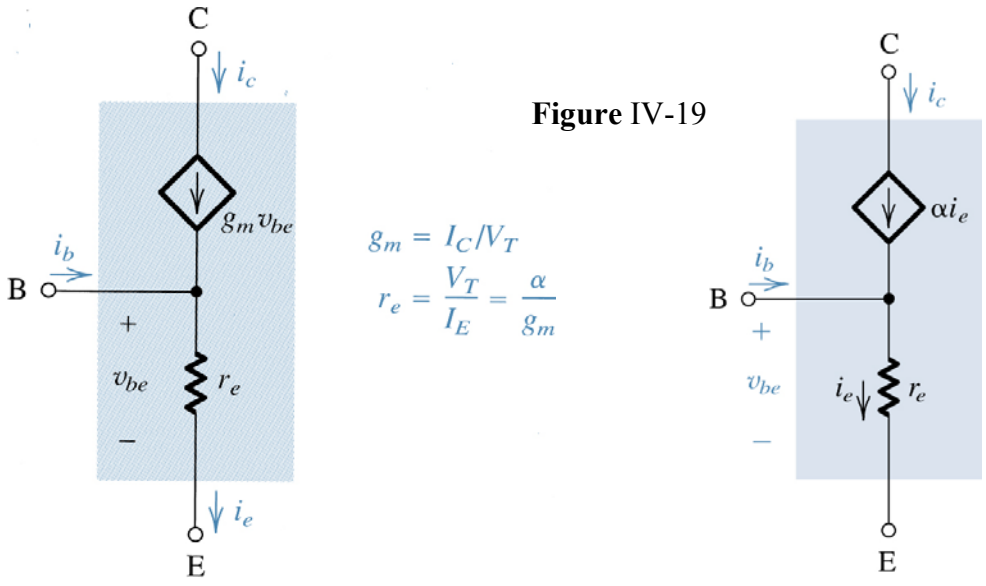


Figure IV-19

I – Application of the small-signal equivalent circuits

The process of applying small-signal models consists of the following steps:

- Determine the dc operation point of the BJT and in particular the dc collector current I_C
- Calculate the values of the small-signal parameters: g_m, r_π and r_e:

$$r_e = \frac{V_T}{I_E} = \frac{\alpha}{g_m}$$

$$g_m = \frac{I_C}{V_T}$$

$$r_\pi = \frac{\beta}{g_m} = \frac{V_T}{I_B}$$

- Eliminate the dc sources by replacing each dc voltage source with a short circuit and each dc current source with an open circuit.
- Replace the BJT with one of its small-signal equivalent circuit models. Although any one of the models can be used, one might be more convenient than the others for a particular circuit analysis.
- Analyze the resulting circuit to determine the required quantities, i.e., the voltage gain, the input resistance, etc.

II – Example: analysis of a BJT amplifier

We wish to analyze the circuit shown in Figure IV-20. We assume $\beta = 100$.

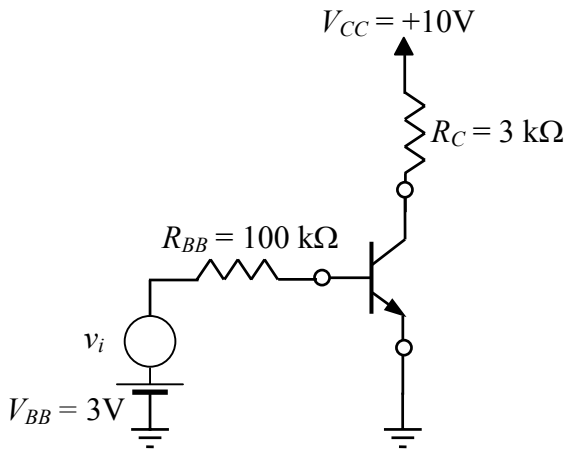


Figure IV-20

The first step is the dc analysis ($v_i = 0$). We have

$$I_B = \frac{V_{BB} - V_{BE}}{R_{BB}} = \frac{3 - 0.7}{100k} = 0.023\,\text{mA} \tag{45}$$

Then

$$I_C = \beta I_B = 2.3\,\text{mA} \tag{46}$$

and

$$V_C = V_{CC} - I_C R_C = 10 - 2.3 * 3 = 3.1\,\text{V} \tag{47}$$

Having determined the operating point, we may now proceed to determine the small-signal model parameters (Figure IV-21):

$$r_e = \frac{V_T}{I_E} = \frac{25\,\text{mV}}{(2.3/0.99)\text{mA}} = 10.8\Omega \tag{48}$$

$$g_m = \frac{I_C}{V_T} = \frac{2.3\,\text{mA}}{25\,\text{mV}} = 92\,\text{mA/V} \tag{49}$$

$$r_\pi = \frac{\beta}{g_m} = \frac{100}{92} = 1.09\Omega \tag{50}$$

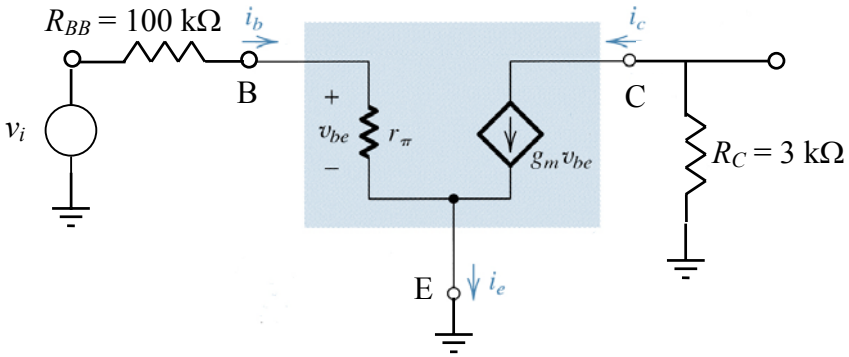


Figure IV-21

Analysis of the equivalent circuit gives

$$v_{be} = v_i \frac{r_\pi}{r_\pi + R_{BB}} = v_i \frac{1.09}{101.09} = 0.011 v_i \tag{51}$$

The output voltage is given by

$$v_o = -g_m v_{be} R_C = -92 * 0.011 v_i * 3 = -3.04 v_i \tag{52}$$

Thus the voltage gain is –3.04 V/V. To gain more insight into the operation of transistor amplifiers, we wish to consider the waveforms at various points in the circuit analyzed in this example. For this purpose, assume that the input signal has a triangular waveform (Figure IV-22). One constraint on signal amplitude is the small-signal approximation, which stipulates that v_{be} should not exceed about 10 mV ($v_{be} << V_T$). If we take the triangular waveform v_{be} to be 20 mV peak-to-peak, equation (51) gives

$$v_i = \frac{v_{be}}{0.011} \quad \rightarrow \quad v_{i\,max} = \hat{V}_i = \frac{\hat{V}_{be}}{0.011} = 0.91\,\text{V} \tag{53}$$

To check whether or not the transistor remains in the active mode with v_i having a peak value of 0.91V, we have to evaluate the collector voltage. Since the input voltage is triangular, the collector voltage will consists of a triangular wave v_c superimposed on the dc value V_C (+3.1V):

$$\hat{V}_c = \hat{V}_i * gain = 0.91 * 3.04 = 2.77\,\text{V} \tag{54}$$

It follows that when the output swings negative, the collector voltage reaches a minimum of

$$\hat{V}_{c\,min} = 3.1 - 2.77 = 0.33\,\text{V} \tag{55}$$

which is lower than the base voltage (0.7V). Thus the transistor will not remain in the active mode with v_i having a peak value of 0.91V (Figure IV-22). The maximum value of the peak of the input signal such that the transistor remains active at all times should corresponds to the minimum value of the collector voltage being equal to the base voltage, which is approximately 0.7V. Thus using equation (54)

$$\hat{V}_i = \frac{3.1 - 0.7}{3.04} = 0.79\,\text{V} \tag{56}$$

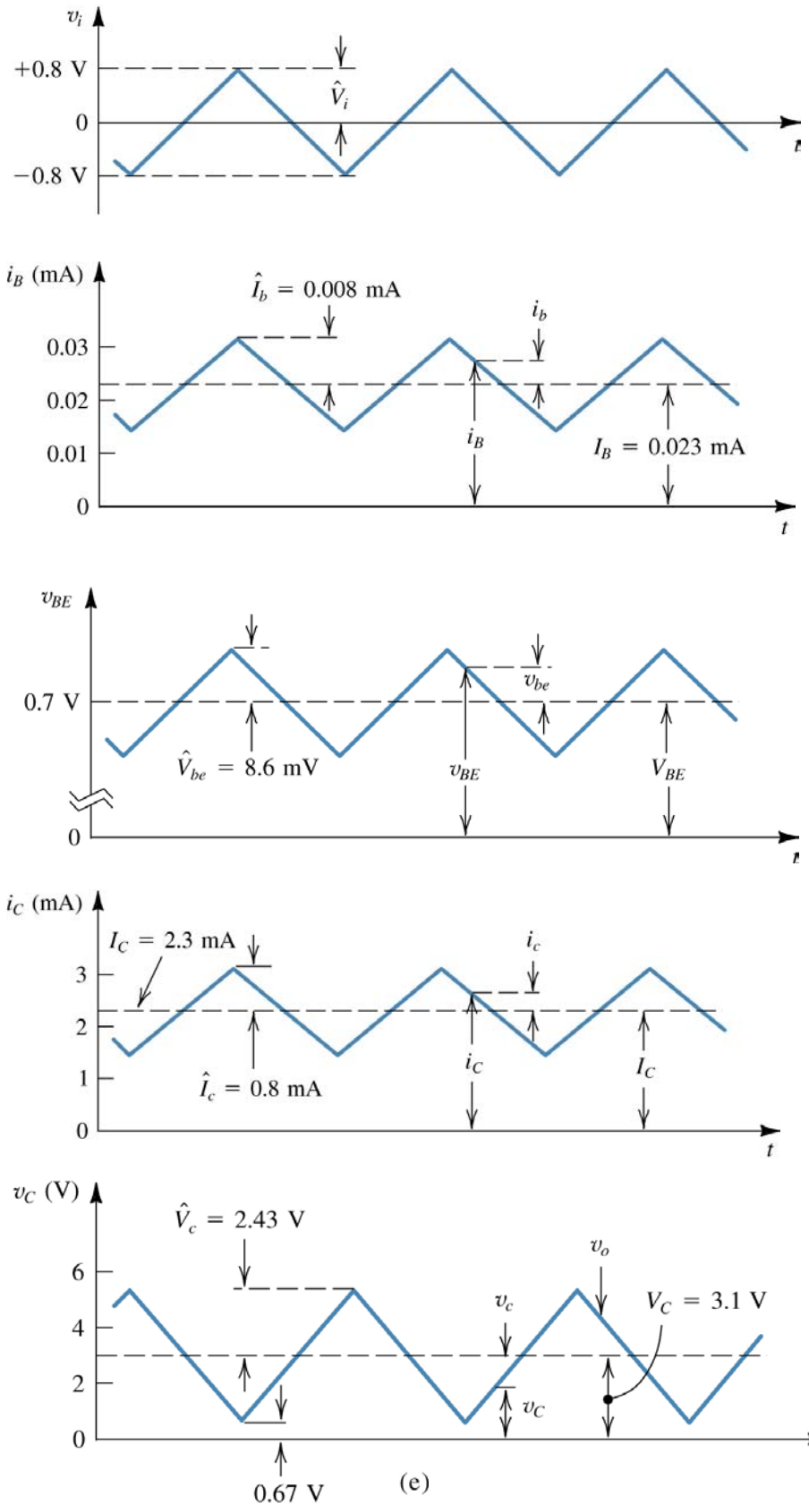

v_i
+0.8 V
0
−0.8 V
$\hat{V}_i$
t
i_B (mA)
$\hat{I}_b$ = 0.008 mA
i_b
0.03
0.02
0.01
0
i_B
I_B = 0.023 mA
t
v_{BE}
0.7 V
v_{be}
$\hat{V}_{be}$ = 8.6 mV
v_{BE}
V_{BE}
0
t
i_C (mA)
I_C = 2.3 mA
i_c
3
2
1
0
$\hat{I}_c$ = 0.8 mA
i_C
I_C
t
v_C (V)
$\hat{V}_c$ = 2.43 V
v_o
6
4
2
0
v_c
V_C = 3.1 V
v_C
0.67 V
t
(e)

Figure IV-22

Let us choose 0.8V, as shown in Figure IV-22-a, and complete the analysis by determining the base current peak value:

$$\hat{I}_b = \frac{\hat{V}_i}{R_{BB} + r_\pi} = \frac{0.8}{100 + 1.09} = 0.008\,\text{mA} \tag{57}$$

This triangular-wave current will be superimposed on the dc base current I_B, as shown in Figure IV-22-b. The base-emitter voltage will consist of a triangular-wave component superimposed on the dc V_{BE} that is approximately 0.7V. The peak value of the triangular waveform will be (Figure IV-22-c)

$$\hat{V}_{be} = \hat{V}_i \frac{r_\pi}{R_{BB} + r_\pi} = 0.8 \frac{1.09}{100 + 1.09} = 8.6\,\text{mV} \tag{58}$$

The signal current in the collector will be triangular in waveform, with a peak value given by

$$\hat{I}_c = \beta \hat{I}_b = 100 * 0.008 = 0.8\,\text{mA} \tag{59}$$

This current will be superimposed on the quiescent collector current I_C (=2.3 mA), as shown in Figure IV-22-d. Finally, the signal voltage at the collector can be obtained by multiplying v_i by the voltage gain (figure IV-22-e):

$$\hat{V}_c = 3.04 * 0.8 = 2.43\,\text{V} \tag{60}$$

III – Improving the hybrid-π model with the Early effect

The Early effect causes the collector current to depend not only on v_{BE} but also on v_{CE}. This dependence on v_{CE} can be modeled by assigning a finite output resistance r_o (as defined by equation (8) to the controlled current-source in the hybrid-π model.

When the transistor operates as an amplifier in which the emitter is grounded, this resistance

$$r_o \approx \frac{V_A}{I_C} \tag{61}$$

is in parallel with R_C. In order to conform with the literature, the voltage v_{be} is renamed as v_π as shown in Figure IV-23.

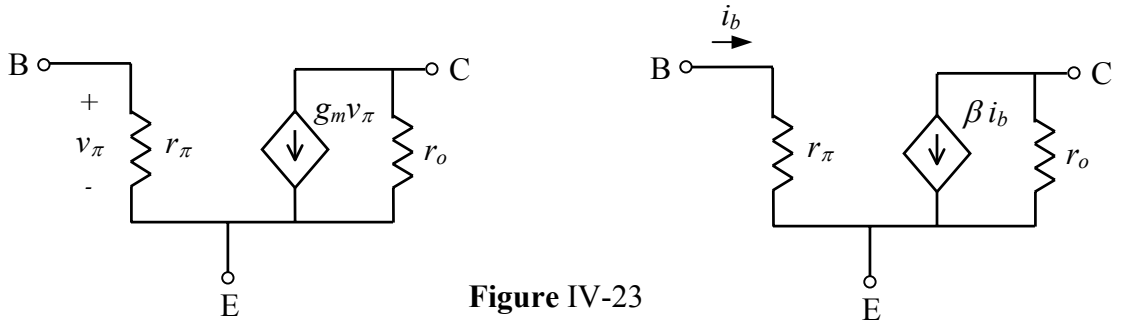


Figure IV-23

Summary: with: $\beta = \dfrac{\alpha}{1-\alpha}$ $\alpha = \dfrac{\beta}{1+\beta}$

Model parameters in terms of dc bias: $r_e = \dfrac{V_T}{I_E} = \alpha\dfrac{V_T}{I_C}$ $g_m = \dfrac{I_C}{V_T}$

$r_\pi = \dfrac{V_T}{I_B} = \beta\dfrac{V_T}{I_C}$ $r_o = \dfrac{V_A}{I_C}$

Parameters in terms of g_m: $r_e = \dfrac{\alpha}{g_m}$ $r_\pi = \dfrac{\beta}{g_m}$

Parameters in terms of r_e: $g_m = \dfrac{\alpha}{r_e}$ $r_\pi = (\beta+1)r_e$

$$g_m + \frac{1}{r_\pi} = \frac{1}{r_e}$$

IV – Summary on the operating modes of BJTs

It is often useful to summarize the different operating modes of BJTs in terms of voltages. For this purpose, we will use the voltages shown in Figure IV-24 as references.

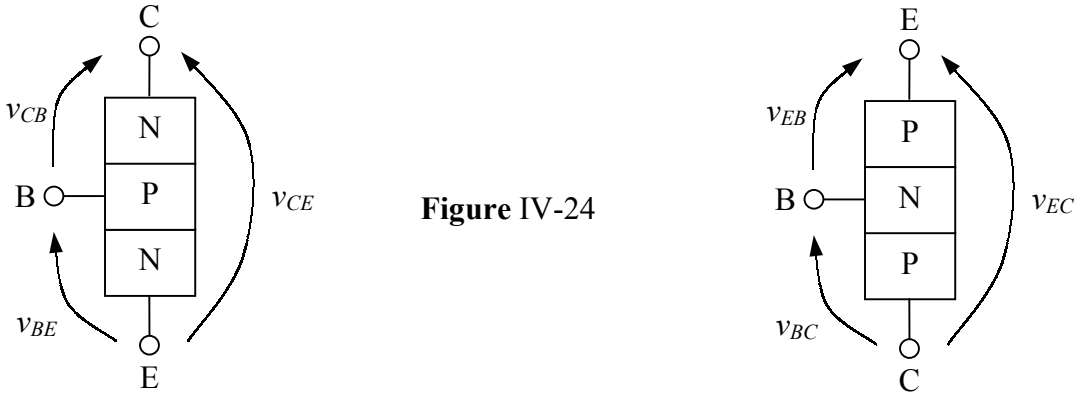


Figure IV-24

$v_{BE} > 0$ $v_{CB} < 0$: The two junctions are forward-biased. The transistor is similar to a short circuit between the collector and the emitter:

→ ***Saturation Mode (used in digital circuits and communication systems)***

$v_{BE} < 0$ $v_{CB} > 0$: The two junctions are reverse-biased. The transistor is similar to an open circuit between the collector and the emitter:

→ ***Cutoff mode (used in digital circuits and communication systems)***

$v_{BE} > 0$ $v_{CB} > 0$: One junction is forward-biased while the second is reverse-biased. The base-emitter voltage generates the collector-emitter current, creating a controlled current-source. This source is mainly used for amplification:

→ ***Active Mode (used in amplifiers)***

$v_{BE} < 0$ $v_{CB} < 0$: One junction is forward-biased while the second is reverse-biased. This case is similar to the previous one, except that the source generates a lower current gain since the junctions are not symmetrical:

→ ***Reverse Active Mode (rarely used)***

H – GRAPHICAL ANALYSIS

I – Graphical dc analysis

Although graphical methods are of little practical value in the analysis of most transistor circuits, it is illustrative to show graphically the operation of a transistor amplifier circuit (Figure IV-25).

A graphical analysis of the operation of this circuit can be performed as follows: First, we have to determine the dc bias point I_B (set v_i to zero). We next move to the voltage-current characteristics (Figure IV-26).

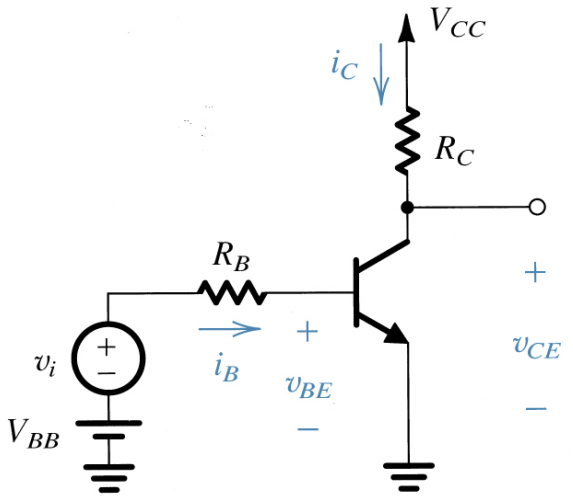


Figure IV-25

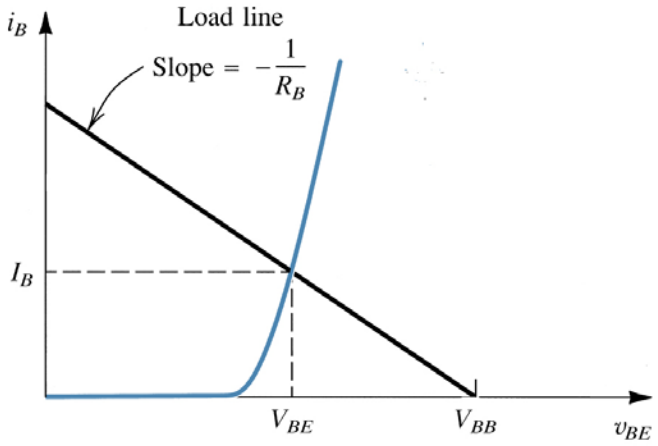


Figure IV-26

Having determined the base bias current, we know that the operating point will lie on the i_C-v_{CE} curve corresponding to this value of base current (the curve for $i_B = I_B$). Where it lies on the curve will be determined by the collector current circuit which represents a linear relationship between v_{CE} and i_C. This case can be represented by a straight line, as shown in Figure IV-27. Since R_C can be considered the amplifier load, this line is known as the **load line**. As for diodes, the dc bias point will be at the intersection of the load line and the i_C-v_{CE} curve corresponding to the base current I_B.

The coordinates of point Q give the dc collector current I_C and the dc collector-to-emitter voltage V_{CE}. Specifically, the collector current imposes the constraint

$$v_{CE} = V_{CC} - i_C R_C \quad \rightarrow \quad i_C = \frac{V_{CC}}{R_C} - \frac{1}{R_C} v_{CE} \tag{62}$$

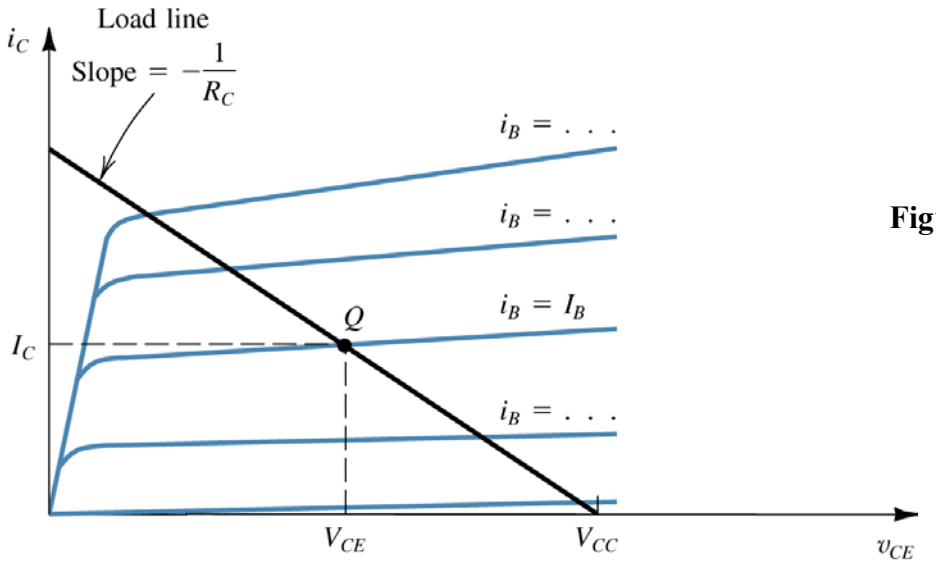


Figure IV-27

Once the dc parameters determined, the signal v_i is applied as illustrated in Figure IV-28. Corresponding to each instantaneous value of { $V_{BB} + v_i(t)$ } one can draw a straight line with slope {$-1/R_B$}.

Such instantaneous load line intercepts the i_B-v_{BE} curve at a point whose coordinates give the total instantaneous values of i_B and v_{BE} corresponding to the particular value of { $V_{BB} + v_i(t)$ }. On Figure IV-28, we can see the straight lines corresponding to $v_i = 0$, v_i at its positive peak and v_i at its negative peak.

If the amplitude of v_i is sufficiently small so that the instantaneous operating point is confined to an almost-linear segment of the i_B-v_{BE} curve, then the resulting signals i_b and v_{be} will be triangular in waveform. Next, we move to the i_C-v_{CE} characteristics of Figure IV-29. The operating point will move along the load line of slope {$-1/R_C$} as i_B goes through the instantaneous values determined from Figure IV-28.

II – Effects of bias-point location on allowable signal swing

Refer to Figure IV-29, the positive peaks of v_{ce} cannot go beyond V_{CC}, otherwise the transistor enters the cutoff region. Similarly, the negative peaks of v_{ce} cannot extend below a few tenths of a volt, otherwise the transistor enters the saturation region.

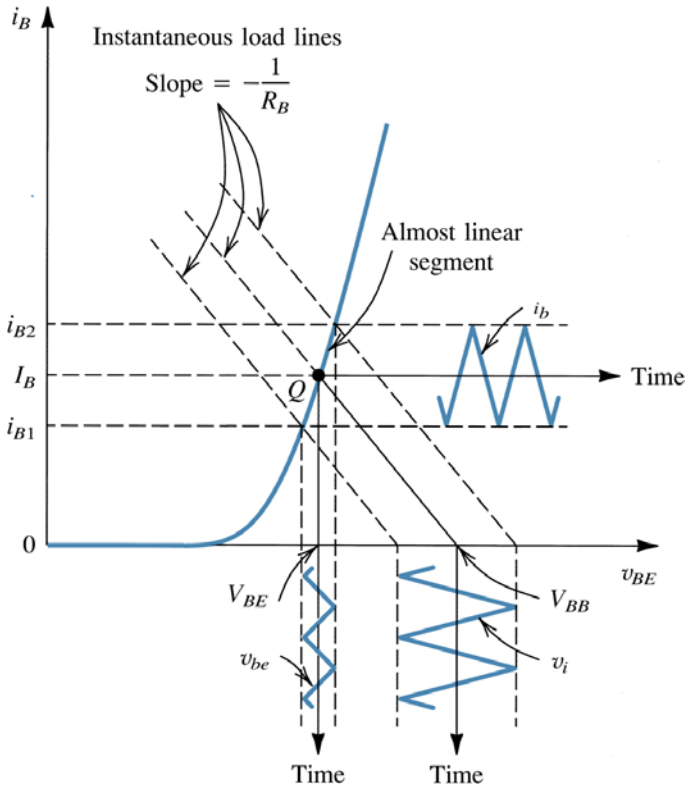


Figure IV-28

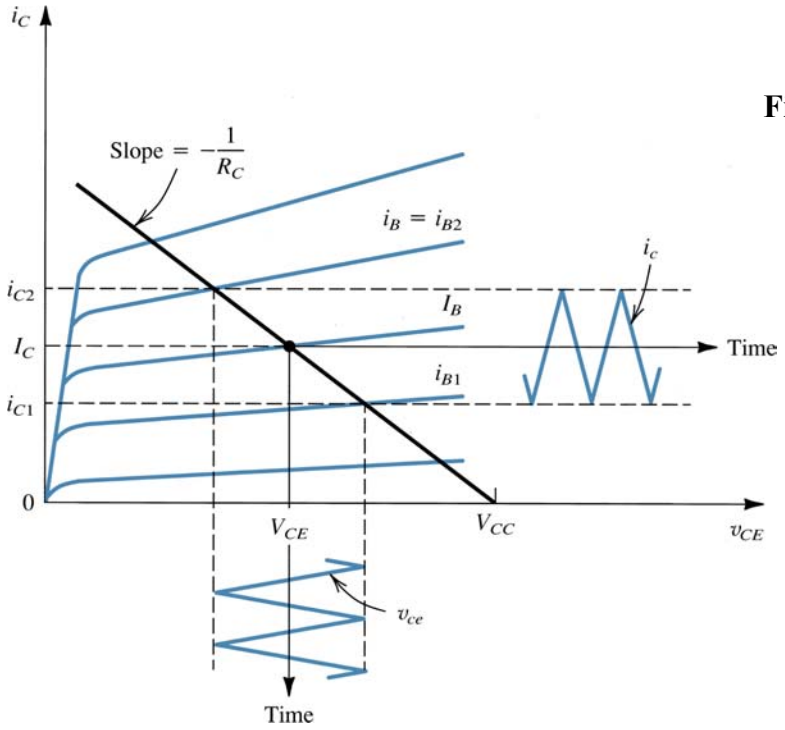


Figure IV-29

Figure IV-30 shows that a low value of R_C corresponds to the load line "A" where the operating Q_A exhibits a value of V_{CE} very close to V_{CC} (0).

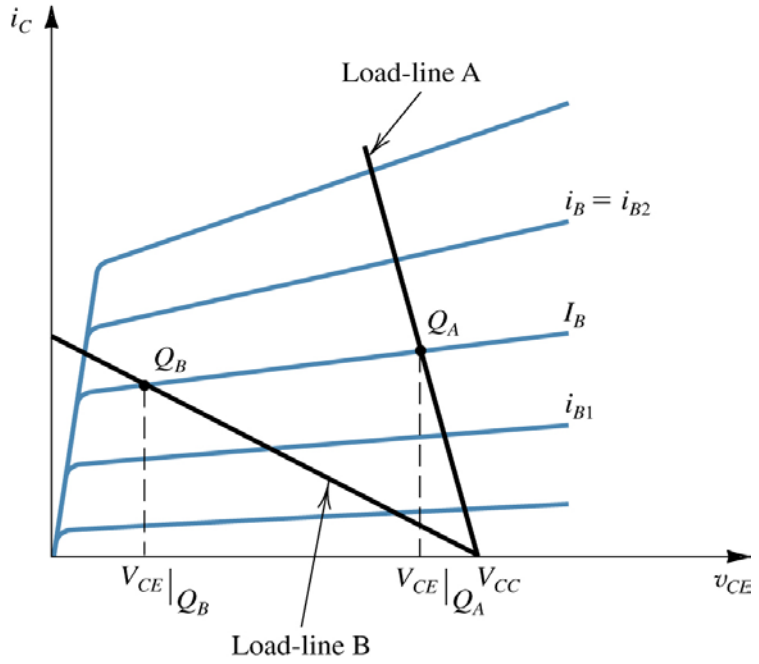


Figure IV-30

Thus the positive swing of v_{ce} will be severely limited (from V_{CE} to the dc bias V_{CC}). On the other hand, line "B", which corresponds to a large R_C, results in the bias point Q_B whose V_{CE} is too low. (Swing from 0 to V_{CE}). A compromise between these two extreme situations is obviously called for.

I – CIRCUIT BIAS

I – Bias using a single dc power supply

The bias problem is to establish a constant dc current in the emitter of the BJT. This current has to be calculable, predictable, ad insensitive to variations in temperature and to the large variations in the value of β encountered among transistors of the same type.

Another important consideration in bias design is locating the dc bias point in the i_C-v_{CE} plane so as to allow for maximum output signal swing.

Figure IV-31 shows the arrangement most commonly used for biasing a transistor amplifier if only a single power supply is available. The technique consists of supplying the base with a fraction of the supply voltage V_{CC} through the voltage divider $R_1//R_2$.

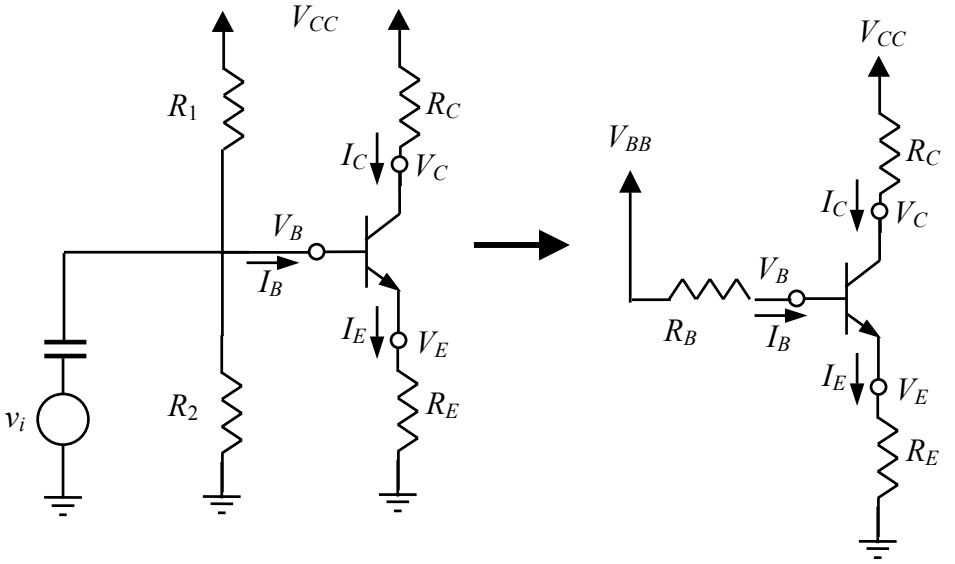


Figure IV-31

This voltage divider can be replaced by its Thevenin equivalent circuit

$$V_{BB} = \frac{R_2}{R_1 + R_2} V_{CC} \tag{63-a}$$

$$R_B = \frac{R_1 R_2}{R_1 + R_2} \tag{63-b}$$

The emitter current can be determined as

$$I_E = \frac{V_{BB} - V_{BE}}{R_E + \left[R_B / (\beta + 1)\right]} \tag{64}$$

To make this current insensitive to temperature and β variations, we design the circuit to satisfy the following two constraints

$$V_{BB} >> V_{BE} \tag{65-a}$$

$$R_E >> \frac{R_B}{1 + \beta} \tag{65-b}$$

Condition (65-a) ensures that small variations in V_{BE} (around 0.7V) will be swamped by the much larger V_{BB}.

This is a limit, however, on how large V_{BB} can be:

- For a given value of the supply voltage V_{CC}, the higher the value we use for V_{BB}, the lower will be the sum of voltages across R_C and the collector-base junction (V_{CB}).
- On the other hand, we want the voltage across R_C to be large in order to obtain high voltage gain and large signal swing (before transistor cutoff).
- We also want V_{CB} (or V_{CE}) to be large to provide a large signal swing (before transistor saturation).

A first compromise would be $\{I_{R1} = I_C/10\}$ which, in first approximation, leads to

$$V_{BB} \approx \frac{1}{3}V_{CC} \tag{66-a}$$

$$V_{CB}\left(or\ V_{CE}\right) = \frac{1}{3}V_{CC} \qquad \text{or} \qquad V_B = \frac{1}{3}V_{CC} - 0.7 \approx \frac{1}{3}V_{CC} \tag{66-b}$$

$$V_{RC} = I_C R_C \approx \frac{1}{3}V_{CC} \tag{66-c}$$

Condition (65-b) makes I_E insensitive to variations in β and could be satisfied by selecting R_B small. This in turn is achieved by using low values for R_1 and R_2.

Lower values for R_1 and R_2, however, will mean a higher current drain from the power supply and normally will result in a lowering of the input resistance of the amplifier (if the signal is coupled to the base), which is the trade-off involved in this part of the design problem.

Further insight into the mechanism by which the bias arrangement stabilizes the dc emitter (and hence collector) current is obtained by considering the feedback action provided by R_E. Consider that for some reason the **emitter current increases**. The **voltage drop across $\boldsymbol{R_E}$** (hence V_E) **will increase**.

Now, if the base voltage is determined primarily by the voltage divider (R_1, R_2), which is the case if R_B is small, it will remain constant, and **the increase in $\boldsymbol{V_E}$** will result in a **corresponding decrease in $\boldsymbol{V_{BE}}$.** This in turn **reduces the collector** (and emitter) **current**.

Thus R_E provides **a negative feedback action that stabilizes the bias current**.

II – Biasing using two dc power supplies

A somewhat simpler bias arrangement is possible if two power supplies are available, as shown in Figure IV-32.

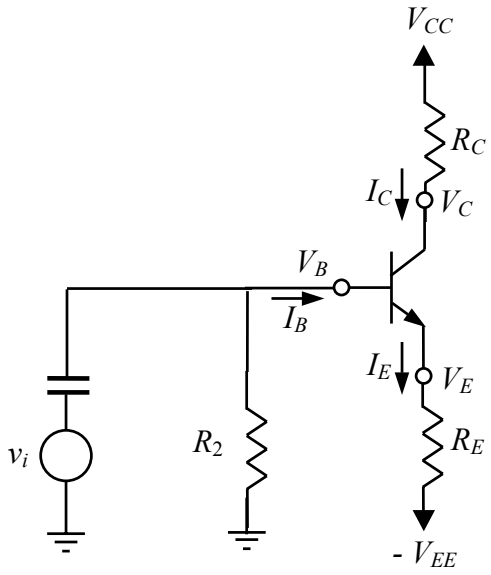


Figure IV-32

Here V_{BB} is replaced by V_{EE} and the loop equation is similar to that of equation (64):

$$I_E = \frac{V_{BB} - V_{BE}}{R_E + \left[R_B / (\beta + 1)\right]} \tag{67}$$

Thus the two above constraints apply here as well. Note that if the transistor is to be used with the base grounded (common-base configuration) then R_B can be eliminated altogether. On the other hand, if the input signal is to be coupled to the base, then R_B is needed. **Note** that here we have **one more degree of freedom**. In fact, if

$$V_{EE} >> V_{BE} \tag{68-a}$$

$$R_E >> \frac{R_B}{1+\beta} \tag{68-b}$$

the emitter current will satisfy the condition

$$I_E \approx \frac{V_{EE}}{R_E} \tag{69}$$

and therefore will be not dependent neither of β nor temperature. Moreover, there is no dc power "lost" in the resistances R_1 and R_2. However, this circuit requires two independent dc power supplies.

III – Alternative biasing arrangement

Figure IV-33 shows a simple but effective alternative biasing arrangement suitable for common-emitter amplifiers.

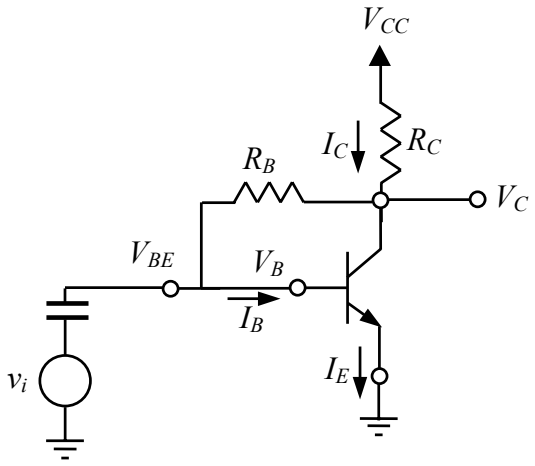


Figure IV-33

We have

$$I_E = \frac{V_{CC} - V_{BE}}{R_C + [R_B / (\beta + 1)]} \tag{70}$$

To obtain a value of I_E that is insensitive to variations of β, we select

$$R_C >> \frac{R_B}{1 + \beta} \tag{71}$$

Note however, that the value of R_B determines the allowable signal swing at the collector since

$$V_{CB} = I_B R_B = I_E \frac{R_B}{\beta + 1} \tag{72}$$

Bias stability in this circuit is achieved by the negative feedback action of R_B.

IV – Biasing using a current source

The transistor BJT can be biased using a constant current source I as indicated in the circuit of Figure IV-34.

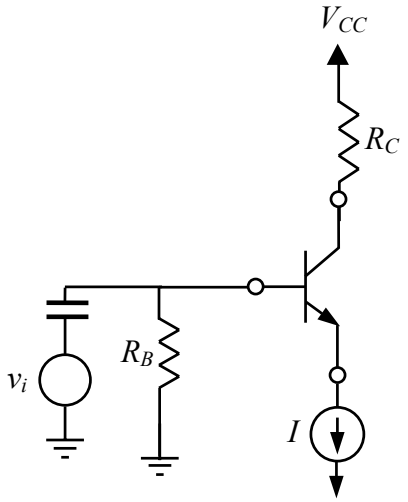


Figure IV-34

This circuit has the advantage that the emitter current is independent of the values of β and R_B. Thus R_B can be made large, enabling an increase in the input resistance at the base without adversely affecting bias stability.

A simple implementation of the constant-current source I is shown in Figure IV-35.

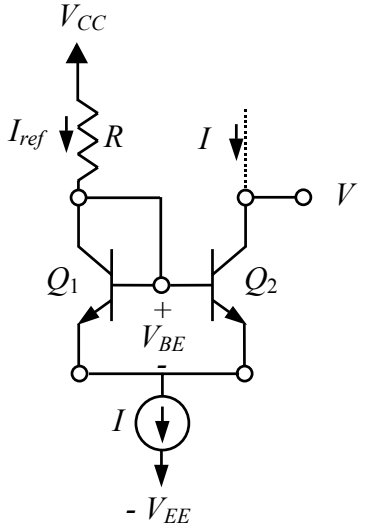


Figure IV-35

This circuit utilizes a pair of matched transistors (i.e., the two transistors have identical parameters). If we assume that the two transistors have identical high β values, we can neglect their base currents. Thus the current through Q_1 will be approximately equal to I_{REF}

$$I_{ref} = \frac{V_{CC} - (-V_{EE}) - V_{BE}}{R} \tag{73}$$

Since the transistors have the same V_{BE}, their collector currents will be equal, resulting in

$$I = I_{ref} = \frac{V_{CC} - (-V_{EE}) - V_{BE}}{R} \tag{74}$$

Neglecting the Early effect in Q_2, the collector current will remain constant at the value given by this equation as long as Q_2 remains in the active region. The circuit $Q_1 - Q_2$ is known as a **current mirror**.

J – SINGLE-STAGE AMPLIFIER CONFIGURATIONS

There are three basic configurations of BJT amplifiers: **The common-emitter** (CE), the **common-base** (CB), and the **common-collector** (CC). Their **name** refers to the terminal that is **common** to input and output ports.

I – Common-emitter amplifier

The basic configuration of the common-emitter amplifier is shown in Figure IV-36 (the emitter is grounded). The BJT is biased with a constant-current source *I* that is assumed to have a high output resistance.

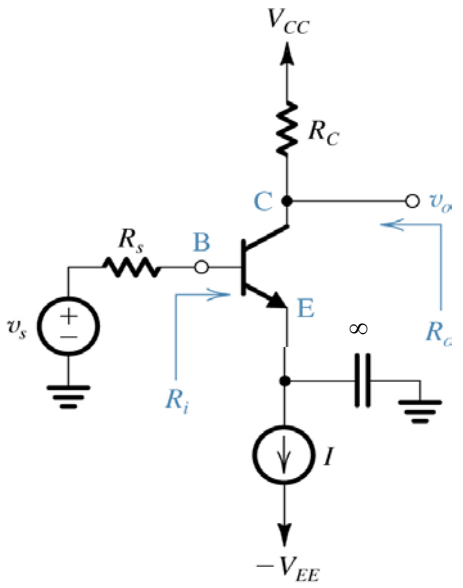


Figure IV-35

We can determine that the input resistance is equal to

$$R_i = r_\pi \tag{75}$$

and the voltage gain as

$$A_v = \frac{v_o}{v_\pi}\frac{v_\pi}{v_s} = -g_m\left(R_C \,//\, r_o\right)\frac{r_\pi}{R_s + r_\pi} = -\frac{\beta\left(R_C \,//\, r_o\right)}{R_s + r_\pi} \tag{76}$$

For usual discrete circuits, $R_C >> r_o$. Thus, choosing a large value for R_C gives

$$A_v = -g_m r_o = -\frac{V_A}{V_T} \tag{77}$$

which is independent of the bias current I_C. The current gain of the CE amplifier can be found to be

$$A_i = \frac{i_o}{i_b} = \frac{-g_m v_\pi r_o /\left(r_o + R_C\right)}{v_\pi / r_\pi} = -\beta\frac{r_o}{r_o + R_C} \tag{78}$$

For $R_C << r_o$, the gain is practically equal to β which is the common-emitter short-circuit current gain (i.e. $R_C = 0$). Finally, the output resistance is equal to

$$R_o = R_C \,//\, r_o \tag{79}$$

To summarize, the CE amplifier can be designed to provide substantial voltage and current gains (an advantage), it has an input resistance of moderate value, and it has a high output resistance (a disadvantage).

II – Common-emitter amplifier with a resistance in the emitter

Including a resistance in the signal path between emitter and ground, as shown in Figure IV-36, can lead to significant changes in the amplifier characteristics (we will have an additional variable to help the designer).

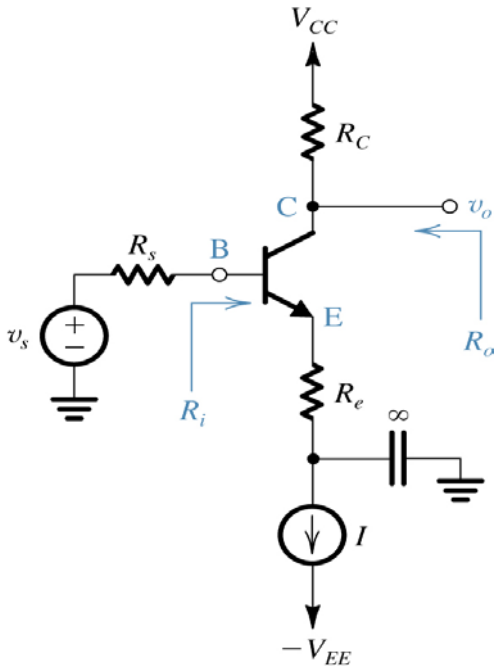


Figure IV-36

Analysis of the circuit can be performed by replacing the BJT with one of its small-signal models. Here the most convenient is the T model. This is because we have a resistance R_e in the emitter that will appear in series with the emitter resistance r_e of the T model and thus be simply added to it. Replacing the BJT with the T model augmented by the collector output resistance r_o results in the amplifier equivalent circuit shown in Figure IV-37.

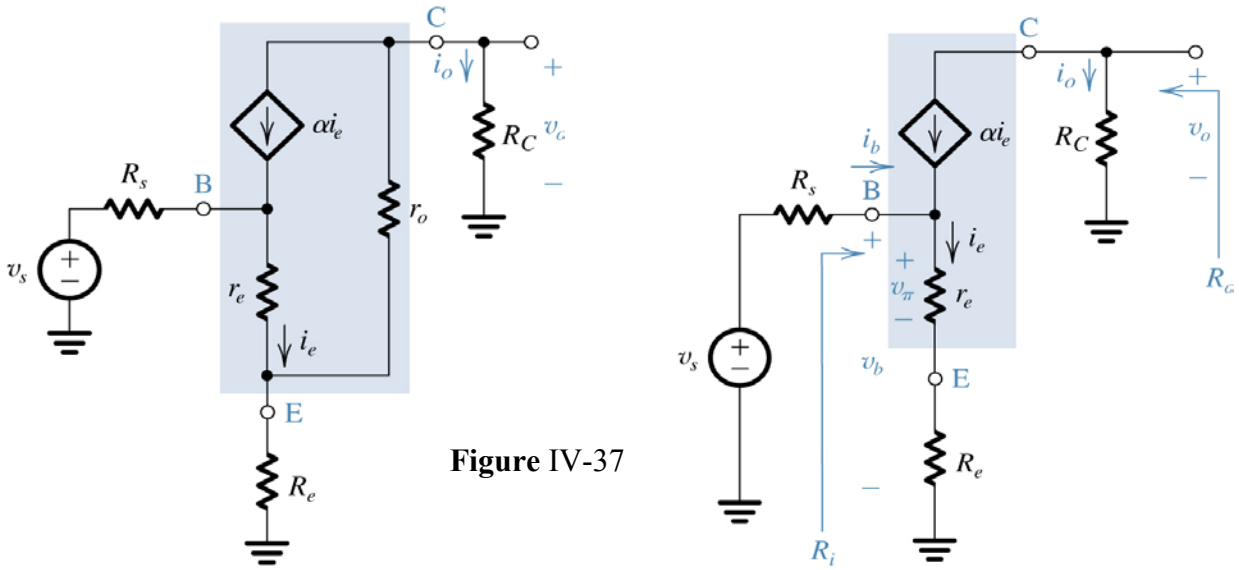


Figure IV-37

To determine the input resistance, we note that

$$R_i = \frac{v_b}{i_b} = \frac{i_e(r_e + R_e)}{i_e(1-\alpha)} = (1+\beta)(r_e + R_e) \tag{80}$$

It says that the input resistance looking into the base is (β + 1) times the total resistance in the emitter. Multiplication by the factor (β + 1) is known as **the resistance-reflection rule**. The factor (β + 1) arises because the base current is 1/(β + 1) times the emitter current.

The expression of the input resistance shows that including a resistance R_e in the emitter can substantially increase the input resistance by the ratio

$$\frac{R_i(\text{with } R_e)}{R_i(\text{without } R_e)} = \frac{(1+\beta)(r_e + R_e)}{(1+\beta)(r_e)} = 1 + \frac{R_e}{r_e} \approx 1 + g_m R_e \tag{81}$$

For the voltage gain, we have

$$A_v = \frac{v_o}{v_s} = \frac{v_o}{v_b}\frac{v_b}{v_s} = \frac{-\alpha R_C}{r_e + R_e}\frac{R_i}{R_i + R_s} \approx \frac{-R_C}{r_e + R_e}\frac{(1+\beta)(r_e + R_e)}{(1+\beta)(r_e + R_e) + R_s} \approx \frac{-\beta R_C}{(1+\beta)(r_e + R_e) + R_s} \tag{82}$$

We note that the gain between base and collector (v_o/v_b) is equal to the ratio of the total resistance in the collector to the total resistance in the emitter. Moreover, the total gain is lower that that for the CE amplifier because of the additional term $(1+\beta)R_e$. The gain, however, is less sensitive to the value of β.

Another important consequence of including the resistance R_e is that the amplifier can handle larger input signals without incurring nonlinear distortion. This is because only a small fraction of the input signal at the base appears between base and emitter. In fact

$$\frac{v_\pi}{v_b} = \frac{r_e}{r_e + R_e} \approx \frac{1}{1 + g_m R_e} \tag{83}$$

shows that for the same v_π, the input signal can be greater than that for the CE amplifier by the factor ($1 + g_m R_e$). Finally, from the circuit, we can see that the output resistance is equal to

$$R_o = R_C \tag{84}$$

and the current gain is

$$A_i = \frac{i_o}{i_b} = -\beta \tag{85}$$

Note:

If we compare the different CE amplifiers, we can see that including a resistance in the emitter results in the following characteristic:

- The input resistance is increased by the factor $\{1+g_m R_e\}$
- For the same nonlinear distortion, we can apply a signal $\{1+g_m R_e\}$ times larger.
- The voltage gain is reduced due to the negative feedback
- The voltage is less dependent on the value of β.

III – Common-base amplifier

Figure IV-38 shows the basic BJT common-base amplifier circuit. Here the base is grounded, the input signal is coupled to the emitter via a large coupling capacitor C_C, and the output signal is taken at the collector.

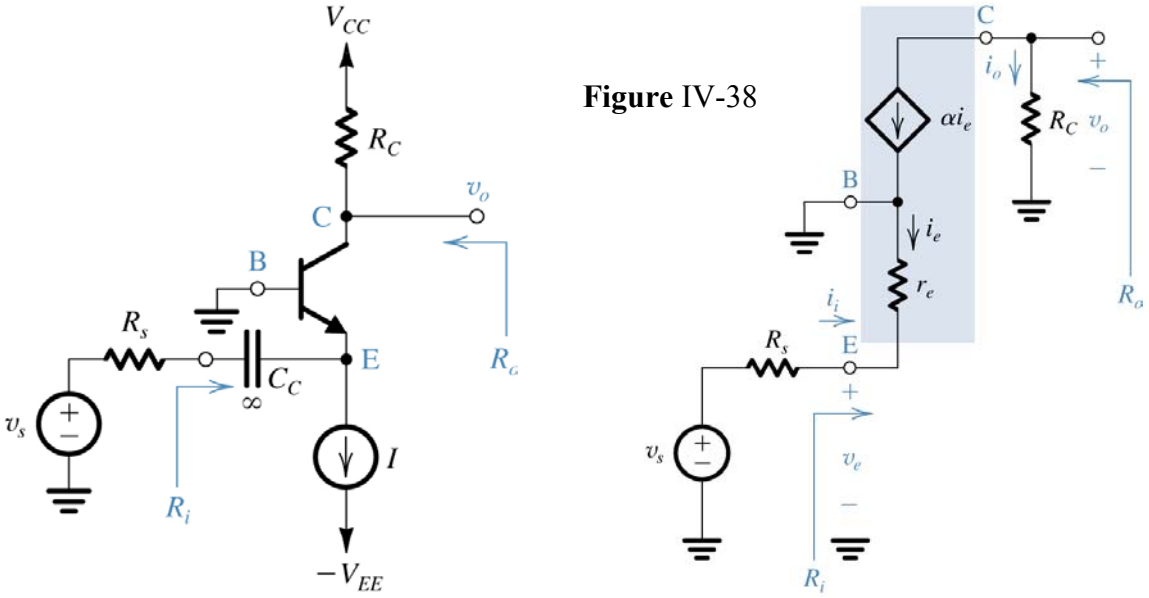


Figure IV-38

Because the input signal is applied to the emitter, it is most convenient to use one of the T models. Note that here we have neglected r_o (including ro complicates the analysis considerably, and it can be verified that its effect on the performance of the CB amplifier is negligible). We have then

$$R_i = r_e \tag{86}$$

Since r_e is quite small (few ohms) we see that the input resistance of the CB amplifier is low. The voltage gain is

$$A_v = \frac{v_o}{v_s} = \frac{-\alpha i_e R_C}{i_e (r_e + R_s)} = \frac{-\alpha R_C}{r_e + R_s} \tag{87}$$

and the current gain is equal to

$$A_i = \frac{i_o}{i_s} = \frac{-\alpha i_e}{-i_e} = \alpha \tag{88}$$

This gain is the common-base short-circuit gain and is very close to unity. Finally the output resistance is equal to

$$R_o = R_C \tag{89}$$

which is relatively small.

IV – Common-collector amplifier

Figure IV-39 shows the basic configuration of the common-collector BJT amplifier (the collector is connected to the positive supply V_{CC} and thus is at signal ground).

The input signal is applied to the base, and the output is taken from the emitter. The main purpose of the CC circuit is to connect a source having a large resistance R_s to a load with a relatively low resistance.

We can observe that the circuit is a simplified version (R_C = 0) of the CE amplifier (Figure IV-40) with a resistance in the emitter ($R_e = r_o // R_L$). The input resistance is then equal to

$$R_i = (1+\beta)(r_e + (r_o // R_L)) \approx (1+\beta) R_L \tag{90}$$

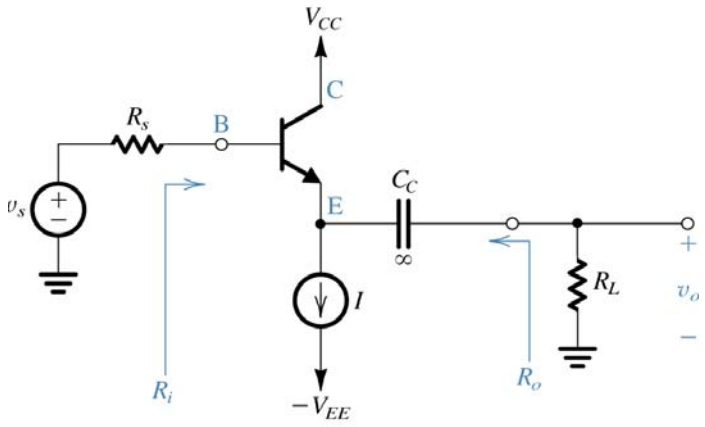


Figure IV-39

for the case { $r_o >> R_L >> r_e$ }. The CC amplifier exhibits a relatively large input resistance. For the voltage gain, we have

$$A_v = \frac{v_o}{v_s} = \frac{v_o}{v_b}\frac{v_b}{v_s} = \frac{(r_o \,//\, R_L)}{r_e + (r_o \,//\, R_L)} \frac{(1+\beta)(r_e + (r_o \,//\, R_L))}{(1+\beta)(r_e + (r_o \,//\, R_L)) + R_s} \tag{91}$$

Another format for this gain is

$$A_v = \frac{(1+\beta)(r_o \,//\, R_L)}{(1+\beta)(r_e + (r_o \,//\, R_L)) + R_s} = \frac{(r_o \,//\, R_L)}{r_e + (r_o \,//\, R_L) + \dfrac{R_s}{1+\beta}} \tag{92}$$

shows that the resistance R_s is divided by the factor (1 + β). **This is the inverse of the resistance reflection rule**.

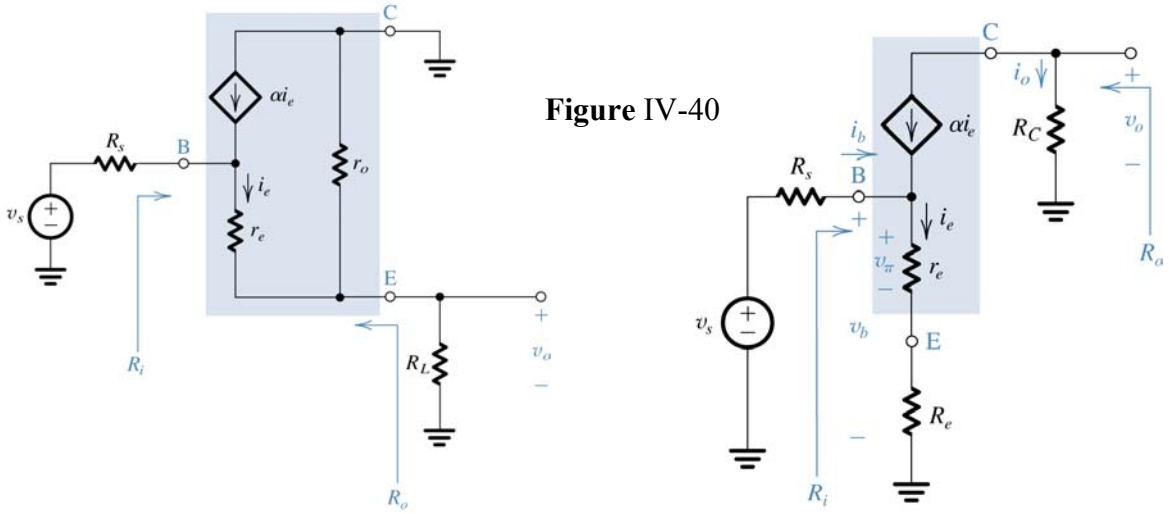


Figure IV-40

Similarly, this factor can be found in the output resistance equation

$$R_o = r_o \,//\left[r_e + \frac{R_s}{1+\beta} \right] \approx r_e + \frac{R_s}{1+\beta} \tag{93}$$

when r_o is large (Figure IV-41). This output resistance is similar to the output resistance of the CE amplifier with a resistance in the emitter, except that here this resistance is divided by the factor $(1 + \beta)$. The voltage and current gains are equal to

$$A_v = \frac{r_o}{r_e + r_o + \dfrac{R_s}{1+\beta}} \frac{R_L}{R_L + R_o} \tag{94}$$

and

$$A_i = (1+\beta)\frac{r_o}{r_o + R_L} \tag{95}$$

which can be approximated to $(1 + \beta)$ when $\{ R_L << r_o \}$.

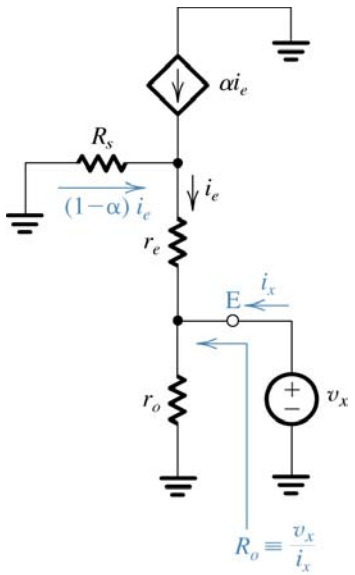


Figure IV-41

Note:

The voltage gain $\{v_o/v_b\}$ is close to unity (r_e is relatively small) which means that the signal at the emitter closely follows that at the base, giving the circuit its most widely used name, **emitter follower**.

K – TRANSISTOR AS A SWITCH-CUTOFF AND SATURATION

To help introduce cutoff and saturation, we consider the simple circuit shown in Figure IV-42.

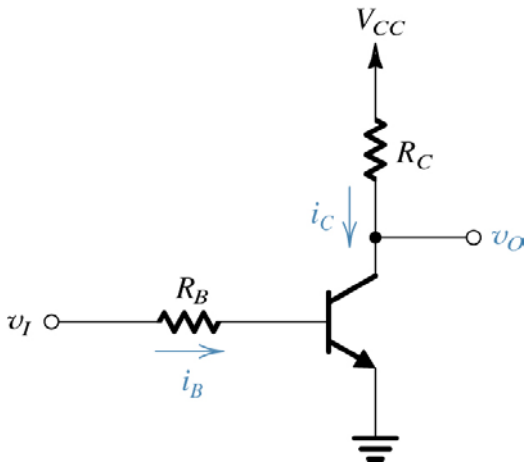


Figure IV-42

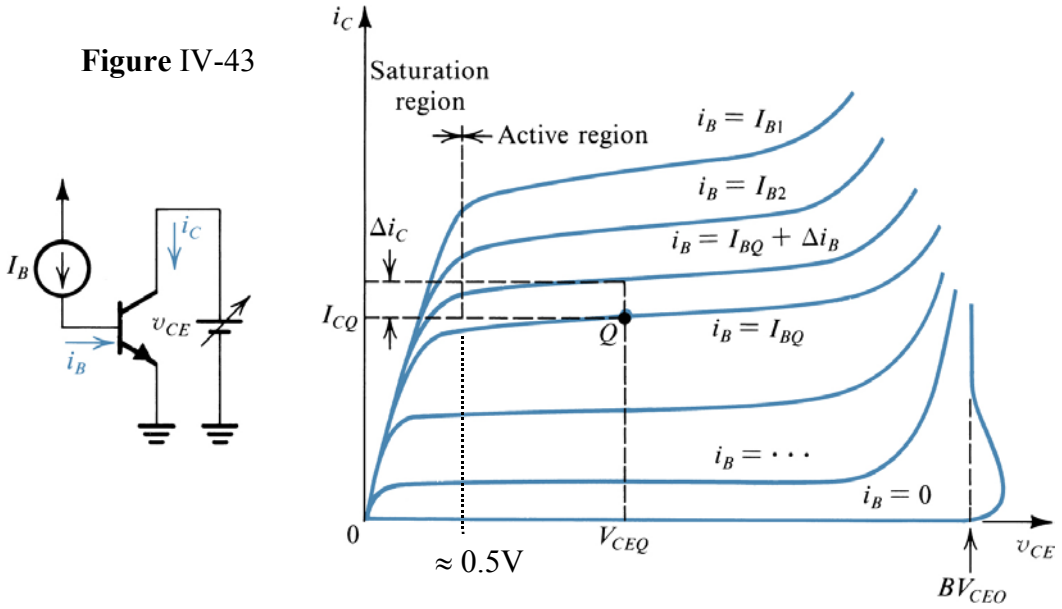
I – Cutoff region

We will analyze this circuit for different values of the voltage source v_i.

If v_i is smaller than about 0.5V, the EB junction will conduct negligible current. In fact, the EB junction could be considered "reverse"-biased, and since the CB junction also is reverse-biased, the device will be in the cutoff mode (Figure IV-43). It follows that

$$i_B = 0 \qquad i_E = 0 \qquad i_C = 0 \qquad v_C = V_{CC} \tag{96}$$

Figure IV-43



II – Active region

To turn the transistor on, we have to increase v_i above 0.5V (practically higher than 0.7V). Thus appreciable currents can flow. We are in the active region.

III – Saturation region

Saturation occurs when we attempt to force a current in the collector higher than the collector circuit can support while maintaining active-mode operation. This collector current is obtained by forcing a base current given by

$$i_B = \frac{v_i - V_{BE}}{R_B} = \frac{i_C}{\beta} \approx \frac{v_i - 0.7}{R_B} \tag{97}$$

Then the collector voltage

$$v_C = V_{CC} - R_C i_C \tag{98}$$

will fall below that of the base v_B (0.7V). We have then reached the saturation region. We can also define the saturation region as the region where the collector current value is too large to maintain the device in the active region.