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SCHOOL OF ELECTRICAL AND ELECTRONICS

DEPARTMENT OF ELECTRONICS AND COMMMUNICATION ENGINEERING

UNIT - I
ANALOG INTEGRATED CIRCUITS – SEC1302

1.1 INTRODUCTION TO OPERATIONAL AMPLIFIER

1.1.1 Integrated Circuit

An Integrated circuit is a miniature electronic circuit comprising of active and passive components irreparably (impossible to rectify or repair) joined together on a single chip of Silicon.

Possible question: *Define Integrated Circuit.*

1.1.2 Advantages of Integrated circuits over discrete component circuits

The integrated circuits are advantageous than that of discrete component circuit with some advantages listed below.

1. Miniaturization and hence density of equipment increased. (Since they are of small size, equipment can hold more components within a same area)
2. Cost is reduced when manufactured in batch processing.
3. Improvised system reliability due to elimination of soldered joints.
4. Complex circuits can be fabricated with better characteristics and thus functional performance is improvised.
5. Increased operating speeds due to minimized parasitic capacitance
6. Power consumption minimized.

Possible question: *List the advantages of IC over discrete circuits.*

1.1.3 Building Blocks of an Operational Amplifier

An operational amplifier is internally built by four blocks namely

1. Unbalanced differential amplifier,
2. Balanced differential amplifier,
3. Buffer and level translator and
4. Output stage (Push-pull Amplifier) as shown in the figure, fig. 1.4.

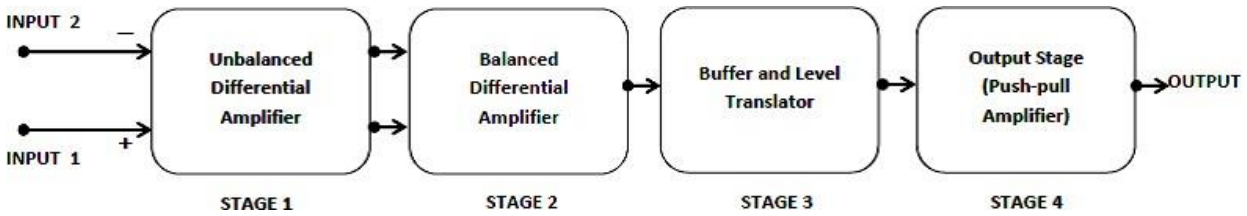


Fig.1.1.3. Building blocks of an OP AMP

Stage 1

This stage offers high impedance to the input terminals. Since it is an unbalanced amplifier, it amplifies the inputs individually with high impedance and the output shall be fed into next stage of balanced amplifier. (Reference figure, fig.1.1.3.1)

Stage 2

Since it is a balanced amplifier, it gives differential output with high gain. This is the stage where high gain is provided and the output is difference between the input signals with low common mode signal. (Reference figure, fig.1.1.3.2)

The above differential amplifiers provide high gain and input impedance with less input current entering into it.

Stage 3

This stage comprises of buffer and level shifter circuits.

Level shifter circuit shifts the reference level of a signal. As shown in figure, fig.1.1.3.3, the input reference level 0.0 is shifted to 2.5 in output signal. Thus this circuit can shift the reference level of the input.

Buffer circuit matches an input circuit of impedance low (or high) with an output load of high (or low) impedance. If they both are connected without this buffer matching circuit, the load drains more current from the input circuit leading to shift of operating point which in turn induces unwanted effect.

Stage 4

Stage four (output stage) is for improvising current, thus a push-pull complementary symmetry amplifier as shown in figure, fig.1.1.3.4. The amplifier separately amplifies positive and negative cycle with NPN and PNP resistors respectively. During positive cycle, current flows into load resistance RL, but in negative cycle current flows from RL in opposite direction. Thus by carefully choosing the value of load resistance, RL, the output amplitude can be varied.

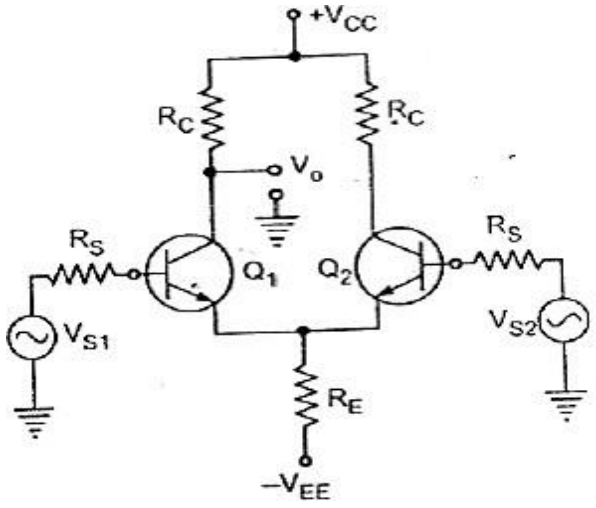


Fig.1.1.3.1. Unbalanced Differential Amplifier

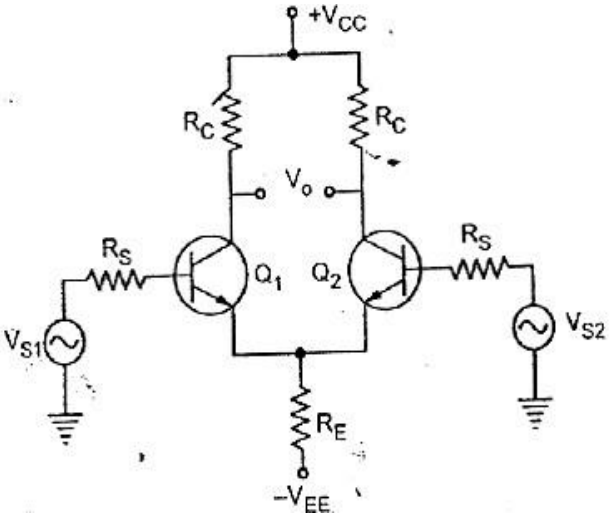


Fig.1.1.3.2. Unbalanced Differential Amplifier

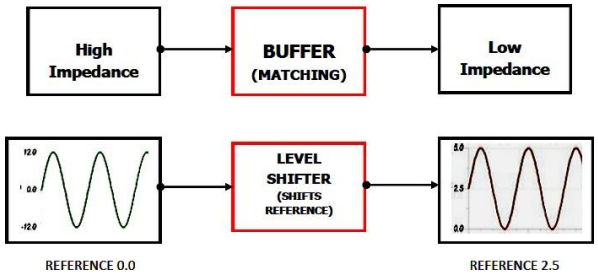


Fig.1.1.3.3. Buffer and Level translator

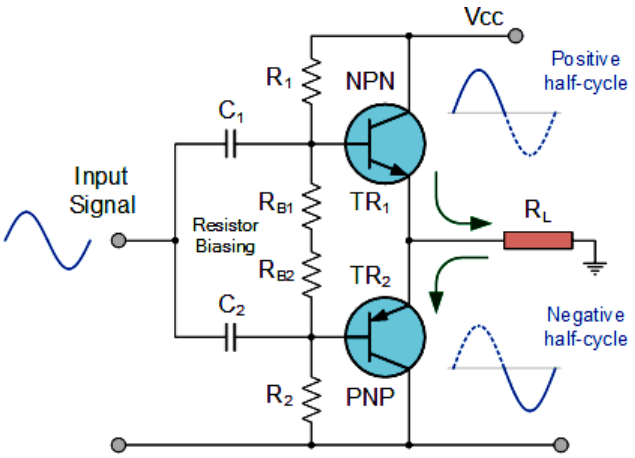


Fig.1.1.3.4. Push-pull Amplifier

Possible question: ***Elaborately explain the building blocks of an operational amplifier with neat sketches.***

1.1.4 Ideal operational amplifier

An Ideal operational amplifier is shown in the figure, fig. 1.1.4.a.

In an ideal op amp,

1. The currents entering the input terminals 1 and 2, i_1 and i_2 respectively, shall be zero. $i_1=i_2=0$.
2. The voltages between reference and the input terminals 1 and 2, V_1 and V_2 respectively, shall be equal. $V_1=V_2$.
3. The difference between input terminal voltages, V_d shall be zero. $V_d=V_2 - V_1$.

As per the figure shown as equivalent circuit, fig. 1.1.4.b, input resistance R_i, output resistance R_o and open loop gain A_{OL} shall be explained further.

4. Input resistance R_i shall be very high (Ideally $R_i=\infty$)
5. Output resistance R_o shall be very low (Ideally $R_o=0$)
6. Open loop gain A_{OL} shall be very high (Ideally $A_{OL}=\infty$)

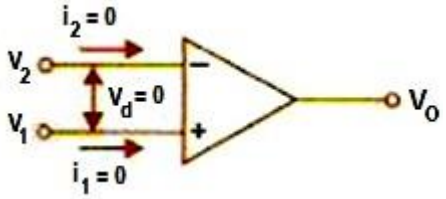


Fig.1.1.4.a. Ideal OP AMP

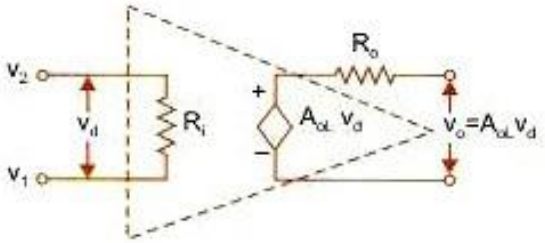


Fig. 1.1.4.b. OP AMP equivalent circuit

Thus ideal op amp shall be an infinite gain amplifier with zero input currents, infinite input resistance and zero output resistance.

Possible question: ***What are all the characteristics of Ideal operational amplifier?***

1.2 DC AND AC CHARACTERISITCS

The two main categories of op amp characteristics are DC and AC Characterisitics.

1.2.1 DC Characteristics

DC characteristics are analyzed when input of the op amp is dc signal. The dc characteristics of op amp and thus it shall be discussed in following section.

1.2.1.1 Input offset voltage (VIOS)

The dc voltage connected any one of the input terminal to make the output offset voltage.

When output offset voltage is more than zero, the non-inverting terminal is supposed to have higher potential than that of inverting terminal due to internal imbalance. So input offset voltage is connected to inverting terminal to compensate the offset and the output voltage to zero.

When output offset voltage is less than zero, the inverting terminal is supposed to have higher potential than that of non-inverting terminal due to internal imbalance. So input offset voltage is connected to non-inverting terminal to compensate the offset and the output voltage to zero.

Thus this dc input offset voltage is known as compensating voltage for output offset voltage.

Possible question: ***Define Input offset voltage, input offset current, input bias current and output offset voltage.***

1.2.1.2 Input bias current (IB)

For an ideal op amp, the dc currents entering the input terminals shall be zero. But practically a minimum amount of current enters the terminals and they are termed as bias currents.

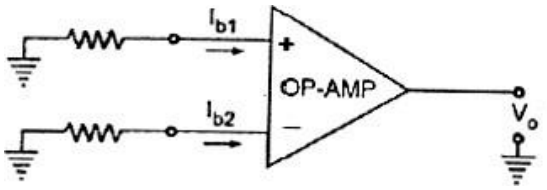


Fig. 1.2.1.2.a. Input bias currents

The bias current entering non-inverting terminal is I_{b1} and entering inverting terminal is I_{b2}. These currents flow into the respective terminals when both input terminals are grounded. The total input bias current is the average currents entering into both the terminals.

$$I_B = \frac{I_{b1} + I_{b2}}{2} \qquad \text{(Eq.1.2.1.2)}$$

1.2.1.3 Input offset current (I_{IOS})

Input dc offset current is the difference between the magnitudes of bias currents I_{b1} and I_{b2} as shown in the equation 1.2.1.3. Practically this current is very small in magnitude in the order of nano-amperes.

$$I_b = I_{b1} - I_{b2} \qquad \text{(Eq.1.2.1.3)}$$

1.2.1.4 Total Output offset voltage (V_{OOS})

As shown in the figure, fig.1.2.1.2.a, when both the inputs are connected to ground potential, the output dc voltage V_o should be zero ideally. But practically the output voltage is not zero. The value of this output voltage is termed as Total output offset voltage.

1.2.2 AC characteristics

AC characteristics are analyzed when input of the op amp is ac signal. Slew rate is a major ac characteristic of op amp and thus it shall be discussed in next section.

1.2.2.1 Slew rate

Slew rate is defined as the maximum rate of change of output voltage with time.

For this, a voltage follower circuit is chosen where output is fed-back directly to inverting terminal and the inverting terminal is connected to a rectangular pulse of 50% duty cycle (Square wave) as shown in figure, fig.1.2.2.1.a.

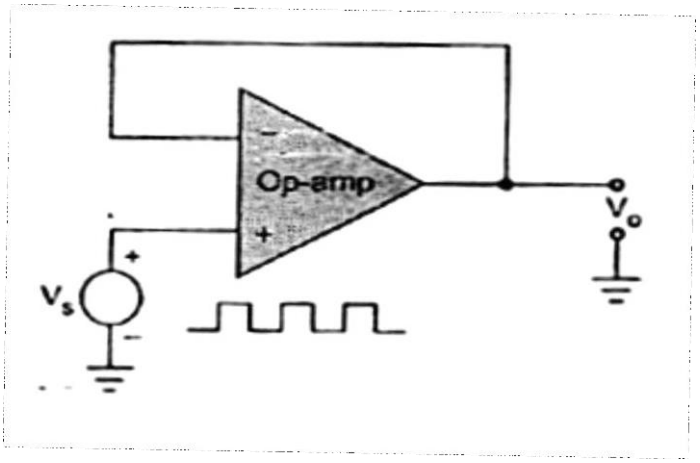


Fig. 1.2.2.1.a Measurement of slew rate of OP AMP

The output V_o is to follow the input. But as shown in figure, fig.1.2.2.1.b, the output wave is distorted and not a rectangular wave as input. Thus the variation of output is denoted by dV_o, change in voltage with change in time dt. Thus maximum change in output voltage with change in time is

$$\text{Slew rate} = S = \left.\frac{dV_o}{dt}\right|_{max}$$

This is due to charging and discharging rate of an internal capacitance C of the op amp. The capacitor charges to maximum current I_{max} due to the input voltage fed in the capacitor. The sudden change in input voltage from low to high, allows the capacitor to charge to its maximum. Thus change in output voltage dV_o/dt mainly depends upon charging current I_{max} and the capacitance C.

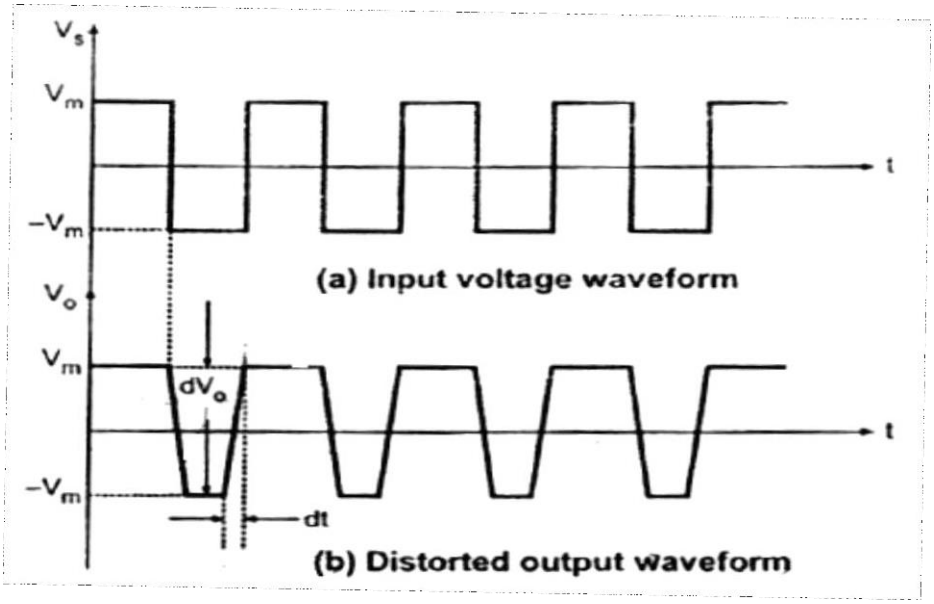


Fig.1.2.2.1.b.slewratewaveforms

Thus slew rate in terms of internal capacitance C is

$$S = \frac{I_{max}}{C}$$

Slew Rate Equation

Let the input voltage V_S is purely sinusoidal. In this case the output voltage V_O will be also purely sinusoidal, as the circuit used to derive the equation is voltage follower circuit as shown in the fig.1.2.2.1 (a). in such circuit output voltage follows input voltage.

So

$$V_i = V_m \sin\omega t$$

And

$$V_i = V_m \sin\omega t$$

$$\frac{dV_o}{dt} = V_m(\omega \cos\omega t)$$

But $\frac{dV_o}{dt}$ maximum is nothing but the slew rate S. For maximum $\frac{dV}{}$, in the equation above cos(□t) must be maximum. i.e.1.

$$S = \left[\frac{dV_o}{dt}\right]_{max} = \omega V_m$$

$$\boxed{S = 2\pi f V_m \quad V/sec}$$

This is required slew-rate equation.

For the distortion free output, the maximum allowable frequency of operation f_m can be decided by the slew rate.

Methods of improving Slew rate

It is known that the slew rate is given by,

$$S = \frac{I_{max}}{C}$$

For understanding the methods of improving slew rate consider the op-amp model for the analysis of the slew rate as shown in the Fig. 1.2.2.3.

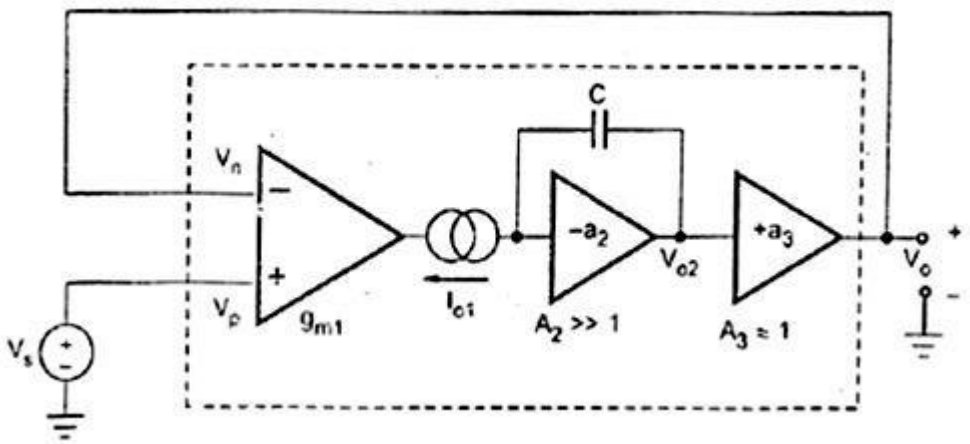


Fig.1.2.2.3 Op-amp model for slew rate analysis

The op-amp used is in voltage follower mode in which the output $V_o = V_i$. The circuit is similar to that used earlier to derive slew rate equation, only the op-amp is replaced by its model.

When input overdrives the input stage then $I_{max} = \pm I_{01}$ (sat) which are saturation current levels of the input stage. Under this condition, op-amp is said to be operating under large-signal conditions.

The saturation of the input stage limits the slew rate because under saturation condition, the rate at which capacitor C can charge or discharge, according to the input overdrive is at its maximum.

From the fig.1.2.2.3, we can write,

$$I_{01}(sat) = C\frac{dV_{02}}{dt}$$

$$\therefore \frac{dV_{02}}{dt} = \frac{I_{01}(sat)}{C}$$

This rate of change of V_{02} is maximum, due to the saturation effect. Now

the gain of the third stage $a_3 \approx 1$, hence $V_0 = V_{02}$,

$$\therefore \left(\frac{dV_{02}}{dt}\right)_{max} = \frac{dV_{02}}{dt} = \frac{I_{01}(sat)}{C}$$

But maximum rate of change of output voltage is the slew rate.

$$S = \frac{I_{01}(sat)}{C}$$

Analyzing the op-amp model used, we can write,

$$V_{02} = drop across C = I_{01}Z_C$$

The input stage is a transconductance amplifier. i.e. voltage input, current output amplifier. For sufficiently small differential input voltage the relation between input voltage and output current for such an amplifier is,

$$Output Current = g_m(differential Input)$$

or inputstage

$$\therefore I_{01} = g_{m1}(V_p - V_n)$$

$$\therefore V_{02} = Z_C g_{m1}(V_p - V_n)$$

But,

$$V_{02} \approx V_o \; as \; a_3 \approx 1$$

$$\therefore V_0 = Z_C g_{m1}(V_p - V_n)$$

$$V_0 = \left[\frac{1}{j\omega C}\right] g_{m1}(V_p - V_n)$$

As,

$$Z_C = X_C = \left[-\frac{j}{\omega C}\right] = \frac{1}{j\omega C}$$

$$\therefore Op - amp\ gain = \frac{|V_o|}{|V_p - V_n|}$$

$$\therefore |a| = \frac{|V_o|}{|V_p - V_n|} = \frac{g_{m1}}{\omega C} = \frac{g_{m1}}{2\pi f C}$$

$$\therefore |a|f = \frac{g_{m1}}{2\pi C}$$

Here in the above equation Saturation current *I01(sat)*, mutual conductance *gm1*, and gain-bandwidth product *ft* of the op amp can be set in accordingly to improve *slew rate.*

Improving slew rate by

1. Increasing saturation current *I01(sat)* : This is very tough to increase because this may affect the operating point of the transistors used in the circuit.

2. Increasing gain-bandwidth product *ft* : This is done by using feed-forward compensation. That is two op amps connected in series that one's output is fed into other. This improves the bandwidth by increasing gain-bandwidth product, thus improving slew rate.

***3.* Decreasing mutual conductance *gm1* : This is done by replacing BJT by FET's. Normally FET's are having less mutual conductance *gm* by improving slewrate.**

Possible question: ***Define slew rate and write the slew rate equation. Explain about the methods of improving slew rate.***

1.2.2.2 Thermal drift

In op amp, effect of variation in all parameters is severe due to variations in temperature.

Effect on input offset voltage

Input offset voltage varies with variation in temperature and thus ratio of change in input offset voltage to change in temperature is termed as *thermal drift on input offset voltage.*

$$Inputoffsetvoltagedrift = \frac{\Delta V_{ios}}{\Delta T} \qquad \textbf{(Eq.1.2.2.2.1)}$$

Where ΔT- change in temperature, ΔV_{ios}- change in input offset voltage

Effect on input offset current

Input offset current varies with variation in temperature and thus ratio of change in input offset current to change in temperature is termed as *thermal drift on input offset current.*

$$Input offset current drift = \frac{\Delta I_{os}}{\Delta T}$$ **(Eq.1.2.2.2.2)**

Where ΔT**- change in temperature,** ΔI_{os}**- change in input offset current**

Effect on input bias current

Input bias current varies with variation in temperature and thus ratio of change in input bias current to change in temperature is termed as *thermal drift on input bias current.*

$$Input bias current drift = \frac{\Delta I_{ib}}{\Delta T}$$ **(Eq.1.2.2.2.3)**

Where ΔT**- change in temperature,** ΔI_{ib}**- change in input bias current**

Effect on slew rate

Slew rate varies with variation in temperature and thus ratio of change in slew rate to change in temperature is termed as *thermal drift on slew rate.*

$$slew rate drift = \Delta S / \Delta T$$ **(Eq.1.2.2.2.4)**

Where ΔT**- change in temperature,** ΔS**- change in slew rate**

Possible question: *Explain Thermal drift on various parameters of op amp.*

1.2.2.3 Common Mode Rejection Ratio -CMRR

When the same voltage is applied to both the terminals of op amp, then the op amp is said to be operated in common mode configuration. Op amp is to be operated only in differential mode and common mode signals shall be noise or disturbance signal. The ability of differential amplifier is to reject the common mode signal and expressed as a ratio termed as Common mode rejection ratio (CMRR).

It is defined as ratio of the differential voltage gain (A_d) to common

$$CMRR = \rho = \left|\frac{A_d}{A_c}\right|$$

$$CMRR \text{ in } dB = 20 log \left|\frac{A_d}{A_c}\right| \text{ in } dB$$

Practically CMRR should be larger and ideally it shall be ∞.

Possible questions: *Define CMRR.*

Open loop and closed loop configurations

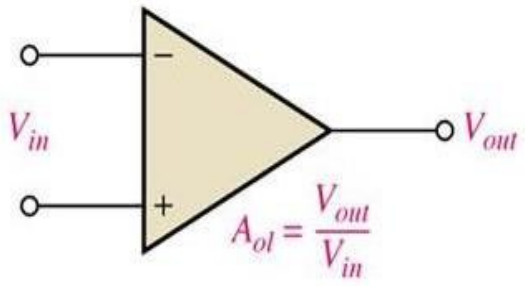


Fig.1.2.3.a Open loop configuration

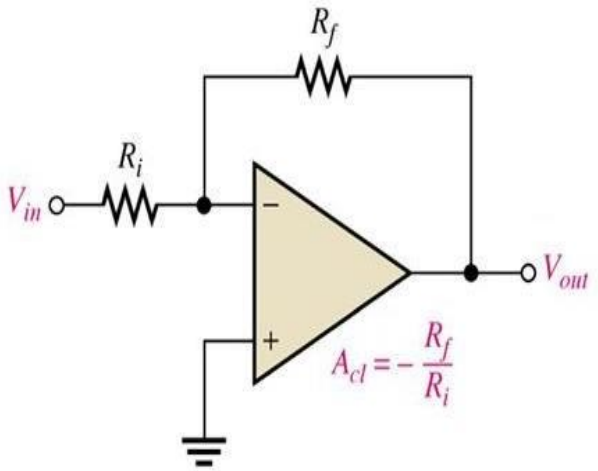


Fig.1.2.3.b Closed loop configuration

Open loop configuration

As shown in figure, fig.1.2.3.a, V_{in} is the input given between input terminals and V_{out} is the output derived. The open loop gain A_{ol} is ratio of the output voltage (V_{out}) to the input voltage (V_{in}).

$$\text{The open loop gain, } A_{ol} = \frac{V_{out}}{V_{in}} \qquad \text{(Eq.1.2.3.1)}$$

As stated above in eq.1.2.3.1, the gain cannot be controlled or changed. Thus this gain is implicit (in-built) and never be changed explicitly. This gain is very large in terms of 10000.

Closed loop configuration

As shown in figure, fig.1.2.3.b, V_{in} is the input given into inverting terminal through a resistance R_i and a feed-back resistor R_f connected between output terminal and inverting terminal. V_{out} is the output derived. The open loop gain A_{cl} is ratio of the feed-back resistor (R_f) to the resistance (R_i). The feedback is *negative*.

$$\text{The closed loop gain, } A_{cl} = -\frac{Rf}{R_i} \qquad \text{(Eq.1.2.3.2)}$$

As stated above in eq.1.2.3.2, the gain now can be controlled or changed. Thus this gain is explicit and by changing the resistor values, gain can be altered.

Thus closed loop gain is advantageous over open loop gain because it can be changed by changing resistor values.

Possible question: *Elaborately explain open loop and closed loop configurations of an op amp with neat sketches.*

1.3.1 OP-AMP used in mathematical operations

1.3.1 Inverting Amplifier

The amplifier in which the output is inverted i.e. having 180^0 phase shift with respect to the input is called an inverting amplifier.

This is possibly the most widely used of all the op-amp circuits. The circuit is shown in Fig. 1.3.1.The output voltage V_o is fed back to the inverting input terminal through the $R_f - R_1$ network where R_f is the feedback resistor. Input signal v_i is applied to the inverting input terminal through R_1 and non-inverting input terminal of op-amp is grounded.

Assume an ideal op-amp. As $V_d = 0$, node 'a' is at ground potential and the current i_1 through R_1 is

$$i_1 = \frac{v_i}{R_1}$$

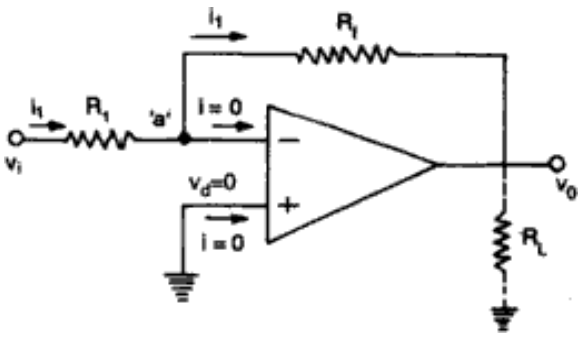


Fig. 1.3.1. Inverting amplifier

Also since op-amp draws no current, all the current flowing through R_1 must flow through R_f. The output voltage is given by

$$v_o = -i_1 R_f = -v_i \frac{R_f}{R_1}$$

Hence, the gain of the inverting amplifier (also referred as closed loop gain) is given by

$$A_{CL} = \frac{v_o}{v_i} = -\frac{R_f}{R_1}$$

Alternatively, the nodal equation at the node 'a' in Fig. 1.3.1 is given by

$$\frac{v_a - v_i}{R_1} + \frac{v_a - v_o}{R_f} = 0$$

where v_a is the voltage at node 'a'. Since node 'a' is at virtual ground v_a=0. Therefore, we get,

$$A_{CL} = \frac{v_o}{v_i} = -\frac{R_f}{R_1}$$

1.3.2 Non-Inverting Amplifier

The amplifier in which the output is amplified without any phase shift in between input and output is called non inverting amplifier.

If the signal is applied to the non-inverting input terminal and feedback is given as shown in Fig. 1.3.2. The circuit which amplifies without inverting the input signal. It may be noted that it is also a negative feed-back system as output is being fed back to the inverting input terminal.

As the differential voltage V_d at the input terminal of op-amp is zero, the voltage at node 'a' in Fig. 1.3. 2. is V_i same as the input voltage applied to non-inverting input terminal. Now R_f and R_1 form a potential divider. Hence

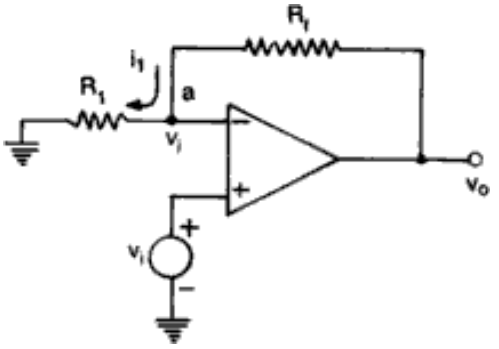


Fig. 1.3.2 Non-inverting amplifier

$$v_i = \frac{v_o}{R_1 + R_f} R_1$$

As no current flows into the op-amp.

$$\frac{v_o}{v_i} = \frac{R_1 + R_f}{R_1} = 1 + \frac{R_f}{R_1}$$

Thus, for non-inverting amplifier the voltage gain,

$$A_{CL} = \frac{v_o}{v_i} = 1 + \frac{R_f}{R_1}$$

The gain can be adjusted to unity or more, by proper selection of resistors Rf and R1. Compared to the inverting amplifier, the input resistance of the non-inverting amplifier is extremely large (= □) as the op-amp draws negligible current from the signalsource.

1.3.3 Voltage Follower

In the non-inverting amplifier of Fig. 1.3.1, if Rf = 0 and R1 = □ , we get the modified circuit of Fig. 1.3.3. The voltage equation becomes

$$v_o = v_i$$

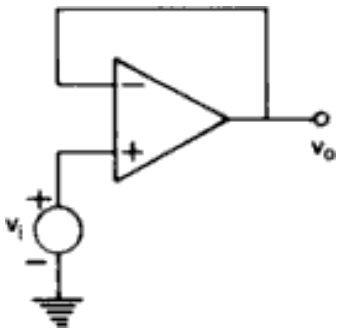


Fig. 1.3.3. Voltage follower

That is, the output voltage is equal to input voltage, both in magnitude and phase. In other words, we can also say that the output voltage follows the input voltage exactly. Hence, the circuit is called a voltage follower. The use of the unity gain circuit lies in the fact that its input impedance is very high (i.e. MΩ order) and output impedance is zero. Therefore, it draws negligible current from the source. Thus a voltage follower may be used as buffer for impedance matching, that is, to connect a high impedance source to a low impedance load.

1.3.4 SUMMING AMPLIFIER

Op-amp may be used to design a circuit whose output is the sum of several input signals. Such a circuit is called a summing amplifier or a summer. An inverting summer or a non-inverting summer may be obtained as discussed now.

1.3.4.1 Inverting summing amplifier

A typical summing amplifier with three input voltages V1, V2 and V3, three input resistors R1, R2, R3 and a feedback resistor Rf is shown in Fig. 1.3.4.1. The following analysis is carried out assuming that the op-amp is an ideal

one, that is, $A_{OL} = \infty$ and $R_i = \infty$. Since the input bias current is assumed to be zero, there is no voltage drop across the resistor R_{Comp} and hence the non-inverting input terminal is at ground potential.

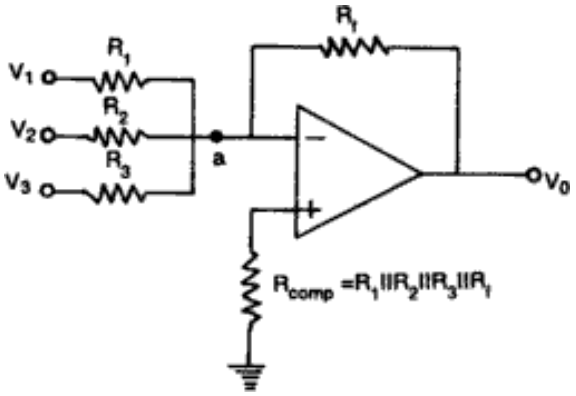


Fig. 1.3.4.1 Inverting Summing Amplifier

The voltage at node 'a' is zero as the non-inverting input terminal is grounded. The nodal equation by KCL at node 'a' is

$$\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} + \frac{V_o}{R_f} = 0$$

$$V_o = -\left(\frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 + \frac{R_f}{R_3} V_3\right)$$

Thus the output is an inverted, weighted sum of the inputs. In the special case, when $R_1 = R_2 = R_3 = R_f$, we have

$$V_o = -(V_1 + V_2 + V_3)$$

in which case the output V_o. is the inverted sum of the input signals. We may also set

$$R_1 = R_2 = R_3 = 3R_f,$$

in which case

$$V_o = -\left(\frac{V_1 + V_2 + V_3}{3}\right)$$

Thus the output is the average of the input signals (inverted). In a practical circuit, input bias current is compensated by using resistor R_{comp}. To find R_{comp}, make all inputs $V_1 = V_2 = V_3 = 0$. So the effective input resistance $R_i = R_1 \text{IIR}_2 \text{IIR}_3$. Therefore $R_{comp} = R_i \text{IIR}_f = R_1 \text{IIR}_2 \text{IIR}_3 \text{IIR}_f$.

Design an adder circuit using an op-amp to get the output expression as

$$V_o = -(0.1\ V_1 + V_2 + 10\ V_3)$$

where V_1, V_2, and V_3 are the inputs.

Solution

The output in Fig. 4.2 (a) is

$$V_o = -[(R_f/R_1)\ V_1 + (R_f/R_2)V_2 + (R_f/R_3)V_3]$$

say $R_f = 10\ \text{k}\Omega,\ R_1 = 100\ \text{k}\Omega,\ R_2 = 10\ \text{k}\Omega,\ R_3 = 1\ \text{k}\Omega$

Then the desired output expression is obtained.

1.3.4.2 Non-inverting Summing Amplifier

A summer that gives a non-inverted sum is the non-inverting summing amplifier and is shown in fig.1.3.4.2. Let the voltage at the (-) input terminal be V_a. The voltage at (+) input terminal will also be V_a. The nodal equation at node 'a' is given by

$$\frac{V_1 - V_a}{R_1} + \frac{V_2 - V_a}{R_2} + \frac{V_3 - V_a}{R_3} = 0$$

From which we have

$$V_a = \frac{\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}}{\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}}$$

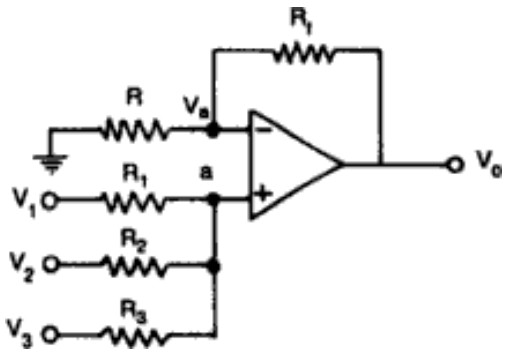


Fig. 1.3.4.2 Non-inverting summing amplifier

The op-amp and two resistors R_f and R constitute a non-inverting amplifier with

$$V_o = \left(1 + \frac{R_f}{R}\right) V_a$$

Therefore, the output voltage is

$$V_o = \left(1 + \frac{R_f}{R}\right) \frac{\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right)}{\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}}$$

which is a non-inverted weighted sum of inputs.

Let R1 = R2 = R3 = R = Rf / 2. Then, V_o = VI + V2 + V3

1.3.5 Differential Amplifier (Subtracting Amplifier)

The basic difference amplifier can be used as a subtractor or subtracting amplifier as shown in below fig.1.3.5

If all resistors are equal in value, then the output voltage can be derived by using superposition principle. To find the output V_{01} due to V_1 alone, make V_2=0. Then the circuit of fig.1.3.5 becomes a non-inverting amplifier having input voltage $V_1/2$ at the non-inverting input terminal and the output becomes

$$V_{01} = \frac{V_1}{2}\left(1 + \frac{R}{R}\right) = V_1$$

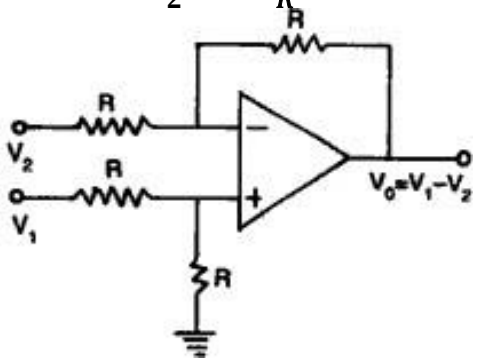


Fig.1.3.5 Subtractor or Subtracting Op-amp

Similarly the output V_{02} due to V_2 alone (with V_1 grounded) can be written simply for an inverting amplifier as

$$V_{02} = -V_2$$

Thus the output voltage V_0 due to both the inputs can be written as

$$V_0 = V_{01} + V_{02} = V_1 - V_2$$

Hence the output voltage V_o is subtraction of input voltages V_1 and V_2.

1.3.6 DIFFERENTIATOR

One of the simplest of the op-amp circuits that contain capacitor is the differentiating amplifier, or differentiator. As the name suggests, the circuit performs the mathematical operation of differentiation, that is, the output waveform is the derivative of input waveform. A differentiator circuit is shown in Fig. 1.3.6.

The node N is at virtual ground potential i.e., $v_N = 0$. The current i_C through the capacitor is,

$$i_C = C_1 \frac{d}{dt}(v_i - v_N) = C_1 \frac{dv_i}{dt}$$

The current i_f through the feedback resistor is v_o/R_f and there is no current into the op-amp. Therefore, the nodal equation at node N is,

$$C_1 \frac{dv_i}{dt} + \frac{v_o}{R_f} = 0$$

from which we have

$$v_o = -R_f C_1 \frac{dv_i}{dt}$$

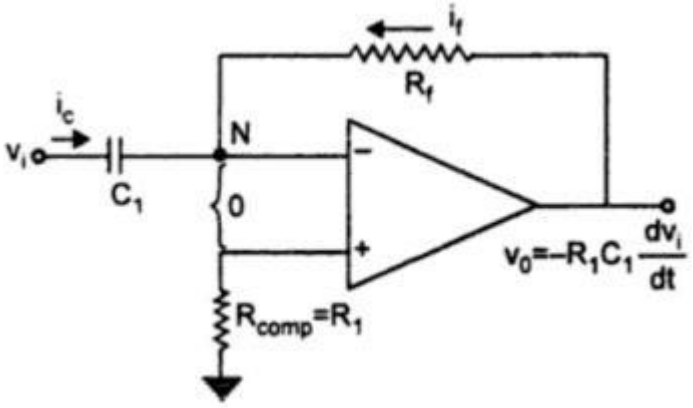


Fig. 1.3.6 Differentiator

Thus the output voltage v_o is a constant ($-R_f C_1$) times the derivative of the input voltage v_i and the circuit is a differentiator. The minus sign indicates a 180° phase shift of the output waveform v_o with respect to the input signal.

The phasor equivalent is, $V_o(s) = -R_f C_1 s V_i(s)$ where V_o and V_i is the phasor representation of v_o and v_i. In steady state, put $s = j\omega$. We may now write the magnitude of gain A of the differentiator as,

$$|A| = \left| \frac{V_o}{V_i} \right| = \left| - j\omega R_f C_1 \right| = \omega R_f C_1$$

one can draw the frequency response of the op-amp differentiator. Equation (4.70) may be rewritten as

$$|A| = \frac{f}{f_a}$$

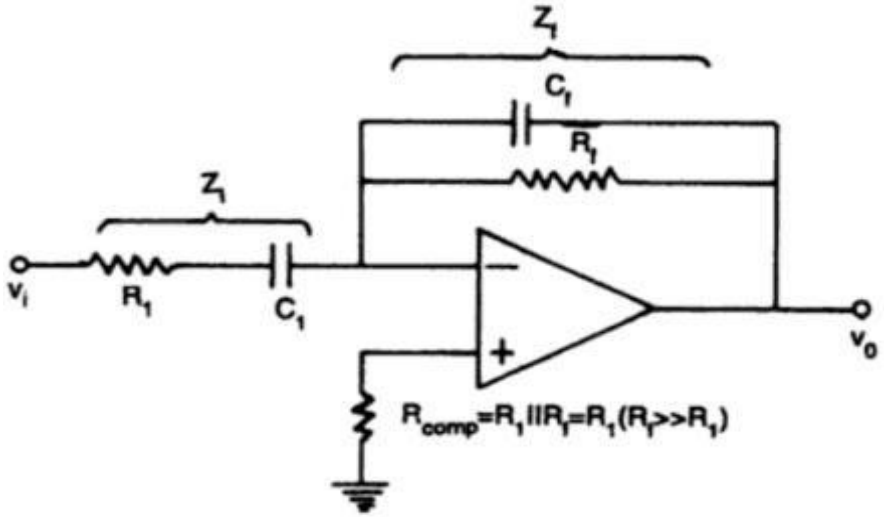
where $$f_a = \frac{1}{2\pi R_f C_1}$$

At $f = f_a$, $|A| = 1$, i.e., 0 dB, and the gain increases at a rate of +20 dB/decade. Thus at high frequency, a differentiator may become unstable and break into oscillation. There is one more problem in the differentiator of Fig. The input impedance (i.e., $1/\omega C_1$) decreases with increase in frequency, thereby making the circuit sensitive to high frequency noise.

A practical differentiator of the type shown in Fig. eliminates the problem of stability and high frequency noise.

The transfer function for the circuit in Fig. is given by,

$$\frac{V_o(s)}{V_i(s)} = -\frac{Z_f}{Z_i} = -\frac{s R_f C_1}{(1 + s R_f C_f)(1 + s C_1 R_1)}$$



1.3.6.1 Practical DifferentiatorFig. 1.3.6.1 Practical Differentiator

For $R_f C_f = R_1 C_1$, we get

$$\frac{V_o(s)}{V_i(s)} = -\frac{sR_f C_1}{(1 + sR_1 C_1)^2} = -\frac{sR_f C_1}{\left(1 + j\frac{f}{f_b}\right)^2}$$

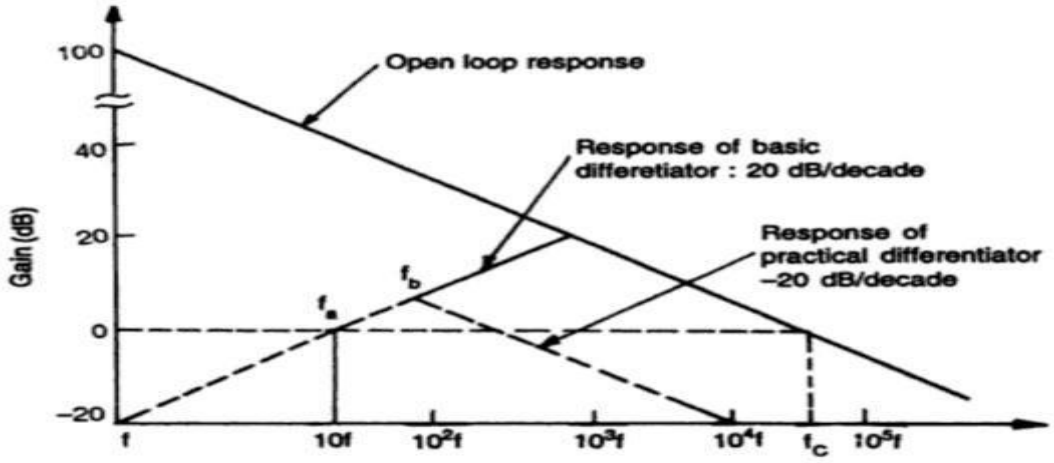


Fig. 1.3.6.2 Frequency response of Differentiator

where, $$f_b = \frac{1}{2\pi R_1 C_1}$$

From Eq. it is evident that the gain increases at +20 dB/ decade for frequency $f < f_b$ and decreases at –20 dB/decade for $f > f_b$ as shown by dashed lines in Fig. . This 40 dB/decade change in gain is caused by $R_1 C_1$ and $R_f C_f$ factors. For the basic differentiator of Fig. the frequency response would have increased continuously at the rate of +20 dB/decade even beyond f_b causing stability problem at high frequency. Thus the gain at high frequency is reduced significantly, thereby avoiding the high frequency noise and stability problems. The value of f_b should be selected such that,

$$f_a < f_b < f_c$$

where f_c is the unity gain-bandwidth of the op-amp in open-loop configuration.

For good differentiation, one must ensure that the time period T of the input signal is larger than or equal to $R_f C_1$, that is,

$$T \geq R_f C_1$$

It may be noted that for $R_f C_1$ much greater than $R_1 C_1$ or $R_f C_f$, Eq. is reduced to, $V_o/V_i = -sR_f C_1$, that is, the expression of the output voltage remains the same as in the case of an ideal differentiator as

$$v_o = -R_f C_1 \frac{dv_i}{dt}$$

A resistance R_{comp} ($= R_1 \| R_f$) is normally connected to the (+) input terminal to compensate for the input bias circuit.

A good differentiator may be designed as per the following steps:

1. Choose f_a equal to the highest frequency of the input signal. Assume a practical value of C_1 (< 1μF) and then calculate R_f.
2. Choose $f_b = 10\, f_a$ (say). Now calculate the values of R_1 and C_f so that $R_1 C_1 = R_f C_f$.

Example

(a) Design an op-amp differentiator that will differentiate an input signal with $f_{max} = 100$ Hz.
(b) Draw the output waveform for a sine wave of 1V peak at 100 Hz applied to the differentiator.
(c) Repeat part (b) for a square wave input.

(a) select, $f_a = f_{max} = 100 \text{ Hz} = \dfrac{1}{2\pi R_f C_1}$

Let $C_1 = 0.1\ \mu\text{F}$,

then $R_f = \dfrac{1}{2\pi (10^2)(10^{-7})} = 15.9\ \text{k}\Omega$

Now choose $f_b = 10 f_a$

$= 1\ \text{kHz}$

$= \dfrac{1}{2\pi R_1 C_1}$

Therefore, $R_1 = \dfrac{1}{2\pi (10^3)(10^{-7})} = 1.59\ \text{k}\Omega$

Since $R_f C_f = R_1 C_1$,

we get, $$C_f = \frac{1.59 \times 10^3 \times 10^{-7}}{15.9 \times 10^3} = 0.01\,\mu F$$

(b) $v_i = 1 \sin 2\pi(100)t$

From Eq.

$$v_o = -R_f C_1 \frac{dv_i}{dt}$$

$$= -(15.9\ k\Omega)\ (0.1\mu F)\ \frac{d}{dt}[(1\ V) \sin (2\pi)\ (10^2)\ t]$$

$$= -(15.9\ k\Omega)\ (0.1\ \mu F)\ (2\pi)\ (10^2) \cos [(2\pi)\ (10^2)t]$$

$$= -0.999 \cos [2\pi\ (10^2)t]$$

$$= -1 \cos [(2\pi)\ (10^2)\ t]$$

The input and output waveforms are shown in Fig. (a).

(c) For a square wave input, say 1V peak and 1 KHz, the output waveform will consist of positive and negative spikes of magnitude V_{sat} which is approximately 13V for ± 15V op-amp power supply. During the time periods for which input is constant at ± 1V, the differentiated output will be zero. However, when input transits between ± 1V levels, the slope of the input is infinite for an ideal square wave. The output, therefore, gets clipped to about ± 13V for a ± 15V op-amp power supply as shown in Fig. (b).

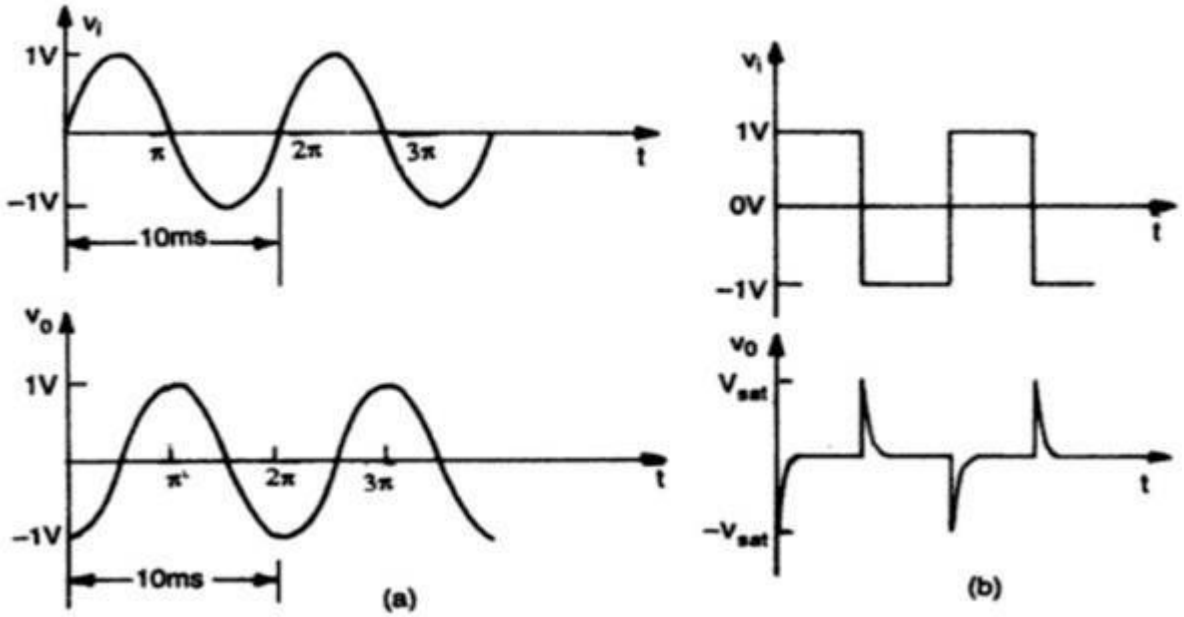


Fig. 1.3.6.3 (a) Sine-wave input and cosine output (b) Square wave input and spike output

1.3.7 INTEGRATOR

If we interachange the resistor and capactior of the differenetiator of Fig 1.3.6 (Differentiator), we have the circuit of Fig.1.3.7 which as we will see, is an integrator. The nodal equation at node N is,

$$\frac{v_i}{R_1} + C_f \frac{dv_o}{dt} = 0$$

$$\frac{dv_o}{dt} = -\frac{1}{R_1 C_f} v_i$$

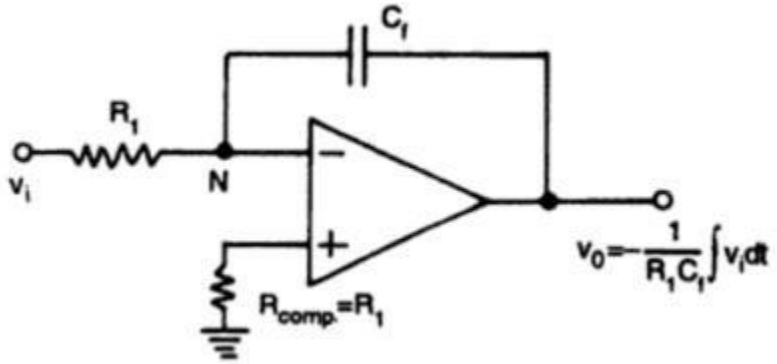


Fig. 1.3.7 Integrator

Integrating both sides, we get,

$$\int_0^t dv_o = -\frac{1}{R_1 C_f}\int_0^t v_i\, dt$$

$$v_o(t) = -\frac{1}{R_1 C_f}\int_0^t v_i(t)\, dt + v_o(0)$$

where $v_o(0)$ is the initial output voltage.

The circuit, thus provides an output voltage which is proportional to the time integral of the input and R_1C_f is the time constant of the integrator. It may be noted that there is a negative sign in the output voltage, and therefore, this integrator is also known as an inverting integrator. A resistance, $R_{comp} = R_1$ is usually connected to the (+) input terminal to minimize the effect of input bias current.

The operation of the integrator can also be studied in the frequency domain. In phasor notation, Eq. can be written as

$$V_o(s) = -\frac{1}{sR_1C_f}V_i(s)$$

In steady state, put $s = j\omega$ and we get

$$V_o(j\omega) = -\frac{1}{j\omega R_1 C_f}V_i(j\omega)$$

So, the magnitude of the gain or integrator transfer function is

$$|A| = \left|\frac{V_o(j\omega)}{V_i(j\omega)}\right| = \left|-\frac{1}{j\omega R_1 C_f}\right| = \frac{1}{\omega R_1 C_f}$$

The frequency response or Bode Plot of this basic integrator is shown in the fig.1.3.7. The bode plot is a straight line of slope -6 dB/ Octave or equivalently -20 dB/Decade. The frequency *fb*, in fig.1.3.7 is the frequency at which the gain f the integrator is 0 dB and is given by

$$f_b = \frac{1}{2\pi R_1 C_f}$$

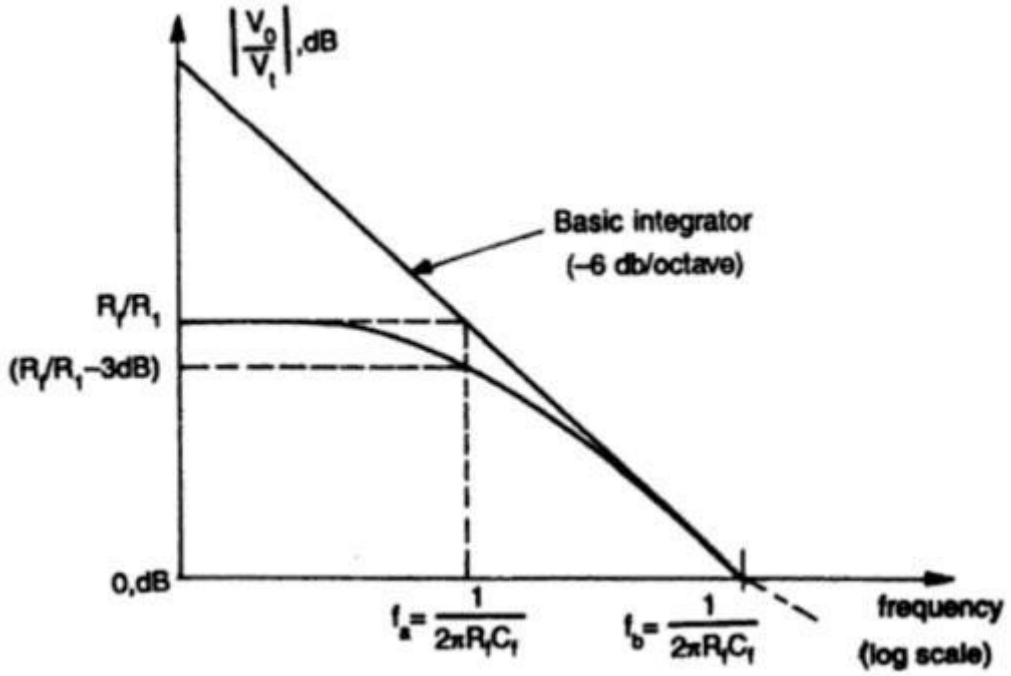


Fig. 1.3.7.1 Frequency response of basic and lossy integrator

As the gain of the integrator decreases with increasing frequency, the integrator circuit does not have any frequency problem as faced in a differentiator. However, at low frequencies such as at dc ($\omega \cong 0$), the gain becomes infinite (or saturates). The solution to this problem is discussed in the following.

1.3.7.1 Practical Integrator (Lossy Integrator)

The gain of an integrator at low frequency (dc) can be limited to avoid the saturation problem if the feedback capacitor is shunted by a resistance R_f as shown in Fig. 2.15 . The parallel combination of R_f and C_f behaves like a practical capacitor which dissipates power unlike an ideal capacitor. For this reason, this circuit is also called a lossy integrator. The resistor R_f limits the low frequency gain to $-R_f/R_1$ (generally $R_f = 10\ R_1$) and thus provides dc stabilization.

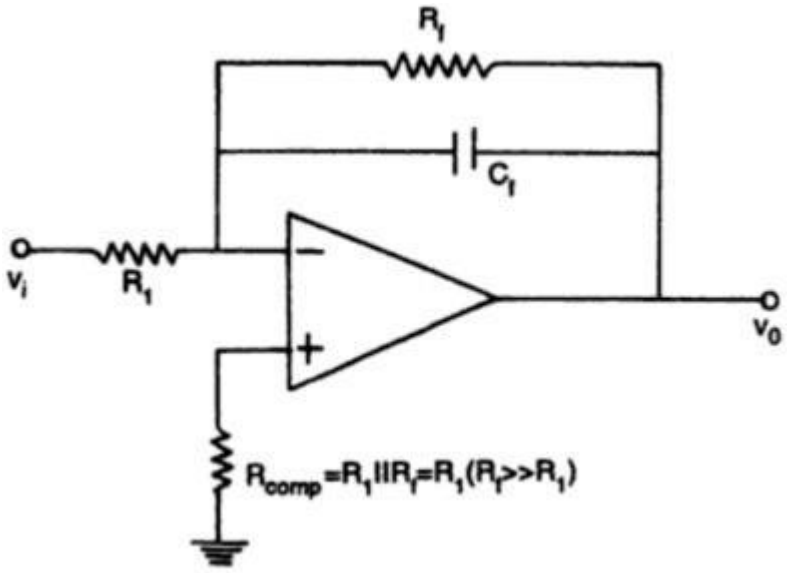


Fig. 1.3.7.2 Practical or lossy integrator The

nodal equation at the inverting input terminal of the op-amp of fig.1.3.7.1 is

$$\frac{V_i(s)}{R_1} + s C_f V_o(s) + \frac{V_o(s)}{R_f} = 0$$

from which we have,

$$V_o(s) = -\frac{1}{sR_1 C_f + R_1/R_f} V_i(s)$$

If R_f is large, the lossy integrator approximates the ideal integrator. For $s = j\omega$, magnitude of the gain of lossy integrator is given by

$$|A| = \left|\frac{V_o}{V_i}\right| = \frac{1}{\sqrt{\omega^2 R_1^2 C_f^2 + R_1^2/R_f^2}} = \frac{R_f/R_1}{\sqrt{1+(\omega R_f C_f)^2}}$$

The bode plot of the lossy integrator is also shown in fig.1.3.7.1. At low frequencies gain is constant at *Rf/R1*. The break frequency *(f=fa)* at which the gain is 0.707 (*Rf/R1)* or -3dB below its value of *Rf/R1*) is claculated from Equation below

$$\sqrt{1+(\omega R_f C_f)^2} = \sqrt{2}$$

Solving for $f = f_a$, we get

$$f_a = \frac{1}{2\pi R_f C_f}$$

This is a very important frequency. It tells us where the useful integration range starts. If the input frequency is lower than f_a the circuit acts like a simple inverting amplifier and no integration results. At input frequency equal to f_a, 50% accuracy results. The practical thumb rule is that if the input frequency is 10 times f_a, than 99% accuracy can result.

1.3.7.2 Input and output waveforms

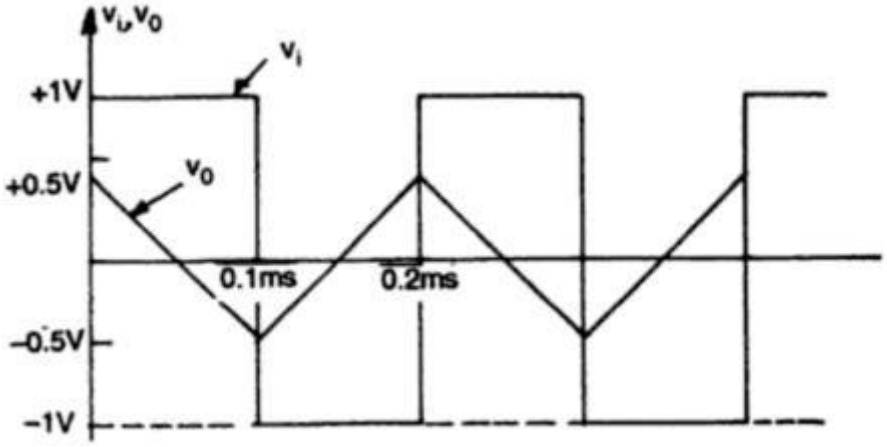


Fig. 1.3.7.3 Input and output waveforms integrator

1.3.8 LOGARITHMIC (LOG) AMPLIFIERS

Log-amp can also be used to compress the dynamic range of a signal. The fundamental log-amp circuit is shown in Fig. 1.3.8 where a grounded base transistor is placed in the feedback path.

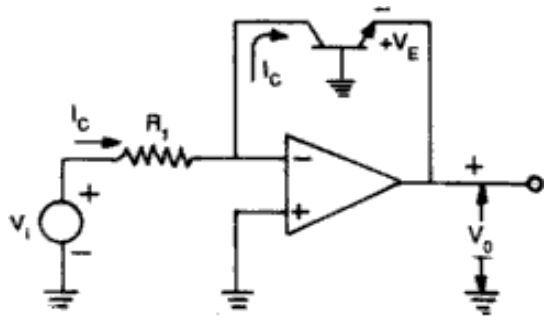


Fig. 1.3.8 Log amplifier

Since the collector is held at virtual ground and the base is also grounded, the transistor's voltage-current relationship becomes that of a diode and is given by

$$I_E = I_s \left(e^{qV_E/kT} - 1\right)$$

Since, $I_C = I_E$ for a grounded base transistor

$$I_C = I_s (e^{qV_E/kT} - 1)$$

I_S = emitter saturation current -10^{-13} A

k = Boltzmann's Constant

T = absolute temperature (in ^{0}K)

Therefore,

$$\frac{I_C}{I_s} = (e^{qV_E/kT} - 1)$$

$$e^{qV_E/kT} = \frac{I_C}{I_s} + 1$$

$$\approx \frac{I_C}{I_s} \qquad [\text{as } I_s = 10^{-13} \text{ A}, I_C >> I_s]$$

Taking natural log on both sides, we get

$$V_E = \frac{kT}{q} \ln\left(\frac{I_C}{I_s}\right)$$

Also in Fig. 1.3.8,

$$I_C = \frac{V_i}{R_1}$$

$$V_E = -V_o$$

$$V_o = -\frac{kT}{q} \ln\left(\frac{V_i}{R_1 I_s}\right) = -\frac{kT}{q} \ln\left(\frac{V_i}{V_{ref}}\right)$$

$$V_{ref} = R_1 I_s$$

The output voltage is thus proportional to the logarithm of input voltage. Although the circuit gives natural log (In), one can find log10 by proper scaling

$$\log_{10} X = 0.4343 \ln X$$

The circuit however has one problem. The emitter saturation current I_S, varies from transistor to transistor and with temperature. Thus a stable reference voltage V_{ref} cannot be obtained. This is eliminated by the circuit given in Fig. 1.3.8.1. The input is applied to one log-amp, while a reference voltage is applied to another log.amp. The two transistors are integrated close together in the same silicon wafer. This provides a close match of saturation currents and ensures good thermal tracking.

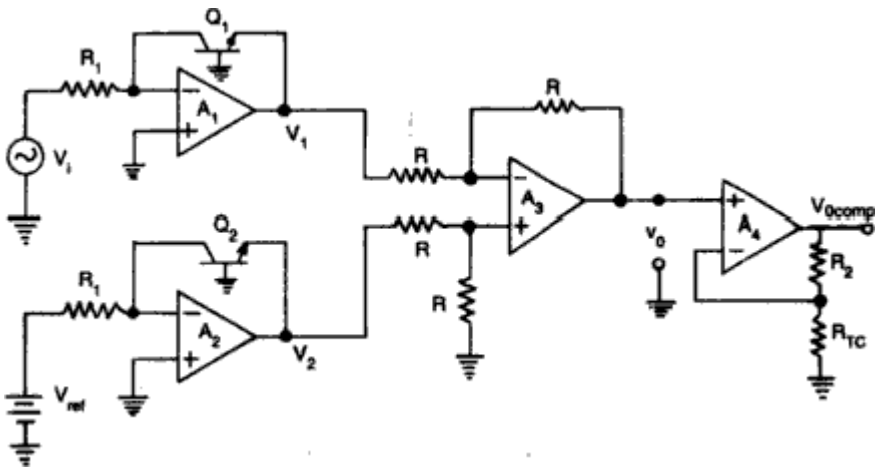


Fig.1.3.8.1. Log-amp with saturation current and temperature compensation

Assume,

$$I_{s1} = I_{s2} = I_s$$

$$V_1 = -\frac{kT}{q}\ln\left(\frac{V_i}{R_1 I_s}\right)$$

$$V_2 = -\frac{kT}{q}\ln\left(\frac{V_{ref}}{R_1 I_s}\right)$$

$$V_o = V_2 - V_1 = \frac{kT}{q}\left[\ln\left(\frac{V_i}{R_1 I_s}\right) - \ln\left(\frac{V_{ref}}{R_1 I_s}\right)\right]$$

$$V_o = \frac{kT}{q}\ln\left(\frac{V_i}{V_{ref}}\right)$$

The voltage V_0 is still dependent upon temperature and is directly proportional to T. This is compensated by the last op-amp stage A4 which provides a non-inverting gain of $(1 + R2/RTC)$. Now, the output voltage is,

$$V_{o\ comp} = \left(1 + \frac{R_2}{R_{TC}}\right)\frac{kT}{q}\ln\left(\frac{V_i}{V_{ref}}\right)$$

where RTC is a temperature-sensitive resistance with a positive coefficient of temperature, so that the slope of the equation becomes constant as the temperature changes.

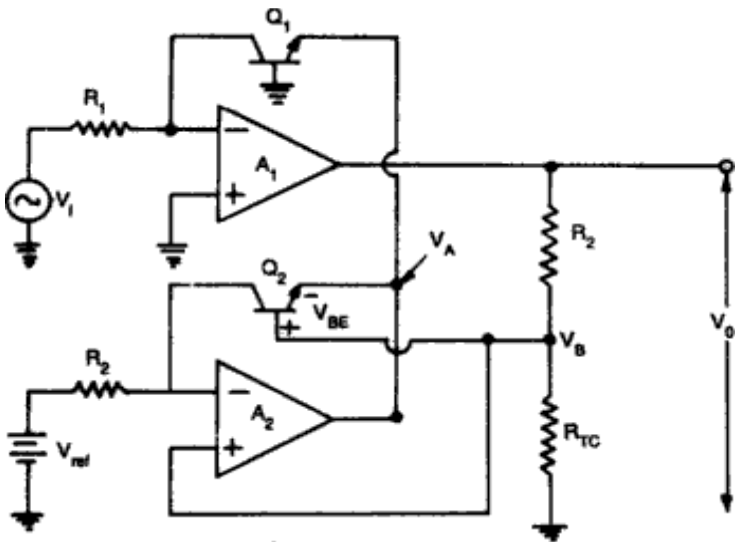


Fig. 1.3.8.2 Log-amp using two op-amps only

The circuit in Fig. 1.3.8.1 requires four op-amps, and becomes expensive if FET op-amps are used for precision. The same output can be obtained by the circuit of Fig. 1.3.8.2 using two op-amps only.

1.3.9 ANTILOG AMPLIFIER

The circuit is shown in Fig. 1.3.9. The input V_i for the antilog-amp is fed into the temperature compensating voltage divider R2 and RTC and then to the base of Q2. The output V_o of the antilog-amp is fed back to the inverting input of A1 through the resistor R1. The base to emitter voltage of transistors Q1 and Q2 can be written as

$$V_{Q1\ B\text{-}E} = \frac{kT}{q} \ln\left(\frac{V_o}{R_1 I_s}\right)$$

$$V_{Q2\ B\text{-}E} = \frac{kT}{q} \ln\left(\frac{V_{ref}}{R_1 I_s}\right)$$

Since the base of Q1 is tied to ground, we get

$$V_A = -V_{Q1\ B\text{-}E} = -\frac{kT}{q} \ln\left(\frac{V_o}{R_1 I_s}\right)$$

The base voltage V_B of Q2 is

$$V_B = \left(\frac{R_{TC}}{R_2 + R_{TC}}\right) V_i$$

The voltage at the emitter of *Q2* is

$$V_{Q2\,E} = V_B + V_{Q2\,E\text{-}B}$$

$$V_{Q2\,E} = \left(\frac{R_{TC}}{R_2 + R_{TC}}\right) V_i - \frac{kT}{q} \ln\left(\frac{V_{ref}}{R_1 I_s}\right)$$

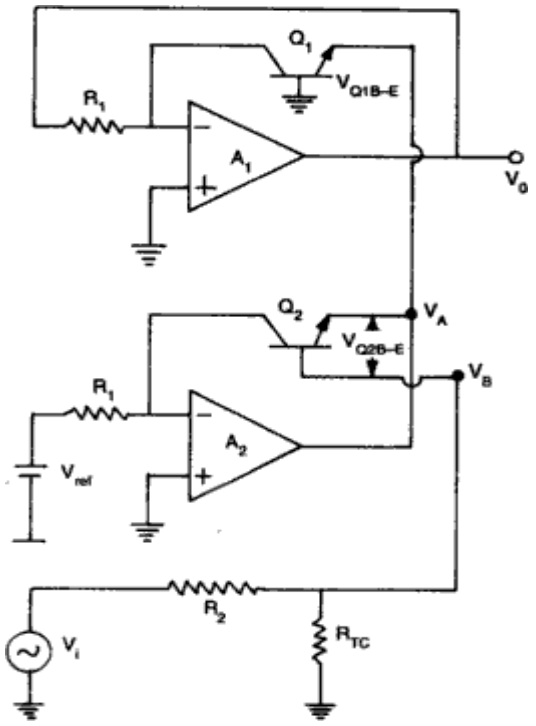


Fig. 1.3.9 Antilog amplifier

But the emitter voltage of Q2 is VA, that is

$$V_A = V_{Q2\,E}$$

$$-\frac{kT}{q} \ln \frac{V_o}{R_1 I_s} = \frac{R_{TC}}{R_2 + R_{TC}} V_i - \frac{kT}{q} \ln \frac{V_{ref}}{R_1 I_s}$$

$$\frac{R_{TC}}{R_2 + R_{TC}} V_i = -\frac{kT}{q}\left(\ln \frac{V_o}{R_1 I_s} - \ln \frac{V_{ref}}{R_1 I_s}\right)$$

$$-\frac{q}{kT} \frac{R_{TC}}{R_2 + R_{TC}} V_i = \ln\left(\frac{V_o}{V_{ref}}\right)$$

Changing natural log, i.e., in to log10 , we get

$$-0.4343\left(\frac{q}{kT}\right)\left(\frac{R_{TC}}{R_2 + R_{TC}}\right) V_i = 0.4343 \times \ln\left(\frac{V_o}{V_{ref}}\right)$$

$$-K' V_i = \log_{10}\left(\frac{V_o}{V_{ref}}\right)$$

$$\frac{V_o}{V_{ref}} = 10^{-K' V_i}$$

$$V_o = V_{ref}\,(10^{-K' V_i})$$

Where $K' = 0.4343 \frac{q}{kT} \frac{RTC}{R2 + RTC}$

Hence an increase of input by one volt causes the output to decrease by a decade. The IC755 log/antilog amplifier IC chip is available as a functional module which may require some external components also to be connected to it.

1.4 OP-AMP USED AS COMPARATORS

1.4.1 COMPARATOR

A comparator is a circuit which compares a signal voltage applied at one input of an op-amp with a known reference voltage at the other input. It is basically an open-loop op-amp with output $\pm V_{sat}$ ($=V_{cc}$) as shown in the ideal transfer characteristics of Fig. 1.4.1(a). However, a commercial op-amp has the transfer characteristics of Fig. 1.4.1(b).

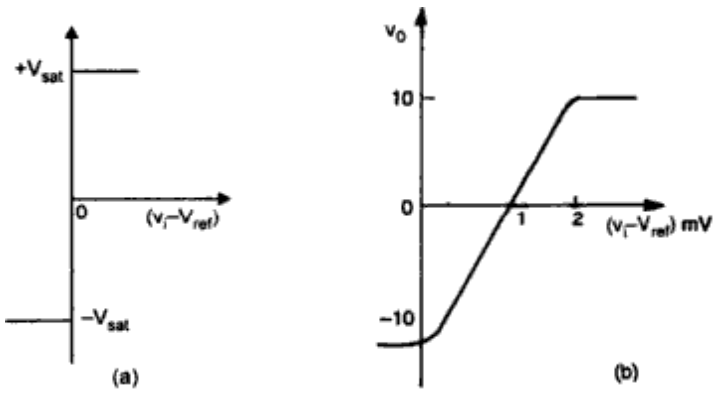


Fig. 1.4.1 The transfer characteristics (a) ideal comparator. (b) Practical comparator There are basically two types of comparators:

Non-inverting comparator

Inverting comparator

The circuit of Fig. 1.4.1.1(a) is called a non-inverting comparator. A fixed reference voltage V_{ref} applied to (-) input and a time varying signal V_i is applied to (+) input. The output voltage is at $-V_{sat}$ for $V_i < V_{ref}$ and V_o goes to $+V_{sat}$ for $V_i > V_{ref}$. The output waveform for a Sinusoidal input signal applied to the (+) input is shown in Fig. 1.4.1.1 (b and c) for positive and negative V_{ref} respectively.

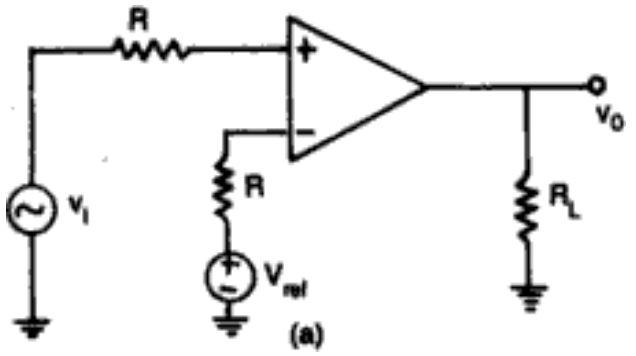


Fig. 1.4.1.1(a) Comparator

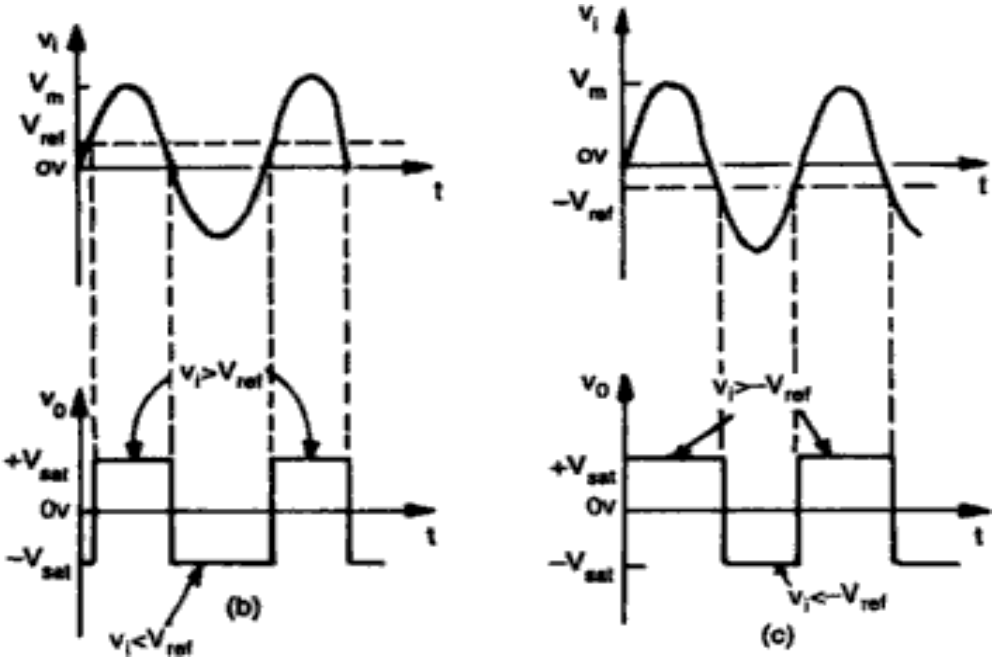


Fig. 1.4.1.1. Input and output of a Comparator when (a)V_{ref}>0 V (b) V_{ref}< 0V

In a practical circuit V_{ref} is obtained by using a 10KΩ potentiometer which forms a voltage divider with the supply voltages V+ and V- with the wiper connected to (-) input terminal as shown in Fig. 1.7.4.1 (d).Thus a V_{ref} of desired amplitude and polarity can be obtained by simply adjusting the 10KΩ potentiometer.

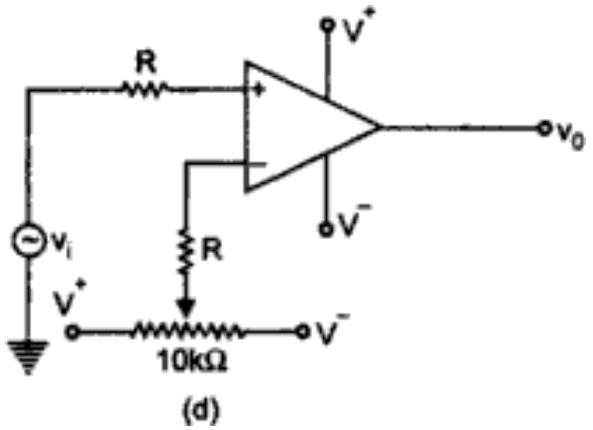


Fig. 1.7.1.1 (d) Non-inverting comparator. Input and output waveforms for (b) V_{ref}

Positive (c) V_{ref} negative (d) Practical non-inverting comparator

Figure 1.7.1.2(a) shows a practical inverting comparator in which the reference voltage V_{ref} is applied to the (+) input and v_i is applied to (-) input. For a sinusoidal input signal, the output waveform is shown in Fig. 1.7.1.2(b) and (c) for V_{ref} positive and negative respectively.

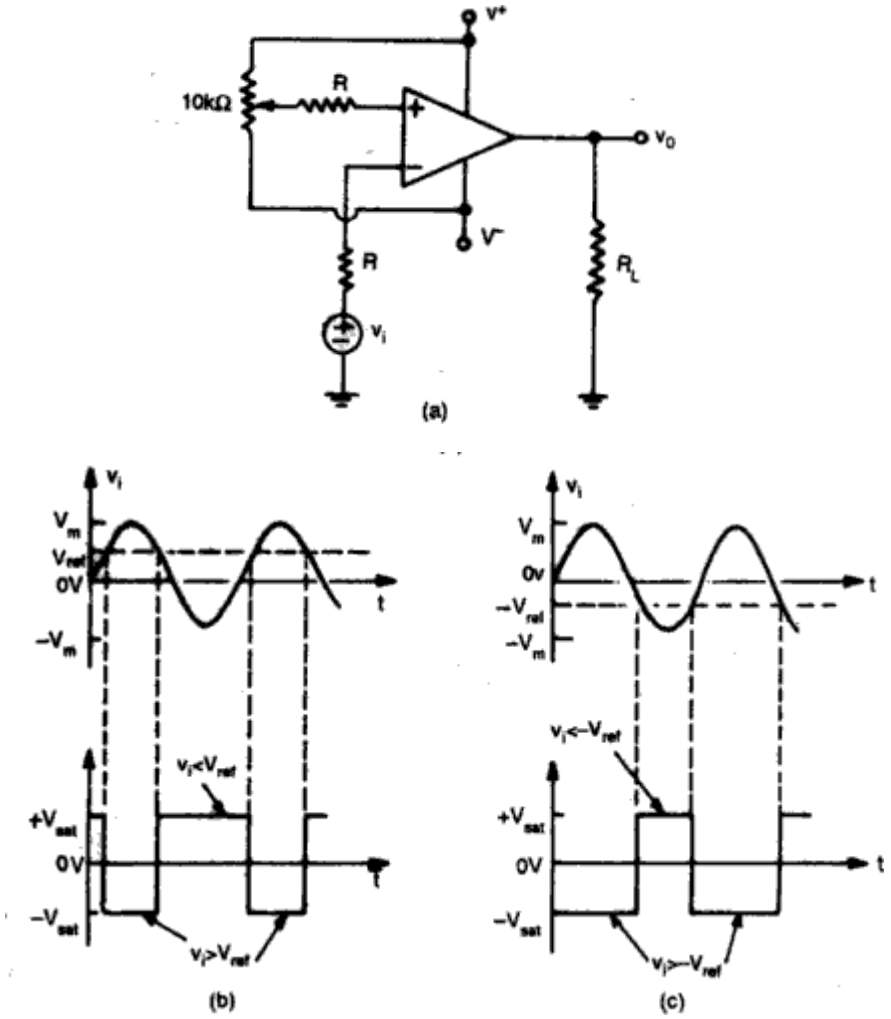


Fig. 1.7.1.2.(a) Inverting comparator. Input and output waveforms for (b) V_{ref}

Positive (c) V_{ref} negative

1.7.2 REGENERATIVE COMPARATOR (SCHMITT TRIGGER)

We have seen that in a basic comparator, a feedback is not used the op-amp is used in the open loop mode. As open loop gain of op-amp is very large, very small noise voltages also can cause triggering of the comparator, to change its state. Such a false triggering may cause lot of problems in the applications of comparator as zero- crossing detector. This may give a wrong indication of zero-crossing due to zero-crossing of noise voltage rather than zero crossing of

input wanted signals. Such unwanted noise causes the output to jump between high and low states. The comparator circuit used to avoid such unwanted triggering is called *regenerative comparator or Schmitt trigger*, which basically uses a positive feedback.

The figure 1.4.2 shows the basic Schmitt trigger circuit. As the input is applied to the inverting terminal, it is also called inverting Schmitt trigger circuit. The inverting mode produces opposite polarity output. This is fed-back to the non-inverting input which is of same polarity as that of the output. This ensures a positive feedback.

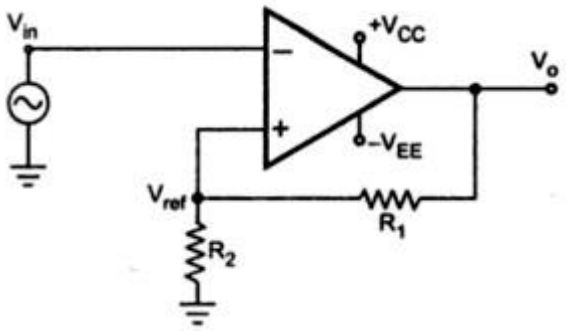


Figure 1.4.2 Schmitt trigger using op amp.(Inverting)

The fig.1.4.2 shows the basic inverting Schmitt trigger circuit.

- As the input is applied to the inverting terminal, it is also called inverting Schmitt trigger circuit.
- The inverting mode produces opposite polarity output (180□ phase shift)
- This is fed-back to the non-inverting input which is of same polarity as that of output.
- This ensures positive feedback.

  Case 1: When V_{in} is slightly positive than V_{ref}, the output is driven into negative saturation at $-V_{sat}$ level.

  Case 2: When V_{in} is slightly negative than V_{ref}, the output is driven into positive saturation at $+V_{sat}$ level.

  Thus the output voltage is always at $+V_{sat}$ or $-V_{sat}$ but the voltage at which it changes its state now can be controlled by the resistance R_1 and R_2. Thus V_{ref} can be obtained as per requirement.

  Now R_1 and R_2 forms a potential divider and we can write,

  Positive saturation

$$+\square_{\square\square\square} = \square \frac{\square_{\square}}{\square_{\square} + \square_{\square}} \times \square_{\square} = \square \frac{+\square_{\square\square\square}}{\square_{\square} + \square_{\square}} \times \square_{\square}$$

  Negative saturation

$$-\square_{\square\square\square} = \square \frac{\square_{\square}}{\square_{\square} + \square_{\square}} \times \square_{\square} = \square \frac{-\square_{\square\square\square}}{\square_{\square} + \square_{\square}} \times \square_{\square}$$

  $+V_{ref}$ is for positive saturation when $V_0 = +V_{sat}$ and is called as upper threshold voltage denoted as VUT

$-V_{ref}$ is for positive saturation when $V_0 = -V_{sat}$ and is called as lower threshold voltage denoted as V_{LT}

The values of these voltages can be determined and adjusted by selecting proper values of R_1 and R_2. Thus

$$-V_{UT} = \frac{+V_{sat} R_2}{R_1 + R_2}$$

and

$$-V_{LT} = \frac{-V_{sat} R_2}{R_1 + R_2}$$

The output voltage remaains in a given state until the input voltage exceed the threshold volage level either postive or negative.

The fig.1.4.2.1 shows the graph of output voltage against input voltage. This is called transfer characteristics of Schmitt trigger.

The graph indicated that once the output changes its state it remains there indefinitely until the input voltage crosses any of the threshold voltage levels. This is called hysteresis of Schmitt trigger. The hysteresis is also called as dead- zone or dead-band.

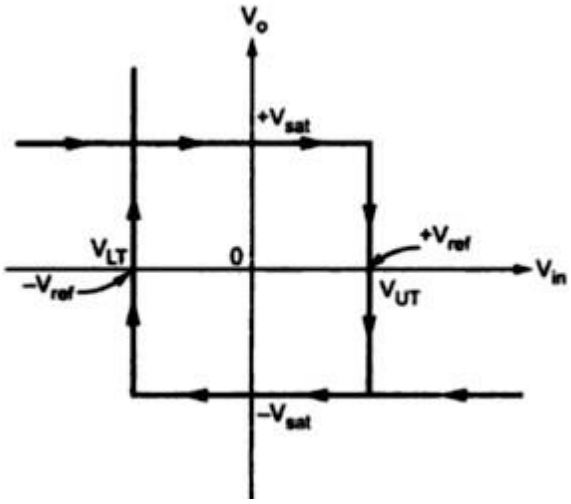


Fig. 1.4.2.1 Hysteresis of Schmitt trigger.

The difference between V_{UT} and V_{LT} is called width of the hysteresis denoted as H.

$$H = V_{UT} - V_{LT}$$

$$H = \frac{+V_{sat} R_2}{R_1 + R_2} - \frac{-V_{sat} R_2}{R_1 + R_2}$$

$$H = \frac{2V_{sat} R_2}{R_1 + R_2}$$

The schmitt trigger eliminates the effect of noise voltages less than the hysterisis H, cannot cause triggering. As for postive V_{in} greater than V_{UT}, the output becomes $-V_{sat}$ and for negative V_{in} less than V_{LT}, the output becomes $+V_{sat}$, this is called *inverting schmitt trigger*.

In short,

$$V_{in} < V_{LT},\ V_0 = +V_{sat}$$

$$V_{in} > V_{UT},\ V_0 = -V_{sat}$$

$$V_{LT} < V_{in} < V_{UT},\ V_o = Previousstateachieved$$

If input applied is purely sinusoidal, the input and output waveforms for inverting Schmitt trigger can be shown as in fig.1.4.2.2.

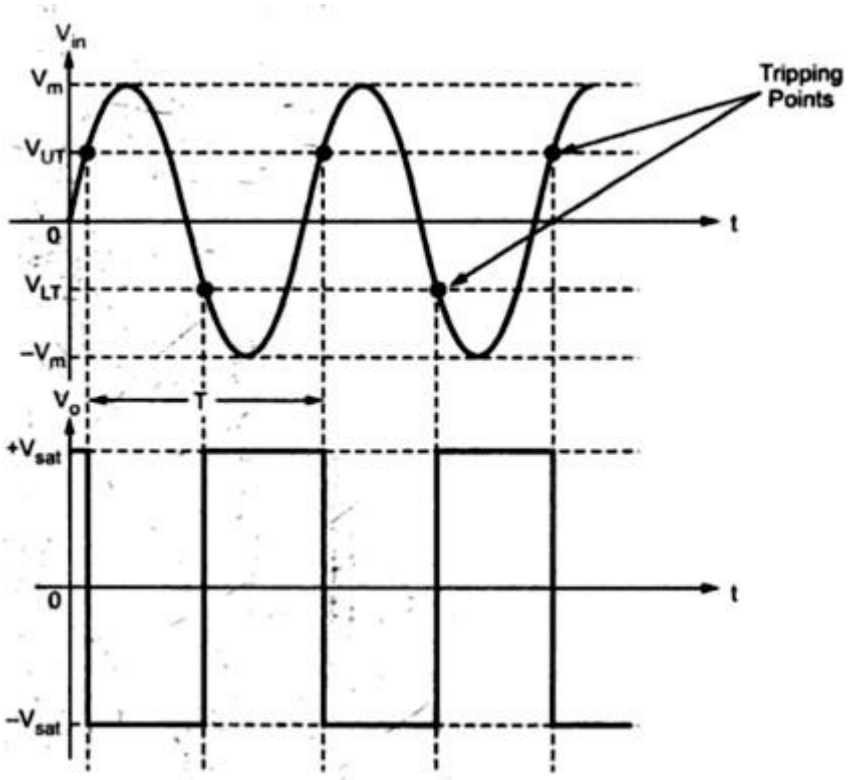


Fig. 1.4.2.2 Input and output waveforms of Schmitt trigger

Text Book References:

1. **Ramakant A.Gayakwad, "0P-AMP and Linear ICs", 4th Edition, Prentice Hall / Pearson Education, 1994.**
2. **D.Roy Choudary, Shail Jain, "Linear Integrated Circuits", New Age International Pvt. Ltd., 2000.**
3. **Grey and Meyer, "Analysis and Design of Analog Integrated Circuits, 4th Edition, Wiley International, 2001.**
4. **Michael Jacob, "Applications and Design with Analog Integrated Circuits, 2nd Edition, Prentice Hall of India, 1993.**
5. **S. Salivahanan, V.S. Kanchana Bhaaskaran, "Linear integrated circuits", 3rd Edition, McGraw-Hill, 2011.**
6. **William D.StaneIy, "Operational Amplifiers with Linear Integrated Circuits", 4th Edition, Pearson Education, 2004.**

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DEPARTMENT OF ELECTRONICS AND COMMMUNICATION ENGINEERING

ANALOG INTEGRATED CIRCUITS - SEC1302
UNIT-II
FILTERS AND OSCILLATORS

2.1 ACTIVE FILTERS

FILTERS are circuits used for select signal components of required frequencies and reject other unwanted frequency components. Thus selectivity is one of the main criteria for a filter circuit in communication engineering.

These filters are actually allowing the required frequency bands and attenuate the unwanted frequency bands but they are not adaptive and precise. The allowing band is termed as pass band and attenuating band is termed as stop band. The output gain of the filters in pass band is high and that in stop band is very low (negligible). For ideal filters, pass band gain is infinite and stop band gain is zero. The frequency that acts as a barrier between stop and pass band is termed as cut-off frequency. The design of a filter is based particularly on this cut-off frequency. It is found that the practical value of the cut-off frequency is 3dB less than the maximum frequency allowed.

These filters are considered to be passive when passive components like resistors, capacitors and inductors are used in constructing the circuits. Passive filters are the basic filters used in communication engineering but they are not adaptive and precise. For a good filter, the slope of frequency response plot from pass band to stop band or vice versa should be high. But passive filters sometimes have very low slope for changing input signals and other factors. Even in pass band the gain is not constant but varies. These problems are minimized by using active filters which are adaptive (manage the gain to be constant throughout the pass band and slope to be very high for even a major change in input signals).

Active filters use OP AMP to be adaptive in nature with lager controllable gain value.

Advantages of active filters over passive filters:

1. **Reduced size and weight**
2. **Increased reliability and improved performance**
3. **Simple design and good voltage gain**
4. **When fabricated in larger quantities, cheaper than passive filters**

Disadvantages of Active Filters:

1. **Limited bandwidth only.**
2. **Quality factor is also limited**
3. **Require power supply (passive doesn't require power supply)**

4. Changes due to environmental factors.

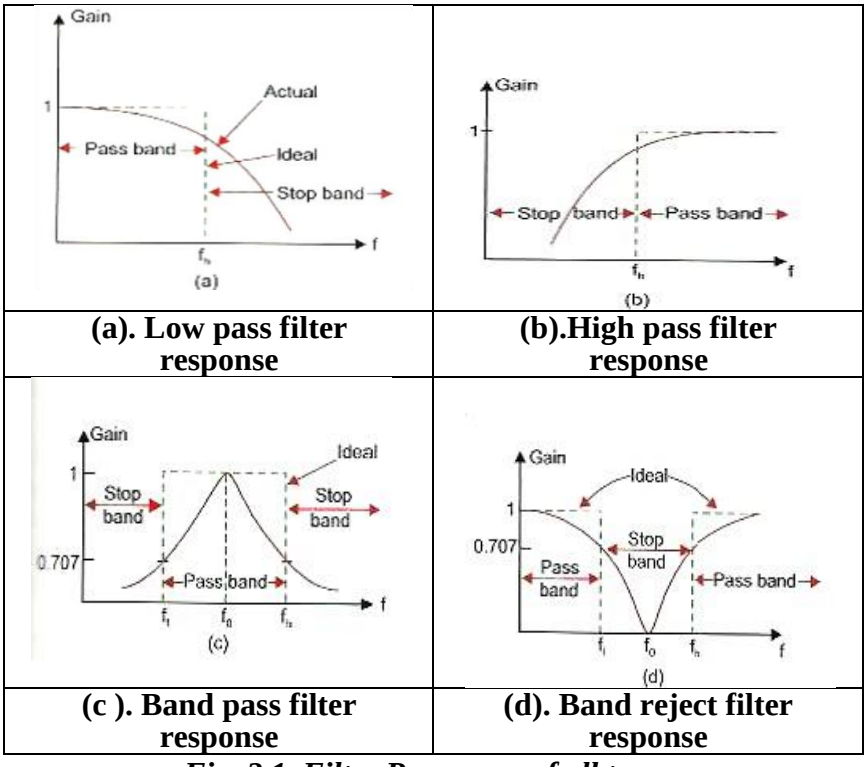
Possible question: ***What is an active filter? What are its advantages over passive filters?***

2.1.1 Order of Butterworth filters

Butterworth filters were designed by a British engineer Stephen Butterworth as a maximally flat-response filter. This filter minimizes ripples and manages to maintain a flat response in pass band.

Order of a filter is the magnitude of voltage transfer function of a filter that decreases by -(20*n)dB/decade as the order „n' increases in stop band and flat in pass band. This is shown in the fig. 2.1.

Types of filters according to the response:



(a). Low pass filter response	(b).High pass filter response
(c). Band pass filter response	(d). Band reject filter response

Fig. 2.1. Filter Responses of all types.

For example, if the order is 50, then the filter response in stop band decreases by -100 dB/decade. So if order increases

1. The magnitude of voltage transfer function in stop band is very high and slope decreases by 20 db/decade.

2. but the circuit complexity increases.

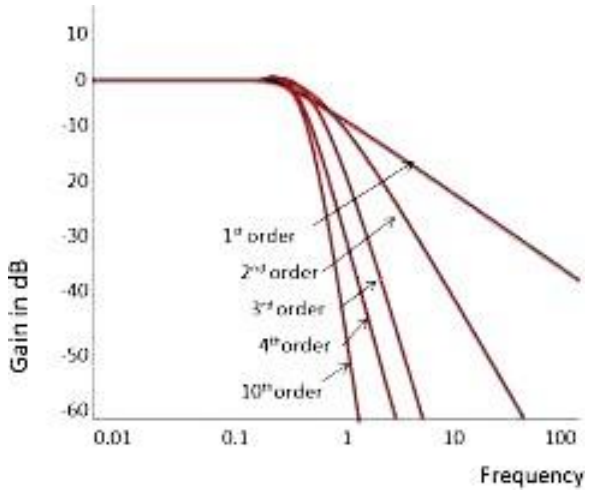


Fig.2.1.1. A Sample Butterworth Filter Response - Order wise

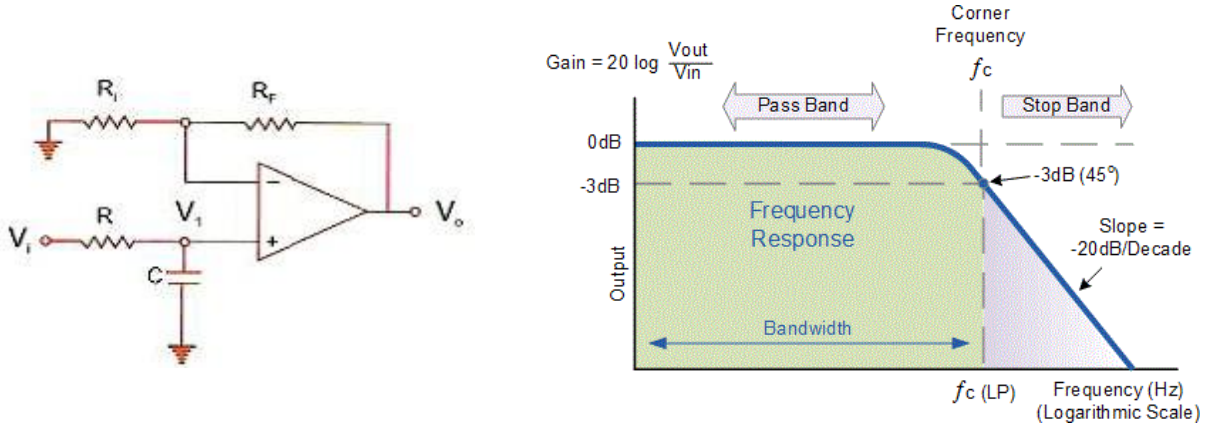
Note: Butterworth filters have flat response in pass bands and decrease in response of -20dB /per decade in pass bands.

Possible question: ***Write short notes on the order of Butterworth filters.***

2.1.1.1. Low Pass Filters

A low pass filter allows low frequencies upto a corner frequency (cut-off frequency) and attenuates (stops) high frequencies above cut-off frequency. This is shown in the frequency response fig. 2.1.1.1.b.

The circuit is a simple non-inverting amplifier, where a RC low pass filter circuit is connected to the input. Capacitor allows high frequencies through it and blocks low frequencies. This characteristic of capacitor is used in these filters.



(a). Filter Circuit ***(b). Filter Response***

Fig. 2.1.1.1. Active Low pass filter- First Order

Therefore, $$H(s) = \frac{V_o(s)}{V_i(s)} = \frac{A_o}{\frac{s}{\omega_h} + 1} = \frac{A_o \omega_h}{s + \omega_h}$$

This is the standard form of the transfer function of a first order low pass systen To determine the frequency response, put $s = j\omega$ in Eq. (7.8). Therefore, we get

$$H(j\omega) = \frac{A_o}{1 + j\omega RC} = \frac{A_o}{1 + j(f/f_h)}$$

where $$f_h = \frac{1}{2\pi RC} \text{ and } f = \frac{\omega}{2\pi}$$

At very low frequency, i.e. $f << f_h$

$$|H(j\omega)| \simeq A_o$$

At $f = f_h$,

$$|H(j\omega)| = \frac{A_o}{\sqrt{2}} = 0.707\, A_o$$

At very high frequency i.e. $f >> f_h$

$$|H(j\omega)| << A_o \simeq 0$$

The voltage V_1 across the capacitor C in the s-domain is

$$V_1(s) = \frac{\frac{1}{sC}}{R + \frac{1}{sC}} V_i(s)$$

So, $$\frac{V_1(s)}{V_i(s)} = \frac{1}{RCs + 1}$$

where $V(s)$ is the Laplace transform of v in time domain.

The closed loop gain A_o of the op-amp is,

$$A_o = \frac{V_o(s)}{V_1(s)} = \left(1 + \frac{R_F}{R_i}\right)$$

So, the overall transfer function from Eqs. (7.4) and (7.5) is

$$H(s) = \frac{V_o(s)}{V_i(s)} = \frac{V_o(s)}{V_1(s)} \cdot \frac{V_1(s)}{V_i(s)} = \frac{A_o}{RCs + 1}$$

Let $$\omega_h = \frac{1}{RC}$$

Therefore, $$H(s) = \frac{V_0(s)}{V_i(s)} = \frac{A_0}{\frac{s}{\omega_h}+1} = \frac{A_0\omega_h}{s+\omega_h}$$

This is the standard form of the transfer function of a first order low pass system To determine the frequency response, put $s = j\omega$ in Eq. (7.8). Therefore, we get

$$H(j\omega) = \frac{A_0}{1+j\omega RC} = \frac{A_0}{1+j(f/f_h)}$$

where $$f_h = \frac{1}{2\pi RC} \text{ and } f = \frac{\omega}{2\pi}$$

At very low frequency, i.e. $f << f_h$

$$|H(j\omega)| \simeq A_0$$

At $$f = f_h,$$

$$|H(j\omega)| = \frac{A_0}{\sqrt{2}} = 0.707\,A_0$$

At very high frequency i.e. $f >> f_h$

$$|H(j\omega)| << A_0 \simeq 0$$

Here resistor R, smoothens the input signal and the capacitor C allows higher frequencies to reach the ground. Thus high frequency signals never reach the input terminal and only low frequency signal reaches the input terminal.

How corner frequency is obtained?

In the response fig. 2.1.1.1.b., a frequency is noted where the response curve point meets a -3dB line drawn below the maximum gain. The frequency is considered as *corner frequency (f_C)* above which the filter attenuates the input signal and below which it allows the signal.

As shown in the fig. 2.1.1.1.b response -20 dB/decade slope is obtained.

Second order Low pass filter and its response

c). Filter Circuit ***(d). Frequency response***

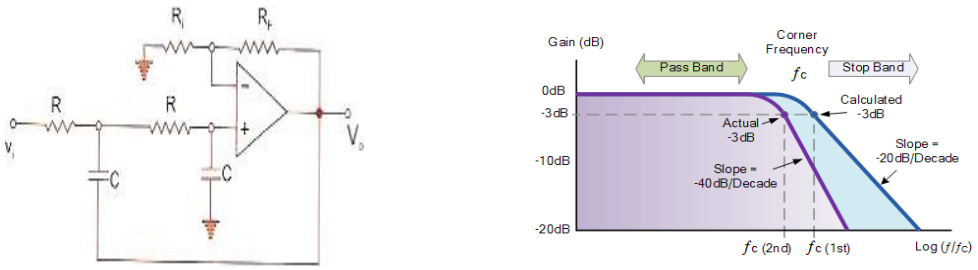


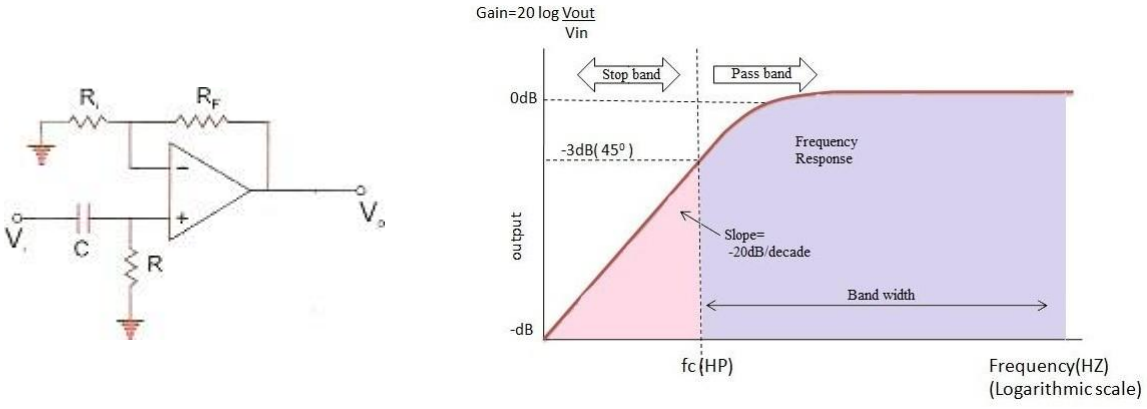
Fig. 2.1.1.1.c & d: Second Order Active Low Pass Filter

With first order circuit, another RC circuit is added as shown in the fig. 2.1.1.1.c and the response is shown in fig. 2.1.1.1.d for second order LPF with a slope of -40 dB/ decade. This is due to the fact that each RC network introduces -20dB decrease in stop band response slope.

2.1.1.2. High Pass Filters

A high pass filter attenuates low frequencies below corner frequency (cut-off frequency) and allows high frequencies above cut-off frequency. This is shown in the frequency response fig. 2.1.1.2.b.

The circuit is a simple non-inverting amplifier, where a RC low pass filter circuit is connected to the input.



(a). Filter Circuit ***(b). Frequency response***

Fig. 2.1.1.2. First Order Active High Pass Filter

As shown in the above fig. 2.1.1.2.(a)., Capacitor C blocks low frequency signals below the corner frequency f_c as shown in fig. 2.1.1.2.(b). The response curve increases 20 dB per decade at low frequencies below corner frequencies.

2.1.1.3. Band Pass Filters

A Band pass filter allows a band of frequencies and blocks lower and higher frequencies other than the allowed band as shown in fig. 2.1.1.3.b. As shown in the fig. 2.1.1.3.a, high pass and low pass filters are connected in series.

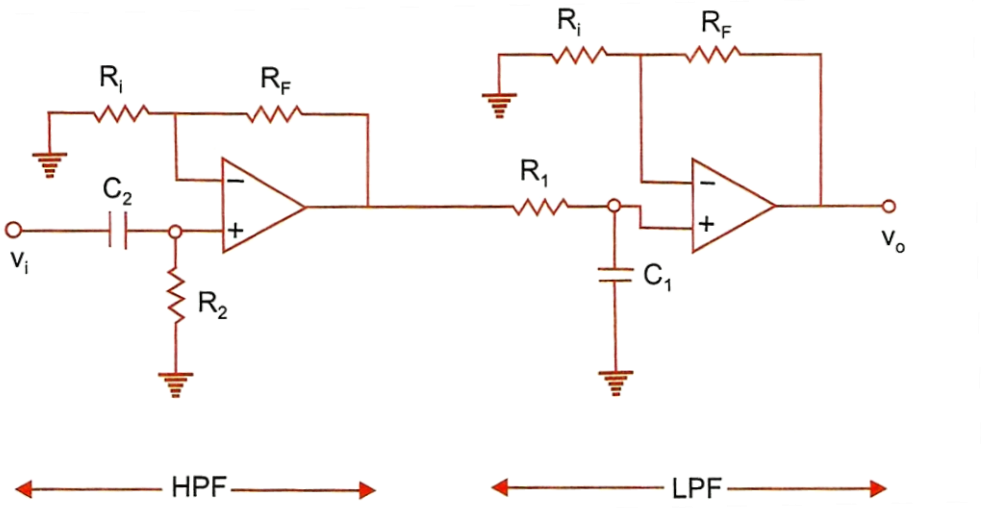


Fig. 2.1.1.3. a. Active Band Pass Filter

The corner frequency of low pass filter f_L is chosen to be lower than that of high pass filter f_H. Thus the difference between f_H and f_L is considered to be the pass band. In low frequency stop band, the response increases 20 dB per decade and in high frequency stop band, the response decreases by 20 dB per decade.

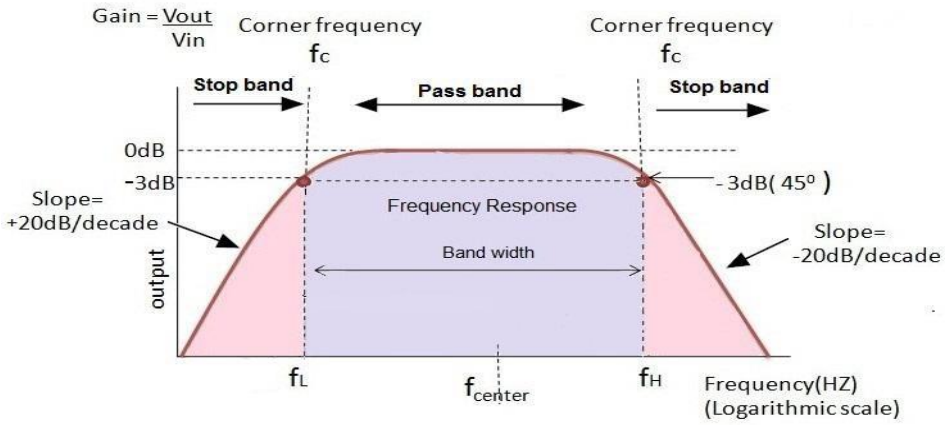


Fig. 2.1.1.3.b. Response of Active Band Pass Filter

2.1.1.4. Band Reject Filters (Notch filter)

A Band pass filter blocks a band of frequencies and allows lower and higher frequencies other than the blocked band as shown in fig. 2.1.1.4.b. As shown in the fig. 2.1.1.4.a, band pass filter is connected to a summer circuit. The input and output of the band pass filter is summed up at the inverting summer input. The bands are inverted by the inverting summer and so pass band of band pass filter becomes stop band and stop bands becomes pass bands. Thus this filter only allows particular band above lower corner frequency f_L and below upper corner frequency f_H.

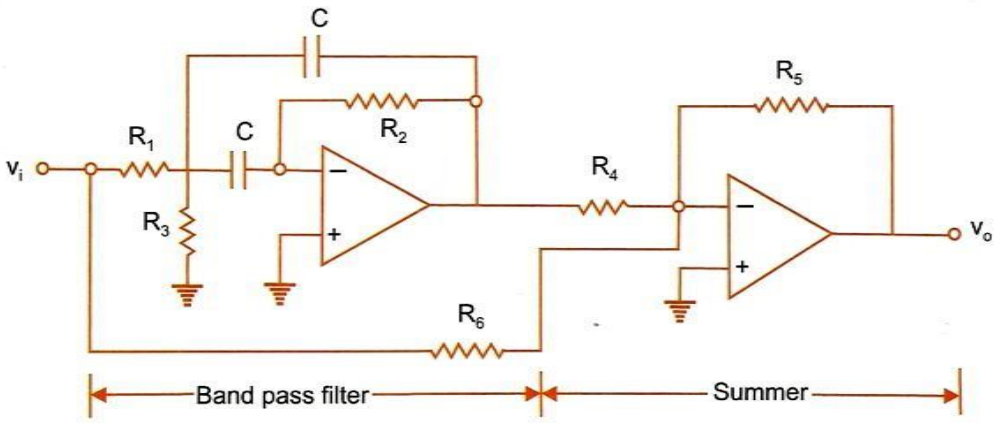


Fig. 2.1.1.4.a. Active Band Reject Filter

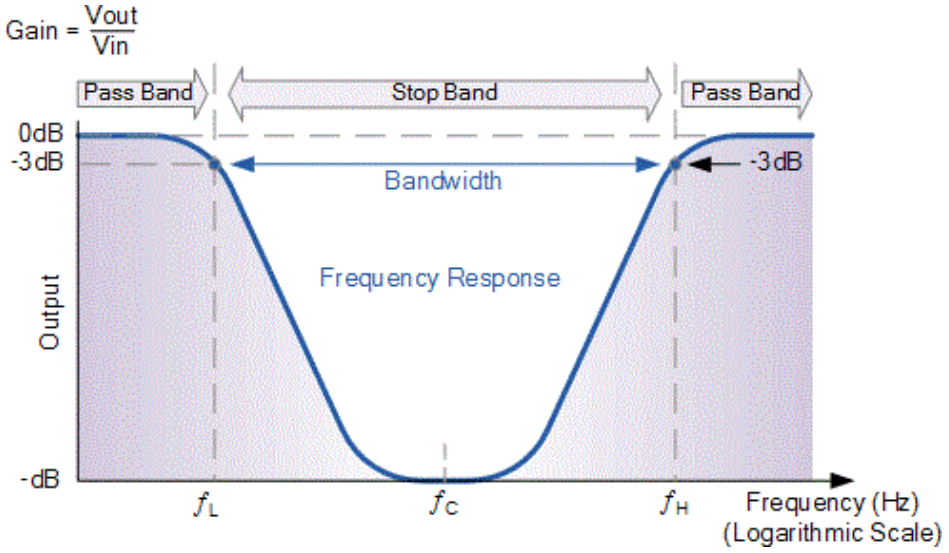


Fig. 2.1.1.4.b. Response of Active Band Reject Filter

Possible questions:

Write briefly about first and second order Butterworth Low-pass filter with neat sketches.

Write briefly about first and second order Butterworth high-pass filter with neat sketches.

Write briefly about first order Butterworth band-pass filter with neat sketches.

Write briefly about first order Butterworth band-reject filter with neat sketches. .

Write briefly about Notch filter with neat sketches.

2.2 OP-AMP OSCILLATORS

In electronics, oscillators are circuits that generate sinusoidal or non-sinusoidal waveforms used as reference signals in communication engineering. The non-sinusoidal waveforms are triangular, ramp, saw-tooth, pulse, TTL, rectangular, spike etc.

The oscillator shall have an amplifier with a positive feedback for generating oscillations. The basic oscillator circuit with feedback is shown below fig. 2.2.a.

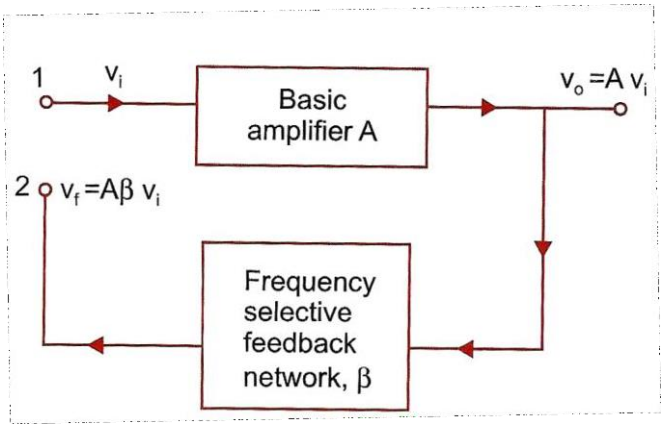


Fig.2.2.a. Basic Feedback Oscillator

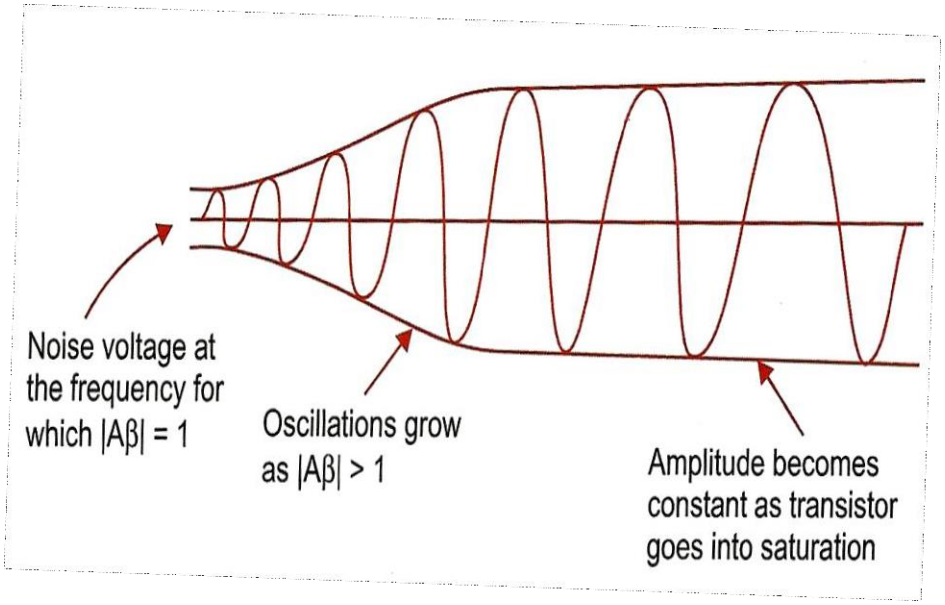


Fig.2.2.b. Feedback Oscillator Output

But for sustained (continuous and steady) oscillations Barkhausen's criteria are to be satisfied. The criteria states that

1. The total gain of the circuit should be equal to or more than one and

2. The overall phase shift in the circuit (amplifier and feedback circuit) shall be zero. If gain of the amplifier is considered as A and feedback factor is β, then

Criterion 1: **□A β □ □ 1**

Modulus of the product of the amplifier gain A and feedback factor of feedback network β should be equal to or greater than zero.

Criterion 2: **□A β = 0° or 360° (0 or 2□ radians)**

Phase angle between the amplifier gain A and feedback factor of feedback network β or total phase shift in the circuit should be equal to or greater than zero. Criterion 1 and 2 are *Barkhausen's criteria for sustained oscillations.*

As shown in fig. 2.2.b, a noise voltage introduced by existing imbalances in the circuit is amplified by the circuit itself. The frequency of noise voltage depends on the design aspects of the circuit and when multiplication factor of total gain □A β □=1 and when □A β □ □ 1, the amplitude of the generated voltage increases till saturation is reached. Then the oscillation at the particular frequency is generated and sustained. This is done when the phase shift of the circuit is 0° or 360° (0 or 2□ radians).

In the following sections two such sinusoidal oscillators are being explained. They are (1). RC phase shift oscillator and

(2). Wien Bridge oscillator

2.2.1. RC Phase Shift Oscillators

RC phase shift oscillator generates sinusoidal output and thus categorized under sinusoidal oscillators. Here in this oscillator the amplifier used is a negative feedback inverting Operational amplifier connected to a RC feedback network.

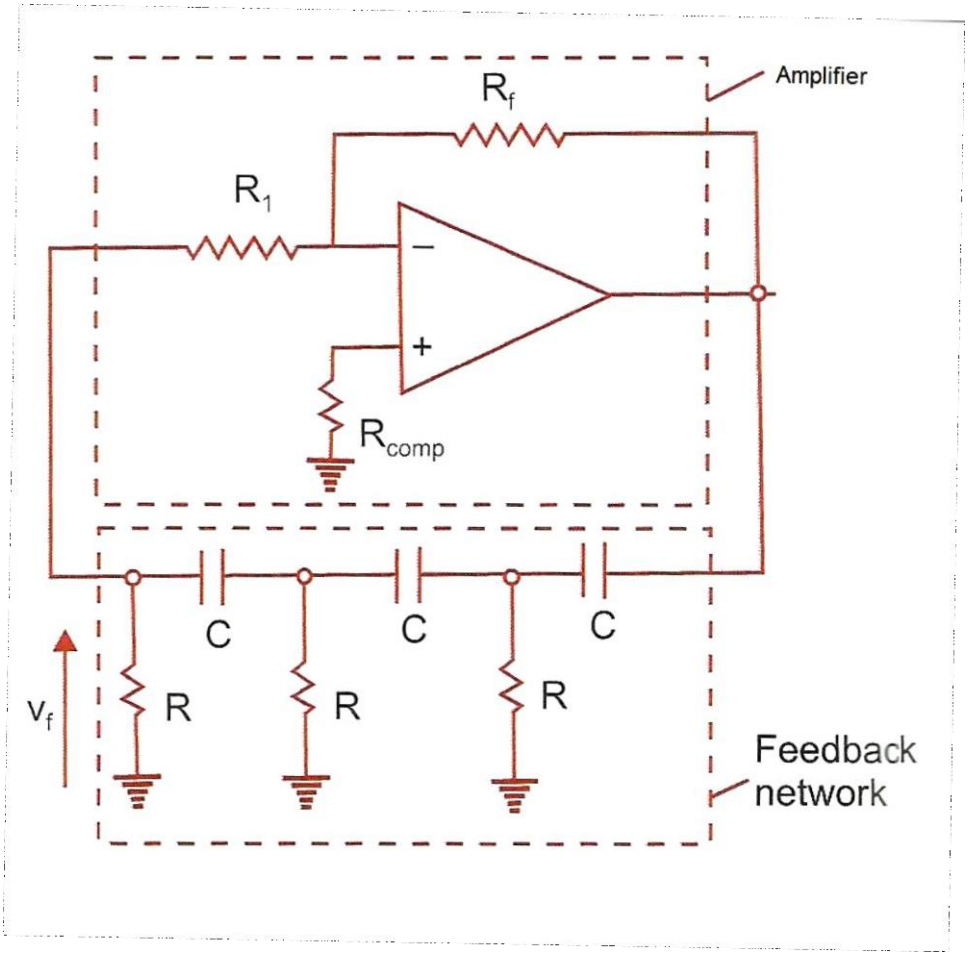


Fig.2.2.1.a. RC Phase Shift Oscillator

Construction: As described earlier the oscillator comprising of a negative feedback inverting operational amplifier whose input resistor is R1 and feedback resistor is R2 as shown in the fig. 2.2.1.a.

An RC network where one end of the resistor R is connected to the ground, the other end is connected to a capacitor C and the other end of the capacitor acts as an input terminal. The combined end of the capacitor and resistor acts as output terminal. Each RC network provides 60° (□/3 radians) phase shift between their input and output terminals. Thus three networks are connected in series, so as to provide a phase shift of 180° or □ radians. The feedback RC network shifts the phase this is termed as RC phase shift oscillator. As said earlier the amplifier is an inverting amplifier, and so 180° or □ radians phase shift between input and output. Hence second Barkhausen's criterion is fulfilled.

Choosing the value of amplifier voltage gain to be more (nearly 30 or so), we can fulfill first Barkhausen's criterion of having overall gain more than 1.

Working: Practically an OP AMP is not perfect and so imbalances are prevailing between their input terminals. This imbalance generates a minor sinusoidal noise voltages fed between the input terminals. This noise voltage is amplified by the amplifier and a sinusoidal output voltage V_o is generated at the output terminal.

As discussed earlier, the RC network provides 180° or 2□ radians where V_o is fed into the feedback RC network and an inverse voltage of V_f shown in fig. 2.2.1.b. We can understand that V_f is 180° (or 2□ radians) phase shifted V_o. This V_f is fed into the inverting terminal of the operational amplifier through an input resistor R1. This voltage is phase inverted of 180° (or 2□ radians) by the amplifier and the output V_o is inverse of V_f.

Since the circuit fulfills the criteria for sustained oscillations, the circuit continuously generates sinusoidal output.

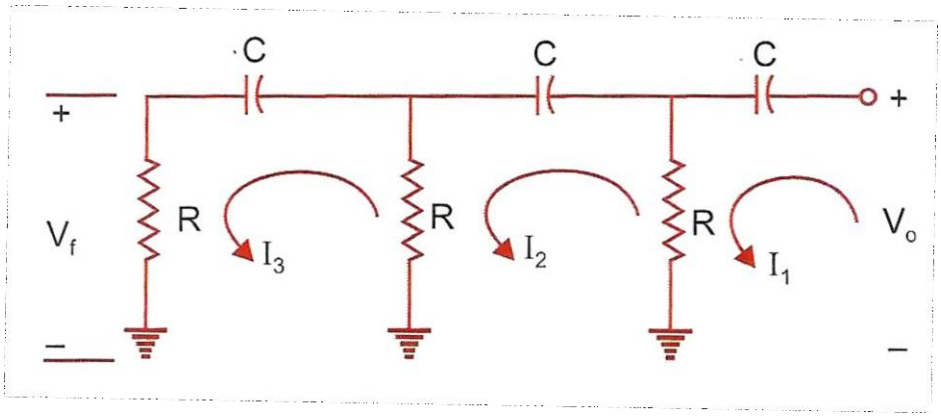


Fig.2.2.1.b. RC Phase Shift Oscillator- Feedback network

Derivation of frequency of oscillation of RC Phase shift oscillator

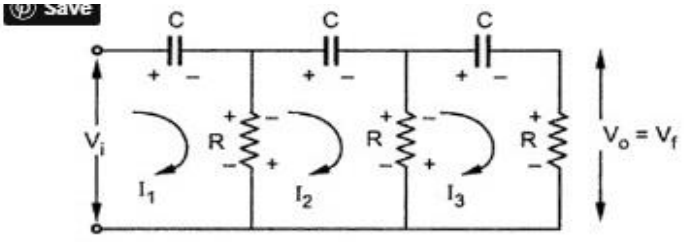


Fig. 2.13

Applying KVL to various loops we get,

$$I_1\left(R+\frac{1}{j\omega C}\right)-I_2 R = V_i \quad \ldots (15)$$

$$-I_1 R + I_2\left(2R+\frac{1}{j\omega C}\right)-I_3 R = 0 \quad \ldots (16)$$

$$0 - I_2 R + I_3\left(2R+\frac{1}{j\omega C}\right) = 0 \quad \ldots (17)$$

Replacing jω by s and writing the equations in the matrix form,

$$\begin{vmatrix} R+\frac{1}{sC} & -R & 0 \\ -R & 2R+\frac{1}{sC} & -R \\ 0 & -R & 2R+\frac{1}{sC} \end{vmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} = \begin{bmatrix} V_i \\ 0 \\ 0 \end{bmatrix} \quad \ldots (18)$$

Using the Crammer's rule to obtain I_3

$$D = \begin{vmatrix} \frac{1+sRC}{sC} & -R & 0 \\ -R & \frac{1+2sRC}{sC} & -R \\ 0 & -R & \frac{1+2sRC}{sC} \end{vmatrix}$$

$$= \frac{(1+sRC)(1+2sRC)^2}{s^3 C^3} - \frac{R^2(1+2sRC)}{sC} - \frac{R^2(1+sRC)}{sC}$$

$$= \frac{(1+sRC)(1+4sRC+4s^2C^2R^2) - R^2 s^2 C^2 [1+2sRC+1+sRC]}{s^3 C^3}$$

$$= \frac{1+5sRC+8s^2C^2R^2+4s^3C^3R^3-3s^3R^3C^3-2R^2s^2C^2}{s^3C^3}$$

$$= \frac{1+5sRC+6s^2C^2R^2+s^3C^3R^3}{s^3C^3} \quad \ldots (19)$$

$$D_3 = \begin{vmatrix} \frac{1+sRC}{sC} & -R & V_i \\ -R & \frac{1+2sRC}{sC} & 0 \\ 0 & -R & 0 \end{vmatrix}$$

$$= V_i R^2 \quad \ldots (20)$$

$$\therefore \quad I_3 = \frac{D_3}{D} = \frac{V_i R^2 s^3 C^3}{1+5sRC+6s^2C^2R^2+s^3C^3R^3}$$

Now $$V_o = V_f = I_3 R = \frac{V_i R^2 s^3 C^3}{1+5sRC+6s^2C^2R^2+s^3C^3R^3} \quad \ldots (21)$$

$$\therefore \quad \beta = \frac{V_o}{V_i} = \frac{R^3 s^3 C^3}{1+5sCR+6s^2C^2R^2+s^3C^3R^3} \quad \ldots (22)$$

Replacing s by $j\omega$, s^2 by $-\omega^2$, s^3 by $-j\omega^3$

$$\therefore \quad \beta = \frac{-j\omega^3 R^3 C^3}{1+5j\omega CR-6\omega^2C^2R^2-j\omega^3C^3R^3}$$

Dividing numerator and denominator by $-j\omega^3R^3C^3$ and replacing $\frac{1}{\omega RC}$ by α we get,

$$\therefore \quad \beta = \frac{1}{1+6j\alpha-5\alpha^2-j\alpha^3}$$

$$\therefore \quad \boxed{\beta = \frac{1}{(1-5\alpha^2)+j\alpha(6-\alpha^2)}} \quad \ldots (23)$$

To have phase shift of 180°, the imaginary part in the denominator must be zero.

$$\therefore \quad \alpha(6-\alpha^2) = 0$$

$$\therefore \quad \alpha^2 = 6 \qquad \text{neglecting zero value}$$

$$\boxed{\alpha = \sqrt{6}}$$

$$\therefore \quad \frac{1}{\omega RC} = \sqrt{6}$$

$$\therefore \quad \omega = \frac{1}{RC\sqrt{6}}$$

$$\boxed{f = \frac{1}{2\pi RC\sqrt{6}}}$$

This is the frequency with which circuit oscillates,

At this frequency,

$$\beta = \frac{1}{1-5\times\left(\sqrt{6}\right)^2} = -\frac{1}{29}$$

The negative sign indicates a phase shift of **180°**

$$\therefore \quad \boxed{|\beta| = \frac{1}{29}} \qquad \ldots (25)$$

Now to have the oscillations, $|A\beta| \geq 1$

$$\therefore \quad |A|\,|\beta| > 1$$

$$|A| \geq \frac{1}{|\beta|} \geq \frac{1}{\left(\frac{1}{29}\right)}$$

Thus circuit will work as an oscillator which will produce a sinusoidal waveform if the gain is 29 and total phase shift around a loop is 360°. This satisfies the Barkhausen criterion for the oscillator. These oscillators are used over the audio frequency range i.e. about 20 Hz up to 100 kHz.

Pblm.2.2.1-Solved Problem:

The capacitor value of an RC phase shift oscillator using OP AMP is 0.01µF and the desired frequency of oscillation is 25 KHz. The voltage gain of the amplifier should be 30. Thus calculate the value of R of RC feedback network, input resistor R1 and feedback resistor R2 connected to the amplifier.

Solution:

Value of R in RC feedback network:

Given C=0.01 µF, and Frequency f= 25 KHz.

$$f = \frac{1}{2\pi RC\sqrt{6}}$$

$$R = \frac{1}{2\pi fC\sqrt{6}}$$

$$R = \frac{1}{2\pi * 25 * 10^{3} * 0.01 * 10^{-6} * \sqrt{6}}$$

$$R = 260\ K\Omega$$

Thus Resistor R value in RC network is 260 K□.

Value of R1 in amplifier circuit:

Given A=30. R1 or R2 are not given and thus we can assume any one resistor value. If R1 is assumed to be 1K□ then R2 can be estimated. Since it is an inverting amplifier

Its gain is,

$$A = \left| \frac{-R2}{R1} \right|$$

$$30 = \frac{R2}{1K\Omega}$$

$$R2 = 30\,K\Omega$$

Thus Resistor R2 (acts as a feedback resistor) value in amplifier is 30 K□.

2.2.2. Wien's Bridge Oscillators

Unlike RC phase shift oscillator, Wien bridge oscillator never uses phase-shift concept. It uses balancing concept of lead-lag network.

Construction: Here this oscillator is connected in a bridge fashion. The inverting terminal is connected to a junction where resistors R_3 and R_F are connected. The other end of R_3 is grounded and R_F is connected to output terminal of the amplifier. This forms a reference voltage across R_3 being fed into inverting terminal as shown in the fig. 2.2.2.a & 2.2.2.b

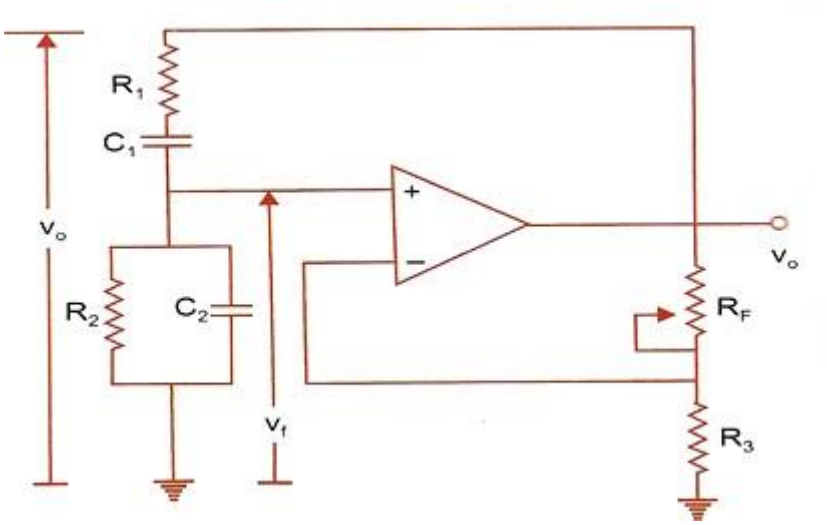


Fig.2.2.2.a. Wien's Bridge Oscillator

The non-inverting connected in between two reactance offering components Z_1 and Z_2 as shown in the fig. 2.2.2.b. Z_1 comprises of serially connected resistor R_1 and capacitor C_1 whereas Z_2 comprises of parallel connected resistor R_2 and capacitor C_2. This combination of Z_1 and Z_2 is termed as *lead-lag circuit.*

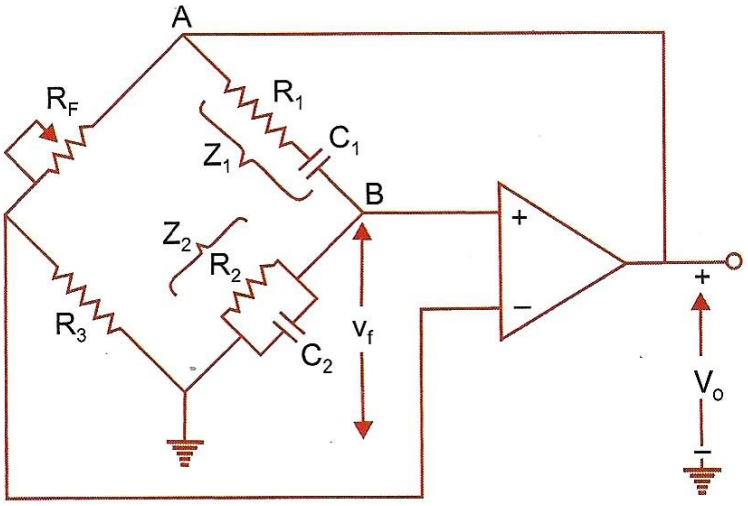


Fig.2.2.2.b. Wien's Bridge Oscillator-Reconstructed

Working: Here the reactive circuits Z_1 and Z_2 connected to non-inverting terminal at B as shown in the fig. 3.3.2.b. A noise voltage is generated between the imbalanced input terminals is amplified by the amplifier and fed in the bridge circuit.

For particular low-frequencies, the capacitors act as open circuit and thus the output voltage of lead-lag circuit shall be zero and for high frequencies the capacitors cat as short circuit and thus voltage shall be zero. Only for a particular frequency called *resonant frequency*, resistance value equals to capacitive reactance value. Thus maximum current is available at this frequency only. So the output appears only for resonant frequency.

The other resistor values of R_3 and R_F of bridge are adjusted to enhance the output to a maximum level. Thus the oscillation is generated.

The amplifier is a non-inverting amplifier circuit and so no phase shift is introduced. Phase shift is 0° (or 2□) for the whole circuit. And the overall gain shall be also more than 1. Thus the Barkhausen's criteria for sustained oscillations are satisfied.

If $R_1 = R_2 = R$ and $C_1 = C_2 = C$ then $R = X_C$ at resonant frequency where X_C is capacitive reactance of C.

Thus

$$R = X_C = \frac{1}{2\pi f C}$$

$$f = \frac{1}{2\pi RC}$$

This is the frequency of oscillation

2.3 OP-AMP MULTIVIBRATORS

Multivibrators are square wave oscillators that produce pulse waveforms with various ON time and OFF time. As shown in fig. 2.3.a, P1, P2 and P3 are ON time of the pulse whose total time period is 10 ms with T_{ON} and T_{OFF} are 3.5 ms and 6.5 ms respectively. T_{ON} and T_{OFF} are two states of the pulse. The place where T_{ON} transits to T_{OFF} or T_{OFF} to T_{ON} is termed as *state transition*.

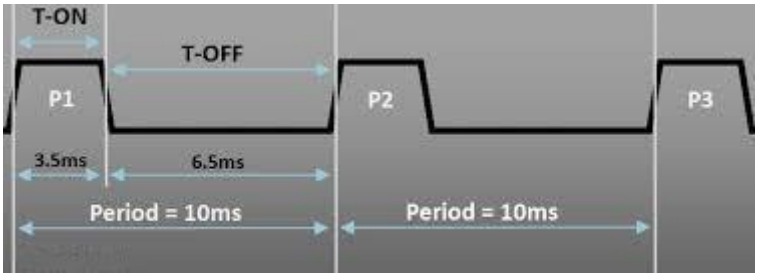


Fig.2.3.a. Pulse waveform - model

The state transition may have slope (with a small time for transition) or infinite slope (No time for transition-being abrupt).

There are three types of multivibrators available according to their state transition. They are (a.) astable, (b.) monostable, and (c). bistable multivibrators.

Astable multivibrator is one that generates pulses those transits from one state to another without any external trigger. It is done by its free-will controlled by the design aspects. Thus this is called *free-running* multivibrator. So the states are not stable for a long time, the states can be termed as Quasi-stable states. Hence this multivibrator generates pulses of no stable states, it is termed as astable multivibrator.

Monostable multivibrator is one that generates pulses those transits from one state to another with the help of *one* external trigger. The multivibrator remains in one state (stable state) and when an external pulse is applied then it transits state from present Stable state to a quasi- stable state. It remains at quasi-stable state for a time period of T as it is designed and then returns to a stable state without any external trigger. Since it changes state from stable to quasi- stable using one external trigger, it is termed as one-shot multivibrator or monostable multivibrator.

Bistable multivibrator is one that generates pulses those transits from one state to another with the help of two external trigger. The multivibrator remains in one state (stable state) and when an external pulse is applied then it transits state from present Stable state to a next stable state. It remains at second stable state until another external trigger is applied. Thus this multivibrator has stable states only and the transitions happen only when triggers are applied, it is termed as bistable multivibrators.

Other related terminology: Duty cycle means

$$D = \frac{T_{ON}}{T_{ON} + T_{OFF}} \%$$

If T_{ON} is 5 ms and T_{OFF} is 10 ms, then Duty cycle D=5/15 ms,
D=33%. D=50%, then $T_{ON} = T_{OFF}$

Possible questions:

What is a Multivibrator?

Define the terminology of astable, monostable and bistable multivibrators.

2.3.1. Astable Multivibrators

These multivibrators are termed as *"Free Running"* multivibrators, and they have only quasi stable states as seen earlier in introduction.

The circuit diagram of astable multivibrator using Operational amplifier is shown below fig.

2.3.1.a.

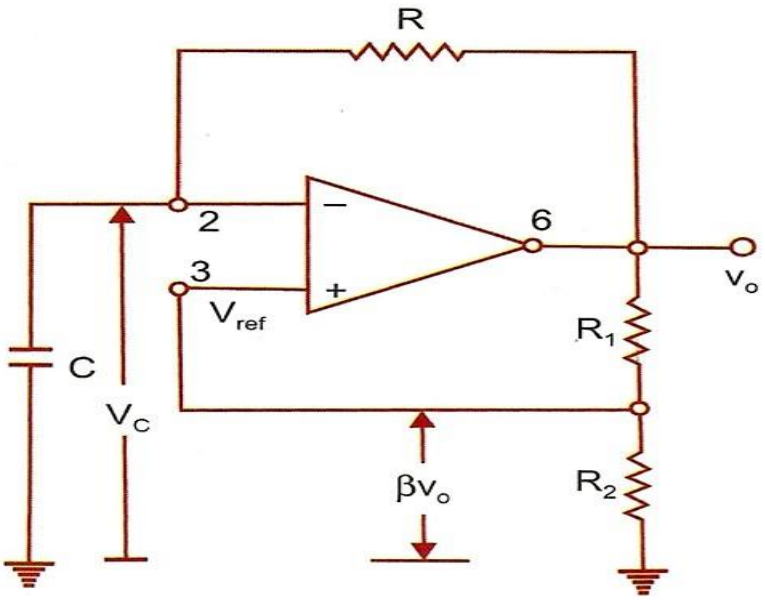


Fig.2.3.1.a. Astable Multivibrator – Circuit Diagram

Construction:

The circuit as simple and resembles like OP AMP Schmitt trigger circuit. One end of a capacitor C and a resistor R are connected to the inverting terminal. The other end of the resistor is connected to the output terminal and that of capacitor is connected to ground terminal. This capacitor C and feedback resistor R decide the period for oscillation of the multivibrator. A resistor R1 is connected between the output terminal and non-inverting terminal and another resistor R2 is

connected between non-inverting terminal and ground terminals. If the output voltage is considered as V_o, then the voltage tapped between R2 shall be a reference voltage applied to the non-inverting terminal with amplitude of βV_o where β is feedback factor for comparison.

Working:

Considering fig. 2.3.1.a and 2.3.1.b, the working part of this generator can be explained.

At Time 0: At time 0, assume the output transits from $-V_{sat}$ to $+V_{sat}$. Since the output is $+V_{sat}$ at time 0, reference voltage $+\beta V_o$ and capacitor voltage is $-\beta V_o$.

From Time 0 to Time T1: Since reference is at $+\beta V_o$, the inverting terminal is also at $+\beta V_o$ due to virtual ground. Now the capacitor tries to charge till the output voltage $+V_o$. It reaches $+\beta V_o$ and tries to charge more, then the inverting terminal go beyond reference voltage $+\beta V_o$ after time constant RC.

At Time T1: At time T1, since the inverting terminal goes little above than reference voltage $+\beta V_o$, the output transits from $+V_{sat}$ to $-V_{sat}$. Now capacitor voltage remains at $+\beta V_o$. The reference voltage at non-inverting terminal is at $-\beta V_o$. The time T1 is decided by RC (time constant) factor.

After Time T1: Since reference is at $-\beta V_o$, the inverting terminal is also at $-\beta V_o$ due to virtual ground. Now the capacitor tries to charge till the output voltage $-V_o$. It tries to reach $-\beta V_o$ and tries to charge more, then the inverting terminal go beyond reference voltage $-\beta V_o$ after time RC (time constant). Now again whatever happened at time 0 happens again. These 3 steps repeat periodically till power is available for the circuit.

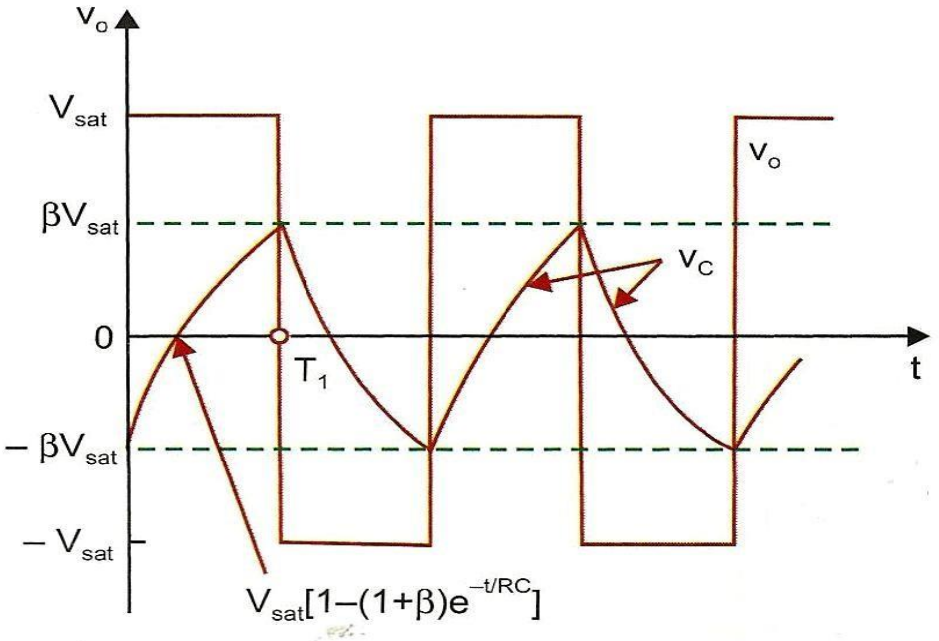


Fig.2.3.1.b. Astable Multivibrator – Output Waveforms

DERIVATION OF FREQUENCY OF OSCILLATION FOR OP-AMP ASTABLE MULTIVIBRATOR

Generally

$$V_C = V_{final} + (V_{initial} - V_{final})e^{-t/RC}$$

Where V_C is capacitor voltage, $V_{initial}$ and V_{final} are capacitors' initial and final charging voltages respectively, t is the time function, RC is time constant where R and C are value of Resistor and capacitor attached to inverting terminal of the op-amp.

In this circuit

$$.V_{initial} = -\beta V_{sat}$$

$$.V_{final} = V_{sat}$$

but capacitor charges upto $+\beta V_{sat}$ only

Now substituting these values in equation above

$$V_C = V_{sat} + (-\beta V_{sat} - V_{sat})e^{-t/RC}$$

$$V_C = V_{sat} - V_{sat}(1+\beta)e^{-t/RC}$$

At time T_1, V_C is $+\beta V_{sat}$ (in waveform fig.2.3.1.b), the above equation becomes

$$V_C = \beta V_{sat} = V_{sat} - V_{sat}(1+\beta)e^{-T_1/RC}$$

At time T_1, V_C is $+\beta V_{sat}$ (in waveform fig.2.3.1.b), the above equation becomes

$$V_C = \beta V_{sat} = V_{sat} - V_{sat}(1+\beta)e^{-T_1/RC}$$

$$V_{sat}(1+\beta)e^{-T_1/RC} = V_{sat} - \beta V_{sat}$$

$$V_{sat}(1+\beta)e^{-T_1/RC} = V_{sat}(1-\beta)$$

$$e^{-T_1/RC} = \frac{V_{sat}(1-\beta)}{V_{sat}(1+\beta)}$$

$$\frac{1}{e^{T_1/RC}} = \frac{(1-\beta)}{(1+\beta)}$$

Inverting both sides we get,

$$e^{T_1/RC} = \frac{(1+\beta)}{(1-\beta)}$$

Taking Natural logarithm on both sides,

$$T_1/RC = ln\frac{(1+\beta)}{(1-\beta)}$$

$$T_1 = RC\ ln\frac{(1+\beta)}{(1-\beta)}$$

But as shown in the figure, T_1 is only ON time and T is the total cycle time which is T_1+T_2 where T_2 is considered $=T_1$.

Then $T=2T_1$,

$$T = 2RC\ ln\frac{(1+\beta)}{(1-\beta)}$$

Since $\beta = \frac{R_2}{R_1+R_2}$ (feedback Factor), R_1 and R_2 decides value of β,

Case 1:

If $R_1=R_2$, then $\beta = \frac{1}{1+1} = 0.5$. Then

$$T = 2RC\ ln\frac{(1.5)}{(0.5)}$$

$$T = 2RC\ \ln(3)$$

$$T = 2RC\ (1.0986)$$

$$T = 2.1972\ RC$$

Case 2:

If R_1=1.16 R_2, then $\beta = \frac{1}{1+1.16} = 0.462$ Then

$$T = 2RC \ln(2.718)$$

as $\ln(2.718) = 1$

$$T = 2RC\ (1)$$

$$T = 2RC$$

Thus when R_1=1.16 R_2,

The frequency of oscillation of Astable multivibrator is

$$f = 1/T = 1/2RC$$

2.3.2. Monostable Multivibrators

These multivibrators are termed as *"one-shot multivibrators"* and they have only one stable state and other is quasi-stable state induced by single external trigger as seen earlier in introduction.

The circuit diagram of monostable multivibrator using Operational amplifier is shown below fig. 2.3.2.a.

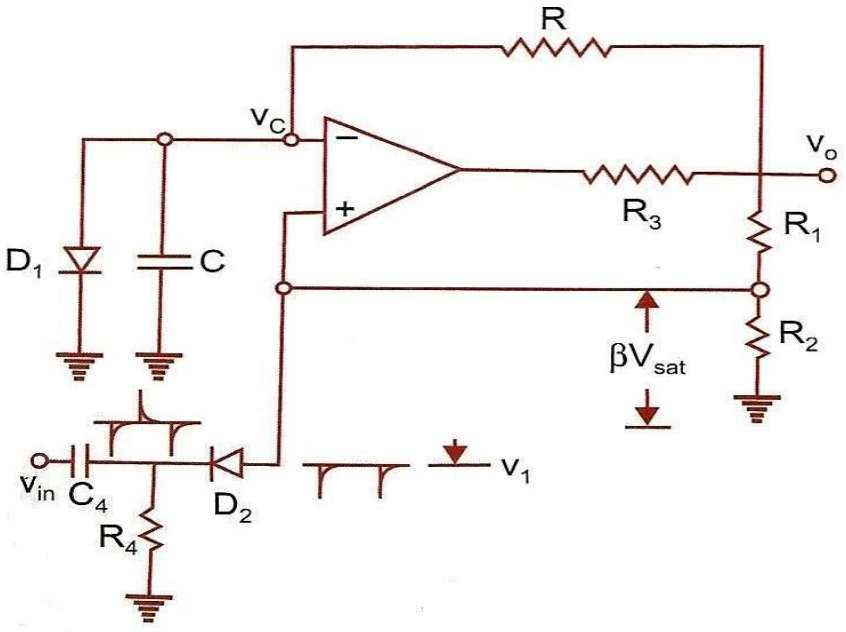


Fig.2.3.2.a. Monostable Multivibrator Using OP AMP

Construction:

The circuit as simple and resembles like OP AMP Schmitt trigger circuit. One end of a capacitor C and a resistor R are connected to the inverting terminal. The other end of the resistor is connected to the output terminal and that of capacitor is connected to ground terminal. A diode D1 is connected parallel to the capacitor C. This capacitor C and feedback resistor R decide the period for T of the multivibrator. A resistor R1 is connected between the output terminal and non-inverting terminal and another resistor R2 is connected between non-inverting terminal and ground terminals. If the output voltage is considered as V_o, then the voltage tapped between R2 shall be a reference voltage applied to the non-inverting terminal with amplitude of βV_o where β is feedback factor for comparison.

A pulse trigger circuit consisting of diode D2 and a differentiator circuit connected to pulse generator of negative pulse width T_P. The anode of the diode D2 is connected to non-inverting terminal

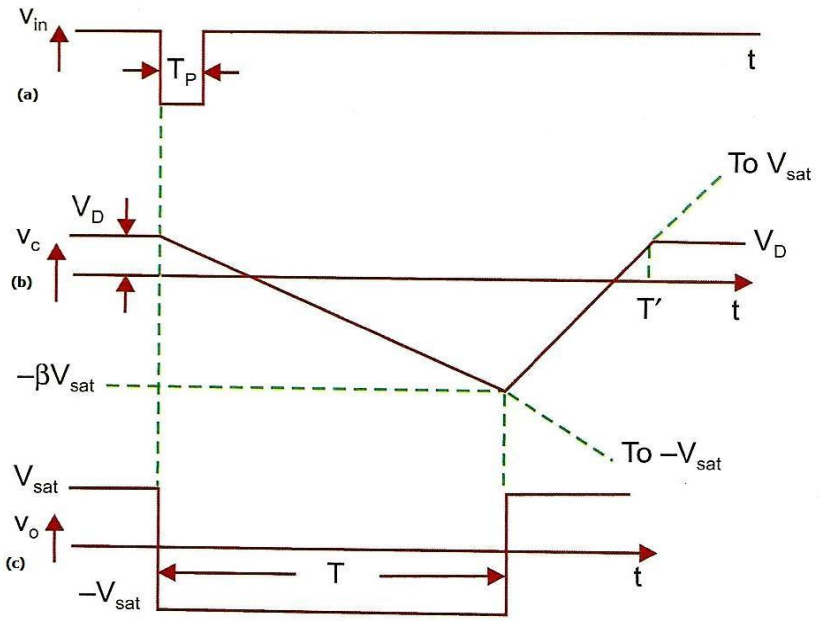


Fig.2.3.2.b. Monostable Multivibrator - Waveforms

Working:

Considering fig."s 2.3.2.a and 2.3.2.b, the working part of this generator can be explained. In fig. 2.3.2.b has three waveforms. Waveform *a* shows the pulse trigger waveform whose trigger pulse width is T_P, waveform *b* shows voltage output V_C across capacitor C and waveform *c* shows

the monostable output V_o of quasi-stable state of time T.

Before pulse trigger: At time before pulse trigger, assume the output is at $+V_{sat}$. Since the output is at $+V_{sat}$, then reference voltage is at $+\beta V_o$ and so capacitor voltage V_C tries to charge towards $+V_{sat}$. Due to this the diode D1 gets forward biased when inverting terminal is positive, and the diode D1 starts conducting beyond 0.7V (Approximate cut-in voltage of Silicon diode). Thus the diode D1 conducts and provides a short path beyond 0.7V, and hence the capacitor C which is parallel can charge upto 0.7V only. So now the capacitor voltage V_C is 0.7V.This voltage is shown as V_D in the fig. 2.3.2.b waveform (*b)*.

At time of pulse trigger: As shown in fig. 2.3.2.b waveform (*a* & *b*), a negative pulse trigger is applied at non-inverting terminal and its amplitude being $-V_{in}$. Hence at the non-inverting terminal, pulse voltage $-V_{in}$ and reference voltage $+\beta V_{sat}$ exists. The total voltage is $(+\beta V_{sat} - V_{in})$. The amplitude of this voltage is less than 0.7V due to existence of diode D2 which is forward biased (ON) due to –ive trigger pulse (Cathode of the diode D2 is negative due to $-V_{in}$ and anode is positive due to $+\beta V_{sat}$).

Now non-inverting terminal acts as reference terminal of an inverting comparator. At this point inverting terminal is at 0.7V and non-inverting reference voltage is below 0.7V. Hence inverting terminal is more than reference voltage at non-inverting terminal and the output transits from $+V_{sat}$ to $-V_{sat}$ as shown in fig. 2.3.2.b waveform (*c*). That is output transited from stable high state to low state.

The capacitor voltage V_C is at 0.7V and output is at $-V_{sat}$. Hence the capacitor C starts charging towards $-V_{sat}$ through the resistor R. The non-inverting terminal reference voltage is less than 0.7V.

At Time AFTER pulse trigger: When pulse trigger ends after time T_P, it becomes positive. So the cathode of diode D2 is at positive voltage and anode is at $-\beta V_{sat}$. Thus the diode D2 is in reverse bias condition (OFF). Due to this the non-inverting voltage is affected only by reference voltage across resistor R2 which is $-\beta V_{sat}$.

Now reference voltage is at $-\beta V_{sat}$ and the charging capacitor is charging towards $-V_{sat}$. but when capacitor voltage V_C reaches just above $-\beta V_{sat}$, output transits from $-V_{sat}$ to $+V_{sat}$ (Inverting terminal voltage V_C is more than reference voltage at non-inverting terminal). This transition happens at time T from start of pulse trigger where T is decided by RC time constant. That is capacitor C took time period of T for charging from V_D to $-\beta V_{sat}$ which is through resistor R. The output stays at a quasi-stable state for a time period of T.

After Time T: Now output voltage V_o is at $+V_{sat}$ and reference voltage at non-inverting terminal is at $+\beta V_{sat}$. The capacitor starts charging from $-\beta V_{sat}$ to $+V_{sat}$. But when the capacitor voltage V_C increases more than V_D, diode D1 is forward biased and starts conducting. Hence the

capacitor voltage V_C cannot charge beyond V_D. The waveform is shown in fig. 2.3.2.b waveform (*a*). As seen initially, now the amplitude at inverting terminal is V_D due to charge of capacitor, non-inverting terminal voltage is at $+\beta V_{sat}$. The output is a negative pulse voltage whose time period is T. This negative pulse was generated due to an external negative trigger (one-shot trigger). The output transit from a stable high state to a low quasi-stable state time T and then to a stable high state. This is a monostable waveform because it has one stable state and a quasi-stable state. In next section, discussion about derivation of time period T is done.

DERIVATION OF FREQUENCY OF OSCILLATION FOR OP-AMP MONOSTABLE MULTIVIBRATOR

Analysis of capacitor voltage V_C(across capacitor C)

Generally

$$V_C = V_{final} + (V_{initial} - V_{final})e^{-t/RC}$$

Where V_C is capacitor voltage, $V_{initial}$ and V_{final} are capacitors' initial and final charging voltages respectively, t is the time function, RC is time constant where R and C are value of Resistor and capacitor attached to inverting terminal of the op-amp.

In this circuit,

$$V_{initial} = V_D$$

$$V_{final} = -V_{sat}$$

Where (V_D= Diode Forward voltage)

Now substituting these values in equation above

$$V_C = V_{sat} + (V_D - (-V_{sat}))e^{-t/RC}$$

$$V_C = -V_{sat} + (V_D + V_{sat})e^{-t/RC}$$

At time T_1, V_C is $-\beta V_{sat}$ (in waveform fig.2.3.2.b), the above equation becomes

$$V_C = -\beta V_{sat} = -V_{sat} + (V_D + V_{sat})e^{-T/RC}$$

$$(V_D + V_{sat})e^{-T/RC} = V_{sat} - \beta V_{sat}$$

Dividing by V_{sat},

$$(\frac{V_D}{V_{sat}} + 1)e^{-T/RC} = 1 - \beta$$

$$e^{-T/RC} = \frac{1 - \beta}{(\frac{V_D}{V_{sat}} + 1)}$$

$$\frac{1}{e^{T_1/RC}} = \frac{1 - \beta}{(\frac{V_D}{V_{sat}} + 1)}$$

Inverting both sides we get,

$$e^{T_1/RC} = \frac{(\frac{V_D}{V_{sat}} + 1)}{1 - \beta}$$

$$T_1 = RC\ ln\frac{(\frac{V_D}{V_{sat}} + 1)}{1 - \beta}$$

But as shown in the figure, T_1 is time period of Monostable multivibrator, it is considered as T

Then $T=T_1$,

$$T = 2RC\ ln\frac{(\frac{V_D}{V_{sat}} + 1)}{1 - \beta}$$

If $V_{sat} >> V_D$ then V_D / V_{sat} becomes negligible and $R_1=R_2$, then $\beta=0.5$,

$$T = 2RC\ ln\frac{(0 + 1)}{1 - 0.5}$$

$$T = 2RC\ \ln(2)$$

$$T = 0.69RC$$

The frequency of oscillation of monostable multivibrator is (if $R_1=R_2$)

$$f = 1/T = 1/0.69RC$$

$$f = 1/T = 1.45/RC$$

Possible question:

Explain the construction and working of monostable multivibrator using OP AMP with neat sketches.

2.4 OP-AMP RECTIFIERS

2.4.1 PRECISION RECTIFIERS

Rectifiers convert bipolar AC signals into unipolar DC signals. The circuit mainly uses diodes that block signals when reverse biased and allow signals when forward biased. But when forward biased diode can only allow signals above 0.7V (cut-in voltage of Silicon diode). So the rectifier cannot precisely rectify ac signals of peak to peak voltages below 0.7V. For eradicating this disadvantage of not rectifying signals below 0.7V we use operational amplifiers for rectification.

OP AMP inverting amplifier circuits are added with diodes to function as precision rectifiers to rectify voltages below 0.7V (cut-in voltages).

2.4.1. Precision Half-wave Rectifiers

As discussed this precision rectifier is used for rectifying ac signals below cut-in voltages.

Circuit construction: An inverting amplifier with input resistor R1 and feedback resistor R2 is altered by adding two diodes D1 and D2 in series as shown in the fig. 2.4.1.a. D1 is connected between output terminal of OP AMP and resistor R2 as shown and diode D2 is connected between input inverting terminal and anode of the diode D1.

Working: An AC signal V_{in} is applied to the inverting terminal and output V_o is tapped at the cathode of diode D1 and one end of resistor R2 as shown in the following fig. The analysis of this circuit in both positive and negative cycle becomes essential.

In positive cycle: **The inverting terminal becomes positive in positive input cycle and since it is an inverting amplifier and output terminal becomes negative. Thus Diode D1 becomes reverse biased and remains in OFF state but diode D2 becomes forward biased and remains ON. Since Diode D1 is OFF and diode D2 is ON and D2 provides short circuit between inverting and non- inverting terminals, so the output V_{out} is zero.**

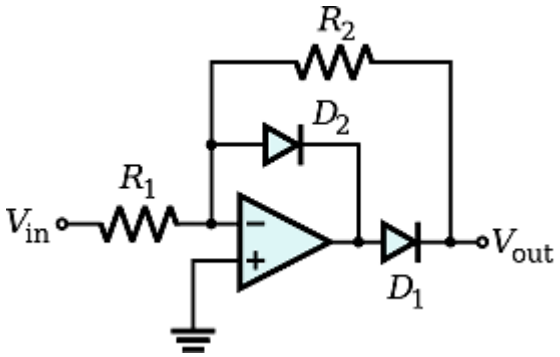


Fig. 2.4.1.a Half-wave precision rectifier

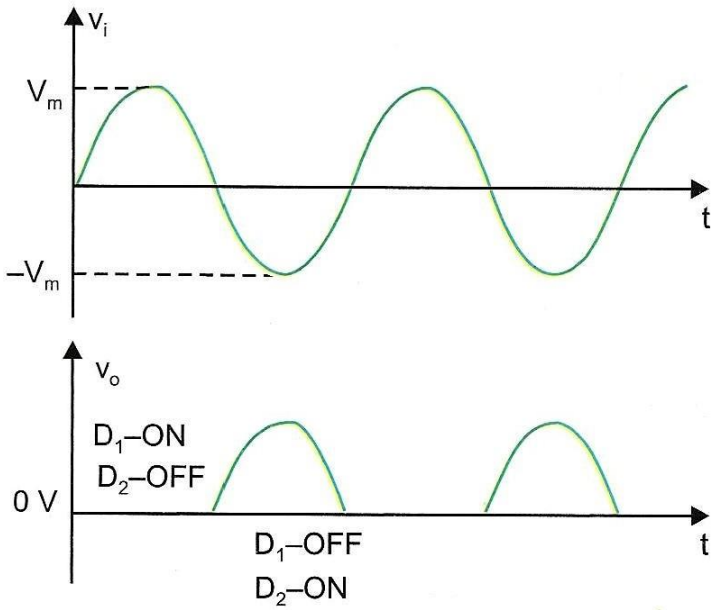


Fig. 2.4.1.b Half-wave precision rectifier-waveforms

In negative cycle: **The inverting terminal becomes negative in negative input cycle and since it is an inverting amplifier and output terminal becomes positive. Thus Diode D1 becomes forward biased and remains in ON state but diode D2 becomes reverse biased and remains OFF. Since Diode D1 is ON and diode D2 is OFF and provides high resistance path between inverting and non-inverting terminals. But resistor R2 provides alternate path between input and output. Since D1**

is ON, it connects V_{out} with output terminal. Now the circuit becomes normal inverting amplifier and so output V_{out} is the input multiplied by scaling factor (-R2/R1).

Thus the rectifier circuit allows one cycle (negative half cycle of the input) but blocks other cycle (positive half cycle). Since the diode doesn't directly involve in rectification and OP AMP has high gain factor, this circuit rectifies even signals less than cut-in voltage. The waveforms are shown in the fig. 2.4.1.b.

2.4.2. Precision Full-wave Rectifiers

Circuit construction: Two inverting amplifiers with input resistor R and feedback resistor R is altered by adding two diodes D1 and D2 in series as shown in the fig. 2.4.2.a. D1 is connected between output terminal of OP AMP and feedback resistor R as shown and diode D2 is connected between output terminal and other end of the resistor R connected to inverting terminal of the first OP AMP and also connected to non-inverting terminal of the second OP AMP.

Working: An AC signal V_i is applied to the inverting terminal through the resistor R and output V_o is tapped at output of second OP AMP as shown in the following fig. The analysis of this circuit in both positive and negative cycle becomes essential.

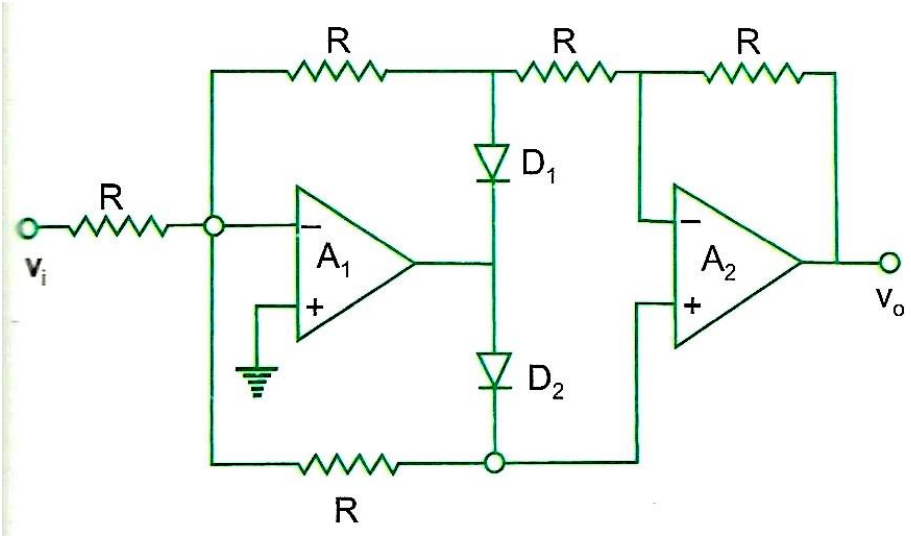


Fig. 2.4.2.a Full-wave precision rectifier

In positive cycle: **The inverting terminal of first OP AMP becomes positive, in positive input cycle and diode D1 is forward biased. But diode D2 is reverse biased because output terminal becomes negative. Now D1 is ON and D2 is OFF. The circuit looks as shown in fig. 2.4.2.b. Thus output voltage V_o is double inverted signal of input voltage V_i. Since gain of both amplifiers is R/R=1, and $V_o = V_i$.**

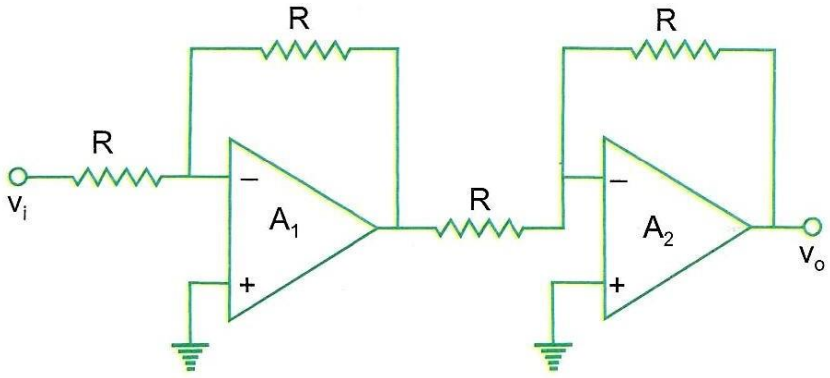


Fig. 2.4.2.b Full-wave precision rectifier-during positive half cycle

In negative cycle: **The inverting terminal of the first OP AMP becomes negative in negative input cycle, the Diode D1 becomes reverse biased and remains in OFF state but diode D2 becomes forward biased and remains ON. Since Diode D1 is OFF and diode D2 is ON as shown in fig. 2.4.2.c. But resistor R provides alternate path between input and output. In second amplifier, voltage at inverting terminal is V/2R volts and non-inverting terminal is V/R. thus**

non-inverting terminal of second amplifier holds two times of voltage than inverting terminal. Thus output voltage V_o is ((V/R)-(V/2R)=V/2R) and is adjusted by changing the value of Feedback resistor R of second amplifier. Hence we get output for negative half-cycle too.

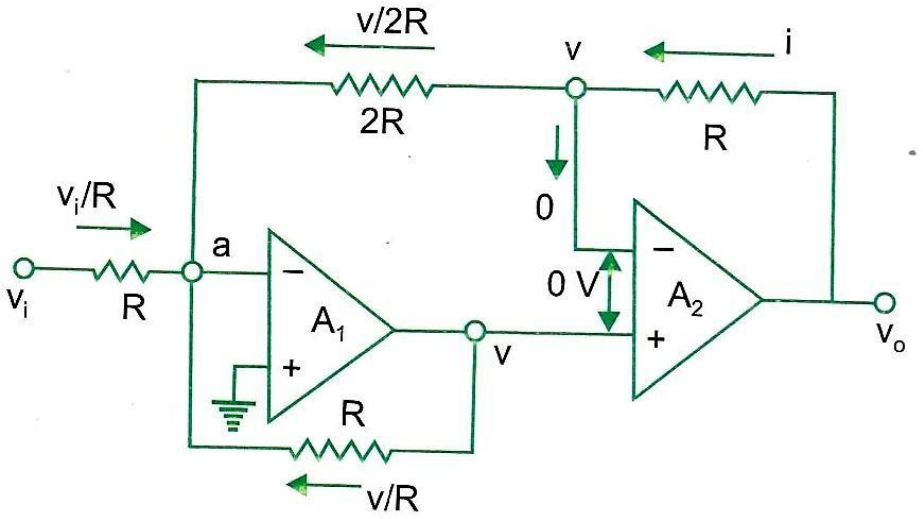


Fig. 2.4.2.c Full-wave precision rectifier-during negative half cycle

This is shown in the fig. of waveforms fig. 2.4.2.d. thus this rectifier converts bipolar AC input to unipolar DC output.

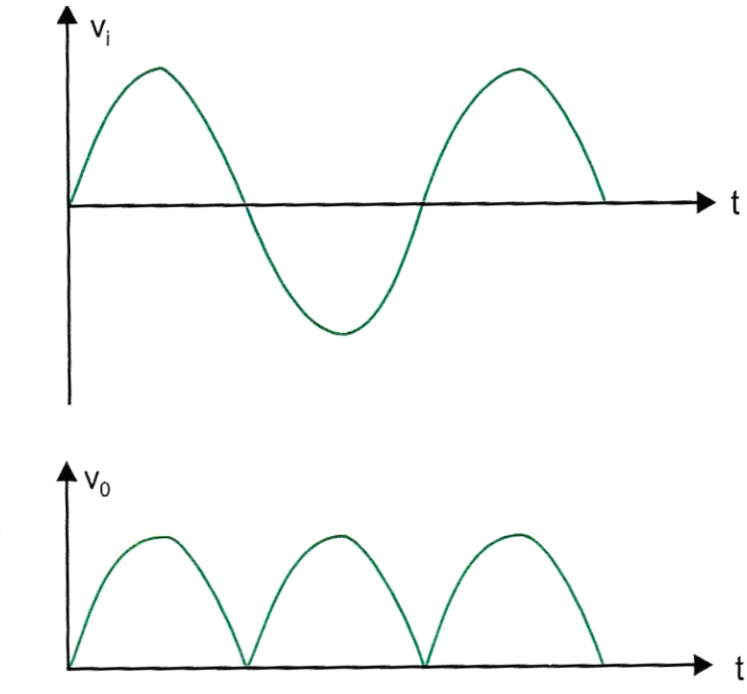


Fig. 2.4.2.d Full-wave precision rectifier waveform

Possible questions:

What is the principle behind precision rectification?

Explain the construction and working of half and full wave precision rectifiers with neat sketches

Text Book References:

1. Ramakant A.Gayakwad, "0P-AMP and Linear ICs", 4th Edition, Prentice Hall / Pearson Education, 1994.

2. D.Roy Choudary, Shail Jain, "Linear Integrated Circuits", New Age International Pvt. Ltd., 2000.

3. Grey and Meyer, "Analysis and Design of Analog Integrated Circuits, 4th Edition, Wiley International, 2001.

4. Michael Jacob, "Applications and Design with Analog Integrated Circuits, 2nd Edition, Prentice Hall of India, 1993.

5. S. Salivahanan, V.S. Kanchana Bhaaskaran, "Linear integrated circuits", 3rd Edition, McGraw-Hill, 2011.

6. William D.StanelY, "Operational Amplifiers with Linear Integrated Circuits", 4th Edition, Pearson Education, 2004.

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UNIT – III

A/D AND D/A CONVERTERS

3.1 INTRODUCTION

- **Most of the real world physical quantities such as voltage, current, temperature, pressure and time etc are available in analog form**
- **Even though an analog signal represents a real physical parameter with accuracy, it is difficult to process, store or transmit the analog signal without errors because of the superimposition of noise.**
- **Therefore for processing, transmission and storage purposes, it is often convenient to express these variables in digital form it gives better accuracy and reduces noise.**
- **The operation of any digital communication system is based on A/D conversion or D/A conversion**

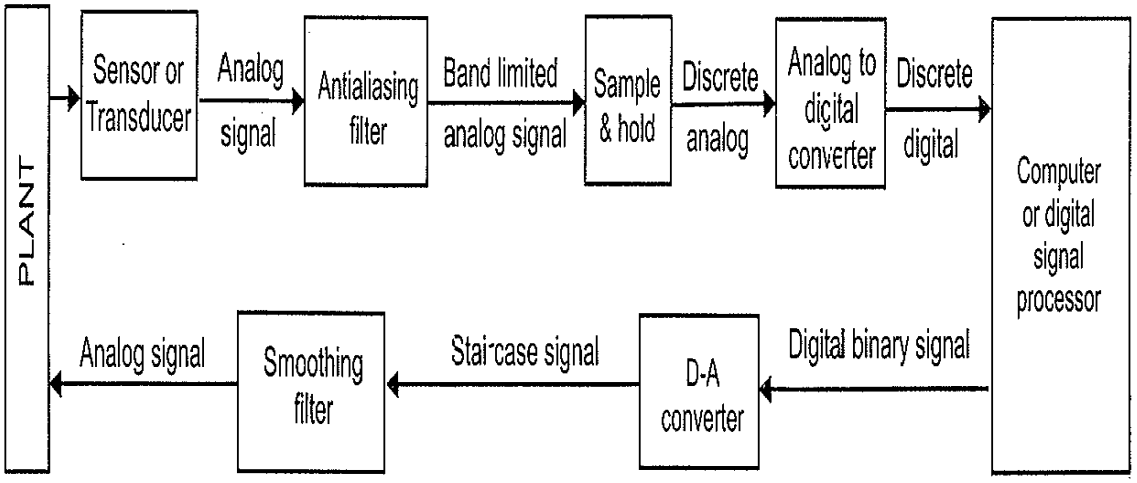


Figure:3.1: Circuit Showing application of A/D and D/A convertor

Block diagram explanation:

- **The analog signal obtained from the transducer is bandlimited by antialiasing filter.**
- **The signal is then sampled at a frequency rate more than twice the maximum frequency of the band limited signal.**
- **The sampled signal has to be held constant while conversion is taking place in A/D converter.**
- **This requires that ADC should be preceded by a sample and hold (S/H) circuit**
- **The ADC output is a sequence in binary digit. The micro- computer or Digital signal Processor performs the numerical calculations of the desired control algorithm.**
- **The DAC converter is operated at the same frequency of the ADC converter**
- **The output of DAC converter is usually a staircase. This staircase like digital output is passed through a smoothing filter to reduce the effect of noise.**

3.2 Applications of ADC and DAC:

This scheme is used either in full or in part in applications such as

1. **Digital audio recording and playback**
2. **Computer**
3. **Music and video synthesis**
4. **Pulse code modulation transmission**
5. **Data acquisition**
6. **Digital multimeter**
7. **Direct digital control**
8. **Digital signal processing**
9. **Microprocessor based instrumentation**

Both ADC and DAC are known as data convertors and available in IC forms

1.What is the decimal equivalent of 1010?

$$\text{Decimal equivalent of } 1010 = 1 \times 2^3+0 \times 2^2+1 \times 2^1+0 \times 2^0$$
$$= 1 \times 8+0 \times 4+1 \times 2+0 \times 1$$
$$=10$$

3.3. Basic DAC Techniques

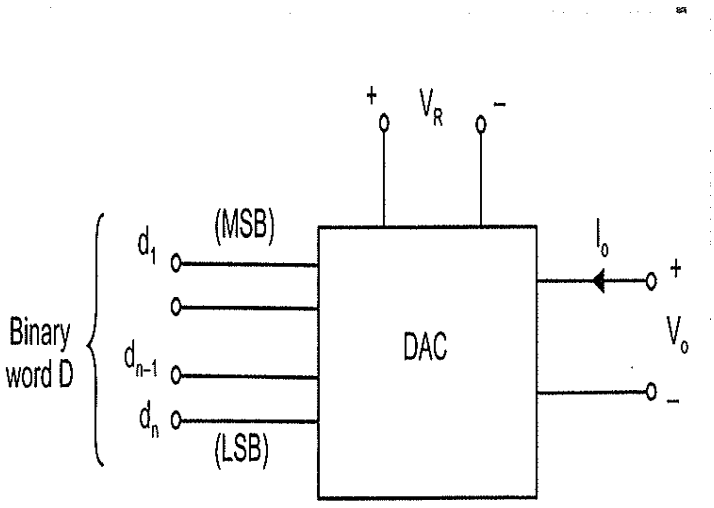


Figure 3.3.1: Block Diagram of DAC

- **The input is a n-bit binary word and is combined with a reference voltage VR to give an analog output signal.**
- **The output of DAC can be either a voltage or current**
- **For a voltage output DAC, the mathematical representation of output is given as,**

$$V_0 = K\,V_{FS}\,(d_1 2^{-1} + d_2 2^{-2} + \ldots + d_n 2^{-n}) \qquad (1$$

where, V_0 = output voltage

V_{FS} = full scale output voltage

K = scaling factor usually adjusted to unity

$d_1 d_2 \ldots d_n$ = n-bit binary fractional word with the decimal point located at the left

d_1 = most significant bit (MSB) with a weight of $V_{FS}/2$

d_n = least significant bit (LSB) with a weight of $V_{FS}/2^n$

3.3 : Types of DAC

- **1. Weighted Resistor DAC**
- **2. R-2R Ladder DAC**

3.3.1 Weighted Resistor DAC

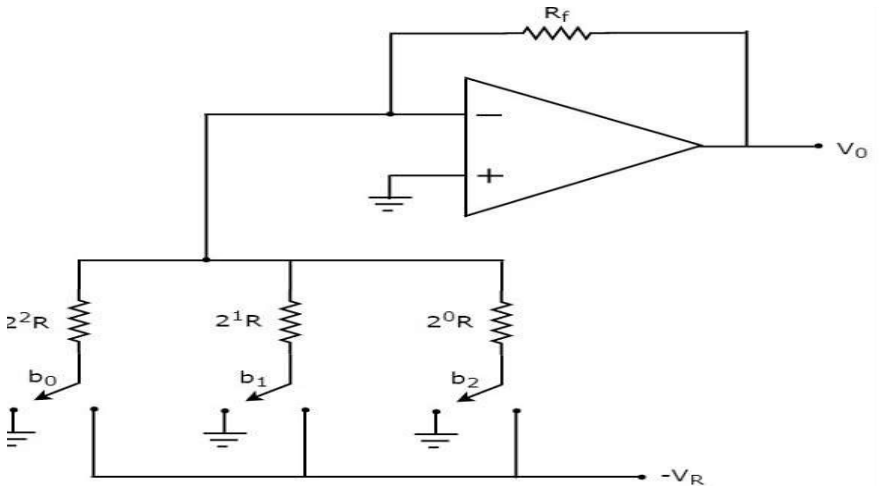


Figure 3.3.1:Binary Weighted DAC

The **nodal equation** at the inverting input terminal's node is:

$$\frac{0+V_R b_2}{2^0 R}+\frac{0+V_R b_1}{2^1 R}+\frac{0+V_R b_0}{2^2 R}+\frac{0-V_0}{R_f}=0$$

$$=>\frac{V_0}{R_f}=\frac{V_R b_2}{2^0 R}+\frac{V_R b_1}{2^1 R}+\frac{V_R b_0}{2^2 R}$$

$$=> V_0=\frac{V_R R_f}{R}\left\{\frac{b_2}{2^0}+\frac{b_1}{2^1}+\frac{b_0}{2^2}\right\}$$

Substituting, $R=2R_f$ f in above equation.

$$=> V_0=\frac{V_R R_f}{2R_f}\left\{\frac{b_2}{2^0}+\frac{b_1}{2^1}+\frac{b_0}{2^2}\right\}$$

Substituting, $R=2R_f$ f in above equation.

$$=> V_0=\frac{V_R R_f}{2R_f}\left\{\frac{b_2}{2^0}+\frac{b_1}{2^1}+\frac{b_0}{2^2}\right\}$$

$$=> V_0=\frac{V_R}{2}\left\{\frac{b_2}{2^0}+\frac{b_1}{2^1}+\frac{b_0}{2^2}\right\}$$

We can write the **generalized output voltage equation** of an N-bit binary weighted resistor DAC as shown below based on the output voltage equation of a 3-bit binary weighted resistor DAC.

$$=> V_0=\frac{V_R}{2}\left\{\frac{b_{N-1}}{2^0}+\frac{b_{N-2}}{2^1}+\ldots+\frac{b_0}{2^{N-1}}\right\}$$

DRAWBACK OF BINARY WEIGHTED DAC

- **The difference between the resistance values corresponding to LSB & MSB will increase as the number of bits present in the digital input increases.**
- **It is difficult to design more accurate resistors as the number of bits present in the digital input increases.**
- **Has problems if bit length is longer than 8 bits For example, if R = 10 k Ohms**

$R_8 = 2^{8-1}$(10 k Ohms) = 1280 k Ohms If V_R = 10 Volts,

I_8 = 10V/1280 k Ohms = 7.8 A

- **Op-amps to handle those currents are expensive because this is usually below the current noise threshold.**

3.3.2 : R-2R ladder Network

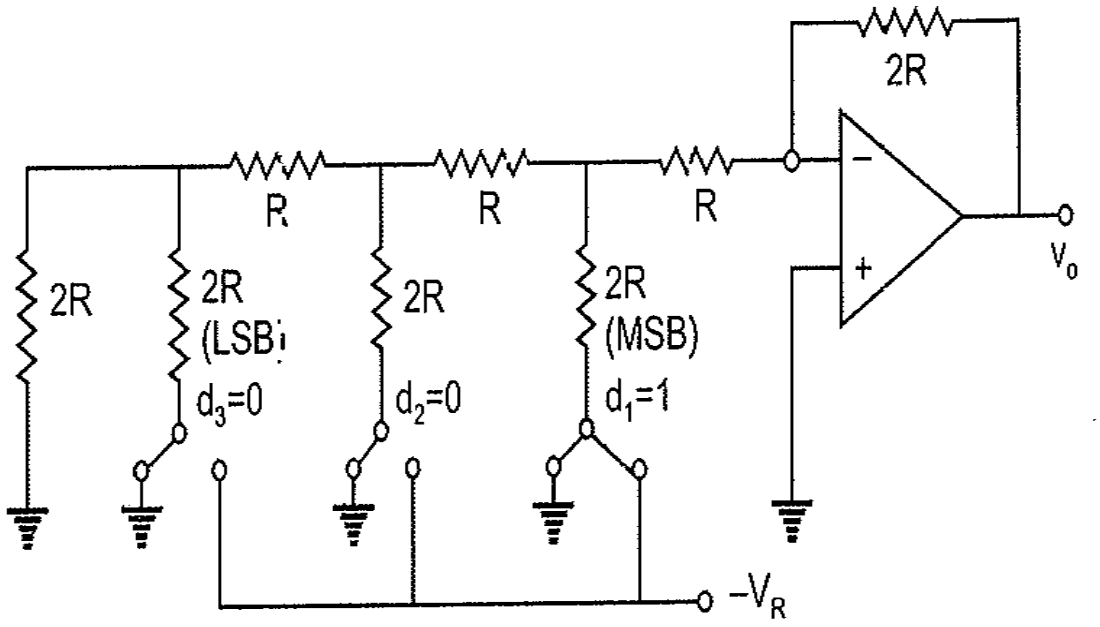
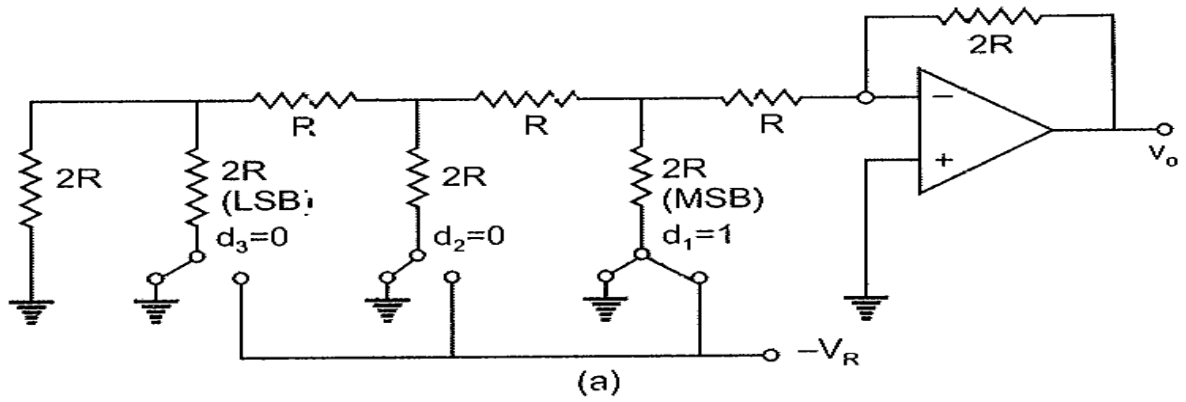


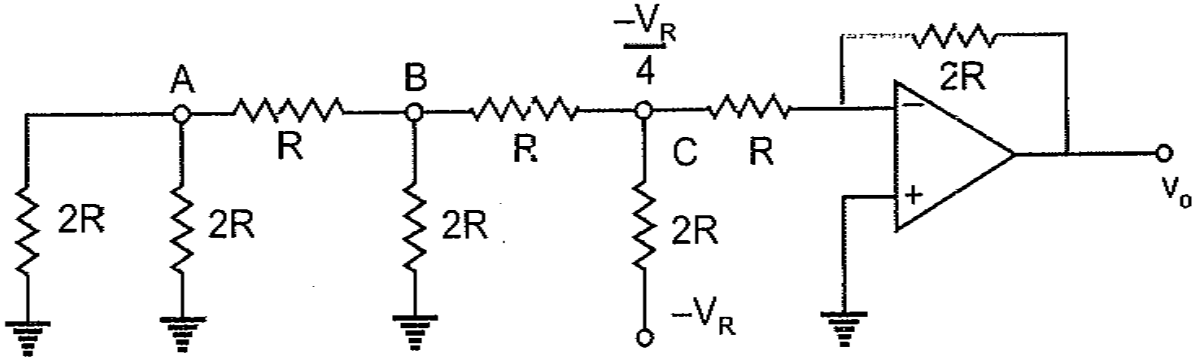
Figure 3.3.2: R-2R Ladder Network

- **The R-2R Digital to Analog Converter uses only two resistance values R and 2R regardless of the number of bits of the converter compared to the weighted resistor implementation where each bit resistor has a different value. The circuit shown is a 3 bit DAC. Typical value of resistors ranges from 2.5kΩ to 10kΩ**

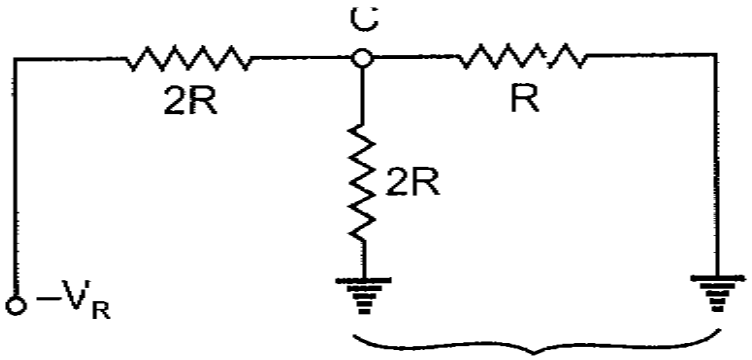


(a)

Consider a 3-bit DAC. where the switch position d1d2d3 corresponds to the binary word 100. The circuit can be simplified to the equivalent form



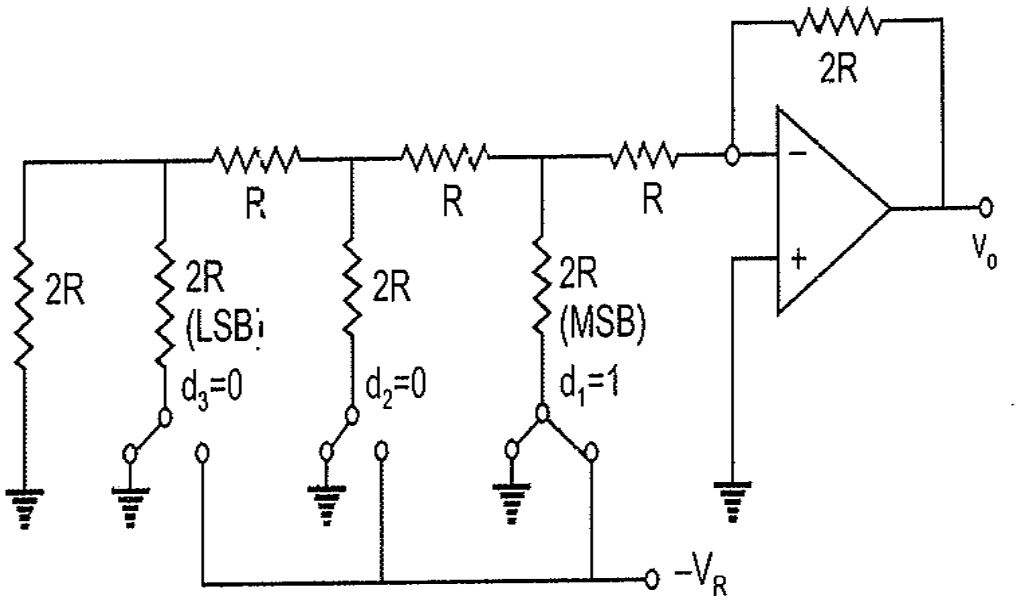
(b)



(c) $\frac{2}{3}R$

The voltage at node C can be given as,

$$\frac{-V_R\left(\frac{2}{3}R\right)}{2R+\frac{2}{3}R} = -\frac{V_R}{4}$$

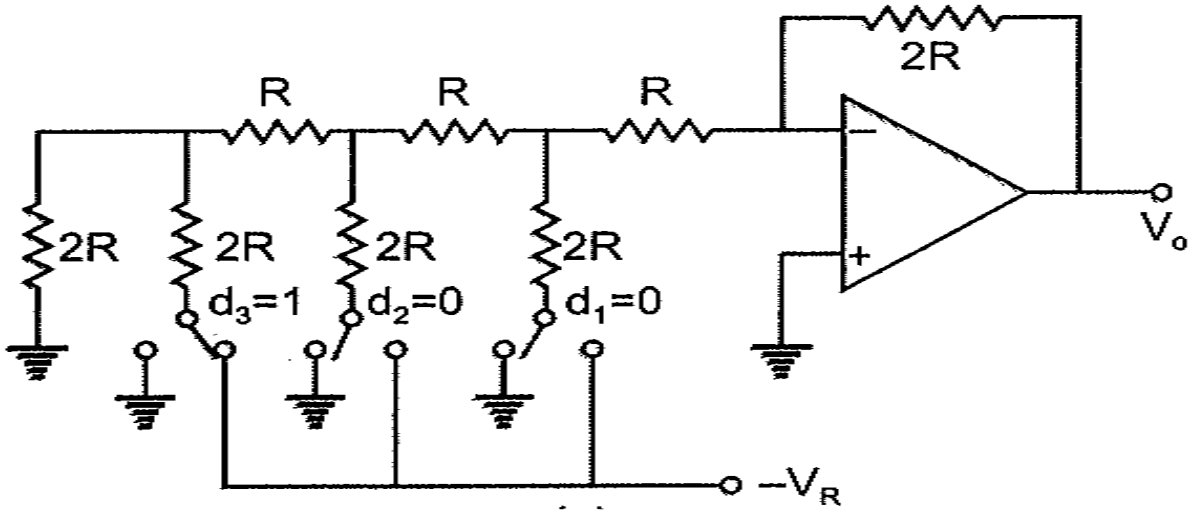


The output voltage is given as,

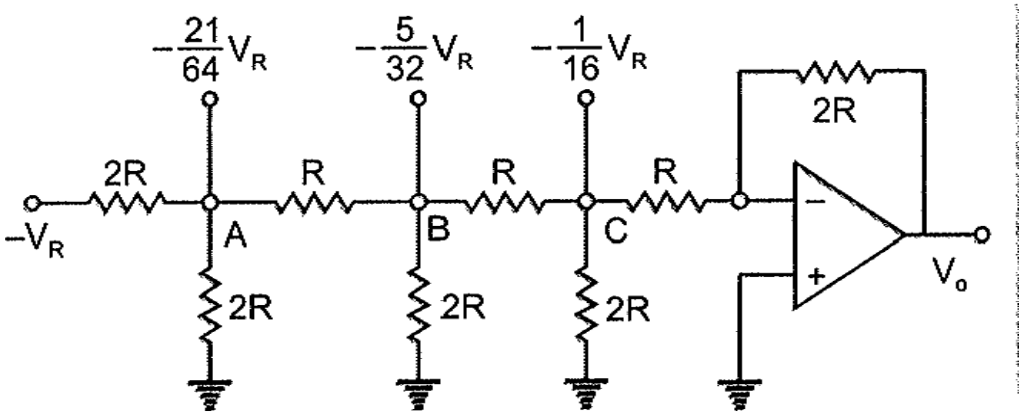
$$V_o = \frac{-2R}{R}\left(-\frac{V_R}{4}\right) = \frac{V_R}{2} = \frac{V_{FS}}{2}$$

PROBLEM:

1. **Calculate the Analog value for the binary digit 001**



The switch position corresponding to the binary word 001 in 3bit DAC is shown. The voltages at the nodes A, BC formed by the resistor branches are easily calculated in a similar fashion



The output voltage is given as,

$$V_0 = \left(-\frac{2R}{R}\right)\left(-\frac{V_R}{16}\right) = \frac{V_R}{8} = \frac{V_{FS}}{8}$$

2. **. The basic step of a 9-bit DAC is 10.3mV.If 0000000 represents 0V. What output is produced if the input is 101101111?**

Solution

The output voltage for input 101101111 is

$= 10.3\ mV\ (1 \times 2^8 + 0 \times 2^7 + 1 \times 2^6 + 1 \times 2^5 + 0 \times 2^4 + 1 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 + 1 \times 2^0)$

$= 10.3\ mV\ (367) = 3.78\ V$

3. What output voltage would be produced by a D/A converter whose output range is 0 to 10V and whose input binary Number is

(i) 10 (for a 2-bit D/A Converter

(ii) 0110 (for a 4-bit DAC)

(iii) 10111100 (For a 8-bit DAC)

Solution

(i) $V_o = 10\text{ V}\left(1 \times \frac{1}{2} + 0 \times \frac{1}{4}\right) = 5\text{ V}$

(ii) $V_o = 10\text{ V}\left(0 \times \frac{1}{2} + 1 \times \frac{1}{2^2} + 1 \times \frac{1}{2^3} + 0 \times \frac{1}{2^4}\right)$

$= 10\left(\frac{1}{4} + \frac{1}{8}\right) = 3.75\text{ V}$

(iii) $V_o = 10\text{ V}\,(1 \times 1/2 + 0 \times 1/2^2 + 1 \times 1/2^3 + 1 \times 1/2^4 + 1 \times 1/2^5 + 1 \times 1/2^6 + 0 \times 1/2^7 + 0 \times 1/2^8)$

$= 10\text{ V}\,(1/2 + 1/8 + 1/16 + 1/32 + 1/64) = 7.34\text{ V}$

- **4. Calculate the values of the LSB,MSB and full scale output for an 8-bit DAC for the 0-10V range**

Solution

$$\text{LSB} = \frac{1}{2^8} = \frac{1}{256}$$

For 10 V range, $\text{LSB} = \frac{10\text{ V}}{256} = 39\text{ mV}$

and $\text{MSB} = \left(\frac{1}{2}\right)\text{ full scale} = 5\text{ V}$

Full scale output = (Full scale voltage − 1 LSB)

$= 10\text{ V} - 0.039\text{ V} = 9.961\text{ V}$

3.4 A-D Converters:

It accepts analog voltage Va, and produces output binary word d1d2….dn of functional value D

$$D = d_1 2^{-1} + d_2 2^{-2} + \ldots + d_n 2^{-n}$$

Where d1 is MSB dn is LSB

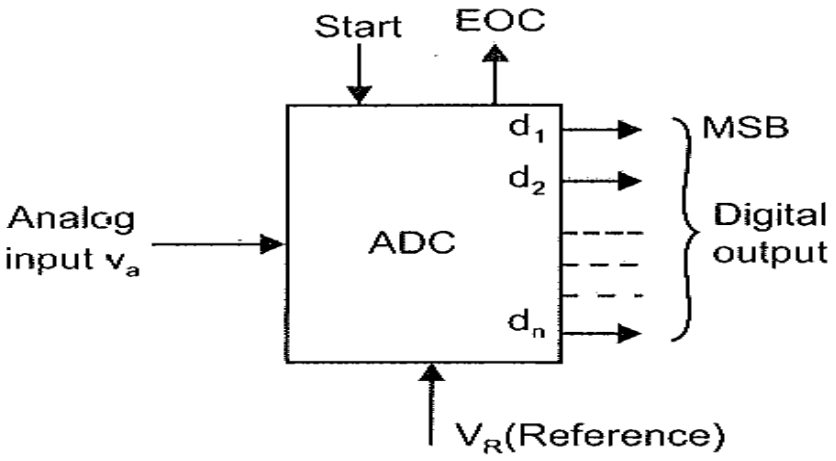


Figure 3.4.1: Analog to Digital converter

An ADC has two additional control lines,

START input tell the ADC when to start the conversion

EOC (End of Conversion) to announce when the conversion is completed

ADCs are designed for microprocessor interfacing or to directly Drive LCD or LED displays.

Classification of ADC

- **Direct Type ADC**
- **Integrating Type ADC**

DIRECT TYPE OF ADC:

It compare a given analog signal with the internally generated equivalent signal. This group include

1. **Flash Type converter**
2. **Successive approximation type converter**

INTEGRATED TYPE ADC:

It performs conversion in an indirect manner by first changing the analog input signal to a linear function of time or frequency and then to a digital code. The two most widely used integrating type converters are

1. **Charge balancing ADC**
2. **Dual slope ADC**

3.4.1 Parallel Comparator(Flash) A/D Converter

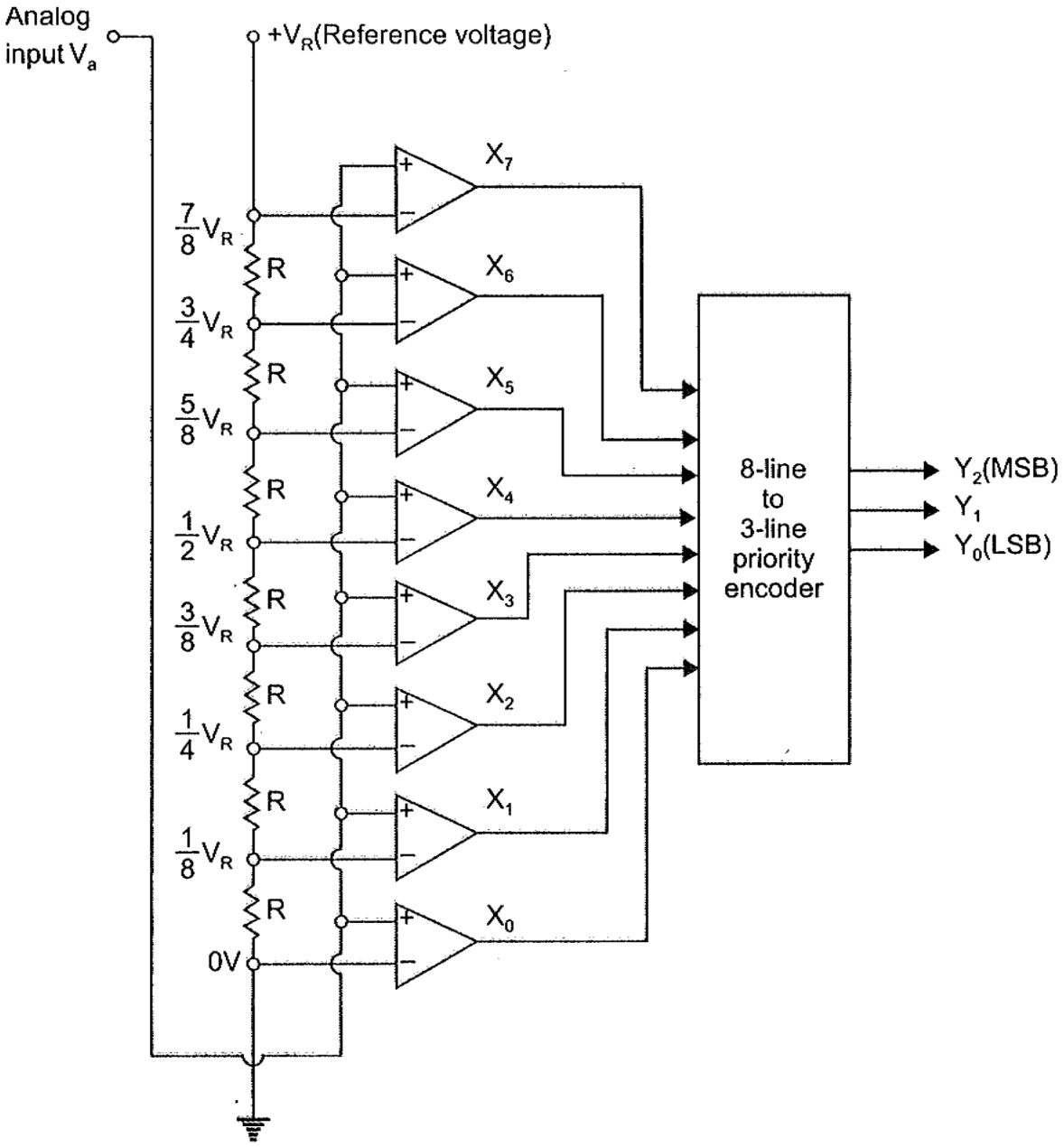


Figure: 3.4.1: Flash Type Converter

- **It is the simplest possible A/D converter**
- **It is at the same time , the fastest and most expensive technique.**
- **The circuit consist of a resistive divider network, 8 op-amp comparator and a 8 line to 3-line encoder.**
- **At each node of the resistive divider, a comparison voltage is available.**
- **Since all the resistors are of equal value, the voltage levels available at the nodes are equally divided between the reference voltage VR and the ground.**
- **The purpose of the circuit is to compare the analog input voltage Va with each of the node voltage.**
- **The circuit has an advantage of high speed, because the conversion take place simultaneously rather than sequentially.**
- **Typical conversion time is 100ns or less.**
- **Conversion time is limited only by the speed of the comparatorand of the priority encoder.**
- **By using an advanced Micro Devices AMD 686A Comparator and a T1147 priority encoder , conversion delays of the order of 20 ns can be obtained.**

Voltage input	Logic output X
$V_a > V_d$	$X = 1$
$V_a < V_d$	$X = 0$
$V_a = V_d$	Previous value

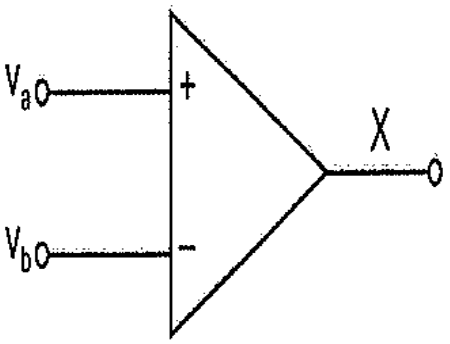


Figure 3.4.2: Comparator truth table

Input voltage V_a	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	Y_2	Y_1	Y_0
0 to $V_R/8$	0	0	0	0	0	0	0	1	0	0	0
$V_R/8$ to $V_R/4$	0	0	0	0	0	0	1	1	0	0	1
$V_R/4$ to 3 $V_R/8$	0	0	0	0	0	1	1	1	0	1	0
3 $V_R/8$ to $V_R/2$	0	0	0	0	1	1	1	1	0	1	1
$V_R/2$ to 5 $V_R/8$	0	0	0	1	1	1	1	1	1	0	0
5 $V_R/8$ to 3 $V_R/4$	0	0	1	1	1	1	1	1	1	0	1
3 $V_R/4$ to 7 $V_R/8$	0	1	1	1	1	1	1	1	1	1	0
7 $V_R/8$ to V_R	1	1	1	1	1	1	1	1	1	1	1

Fig. 3.5.3 Truth table for a flash type A/D converter

Disadvantages of Flash Type converter:

The number of comparators required almost doubles for each added bit . A 2 bit ADC requires 3 comparator, 3- bit ADC needs 7, whereas 4-bit requires 15 comparators. In general, the number of comparator requires are

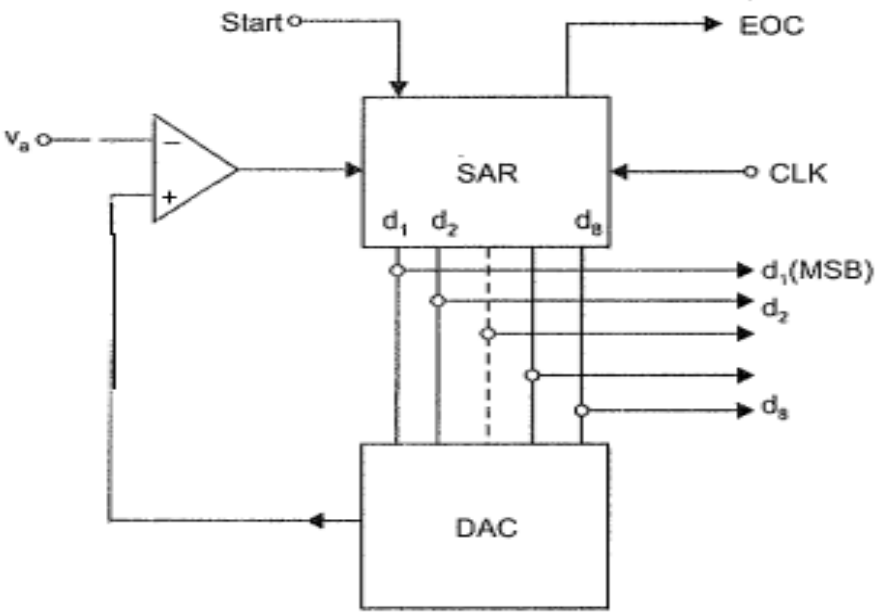
$$2^n - 1$$

Where n is the desired number of bits.

Hence the number of comparators approximately doubles for added bits.

Also the larger the value of n, the more complex is the priority encoder.

3.4.2: SUCESSIVE APPROXIMATION ADC:



Functional diagram of the successive approximation ADC

Figure 3.4.2: Block diagram of Successive Approximation Technique

This method uses a successive approximation register (SAR) to find the required values of each bit by trial and error.

With the arrival of the START command , the SAR sets the MSB d1= 1 with all other bits to zero so that the trial code is 1000000.

The output Vd of the DAC is now compared with analog input Va. If Va is greater than the DAC output Vd then 1000000 is less than the correct digital representation.

The MSB is left at 1 and the net lower significant bit is made 1 and further tested

However , if Va is less than the DAC output, then 1000000 is greater than the correct digital representation.

So reset MSB to '0' and go on to the next lower significant bit as 1,

This procedure is repeated for all subsequent bits, one at a time , until all bit positions have been tested.

Whenever the DAC output crosses Va, the comparator changes state and this can be taken as End of conversion(EOC).

Correct digital representation	*Successive approximation register output V_d at different stages in conversion*	*Comparator output*
11010100	10000000	1 (initial output)
	11000000	1
	11100000	0
	11010000	1
	11011000	0
	11010100	1
	11010110	0
	11010101	0
	11010100	

Fig. 3.5.2 Successive approximation conversion sequence for a typical analog input

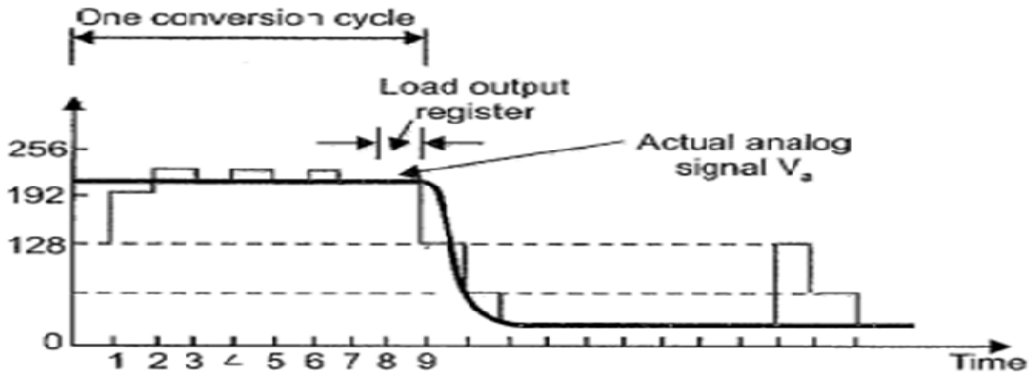


Fig. 3.5.3 The D/A output voltage is seen to become successively closer to the actual analog input voltage

3.5 : INTEGRATING TYPE ADC

The integrating type of ADC do not reqire S/H circuit at the input.If the inpt changes during conversion, the ADC output code will be proportional to the value of the input averaged over the integration period.

- ✓ **Charge Balancing ADC**
- ✓ **Dual slope ADC**

3.5.1 : DUAL SLOPE ADC

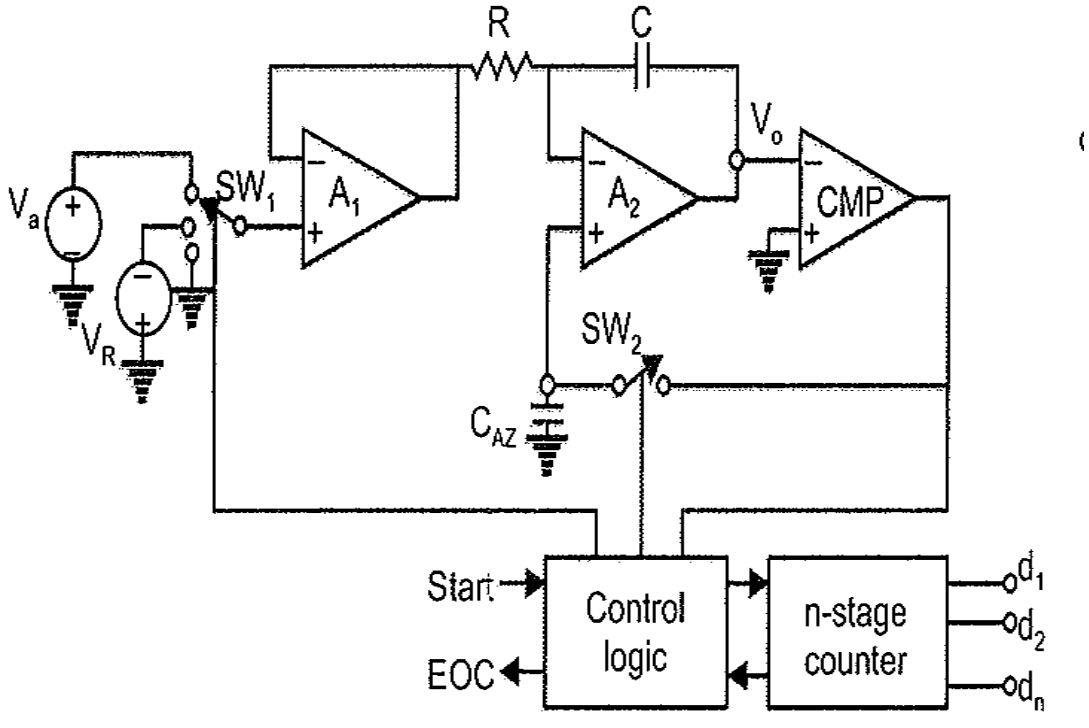


Figure 3.5.1: Dual Slope ADC

The circuit consists of a high input impedance bufferA1, precision integratorA2 and a voltage comparator. The converter first integrates the analog input signal Va for a fixed duration of 2^n clock periods as shown in figure. Then it integrates an internal reference voltage VR of opposite polarity until the integrator output is zero. The number of clock cycles required to return the integrator to zero is proportional to the value of Va averaged over the integration period. Hence N represents the desired output code.

Before the START command arrives, the switch SW_1 is connected to ground and SW_2 is closed. Any offset voltage present in the A_1, A_2, comparator loop after integration, appears across the capacitor C_{AZ} till the threshold of the comparator is achieved. The capacitor C_{AZ} thus provides automatic compensation for the input-offset voltages of all the three amplifiers. Later, when SW_2 opens, C_{AZ} acts as a memory to hold the voltage required to keep the offset nulled. At the arrival of the START command at $t = t_1$, the control logic opens SW_2 and connects SW_1 to V_a and enables the counter starting from zero. The circuit uses an n-stage ripple counter and therefore the counter resets to zero after counting 2^n pulses. The analog voltage V_a is integrated for a fixed number 2^n counts of clock pulses after which the counter resets to zero. If the clock period is T, the integration takes place for a time $T_1 = 2^n \times T$ and the output is a ramp going downwards

The counter resets itself to zero at the end of the interval T_1 and the switch SW_1 is connected to the reference voltage $(-V_R)$. The output voltage v_0 will now have a positive slope. As long as v_0 is negative, the output of the comparator is positive and the control logic allows the clock pulse to be counted. However, when v_0 becomes just zero at time $t = t_3$, the control logic issues an end of conversion (EOC) command and no further clock pulses enter the counter. It can be shown that the reading of the counter at t_3 is proportional to the analog input voltage V_a.

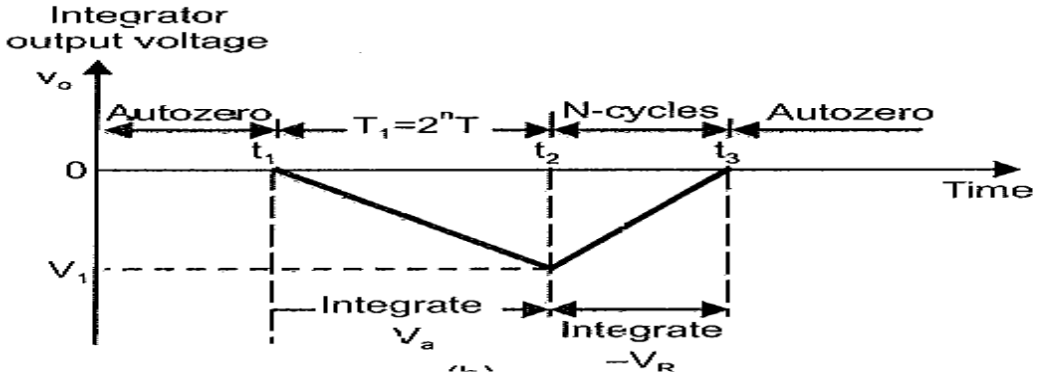


Figure 3.5.2 : Output Waveform

$$T_1 = t_2 - t_1 = \frac{2^n \text{ counts}}{\text{clock rate}}$$

$$t_3 - t_2 = \frac{\text{digital count } N}{\text{clock rate}}$$

For an integrator,

$$\Delta v_0 = (-1/RC)\, V(\Delta t)$$

The voltage v_0 will be equal to v_1 at the instant t_2 and can be written as

$$v_1 = (-1/RC)\, V_a(t_2 - t_1)$$

The voltage v_1 is also given by

$$v_1 = (-1/RC)\, (-V_R)\, (t_2 - t_3)$$

So, $$V_a(t_2 - t_1) = V_R(t_3 - t_2)$$

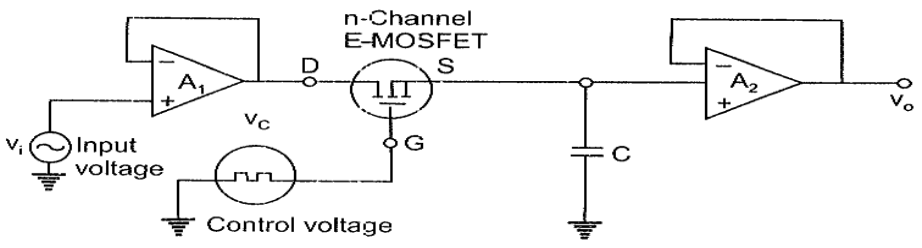
Putting the values of $(t_2 - t_1) = 2^n$ and $(t_3 - t_2) = N$, we get

$$V_a(2^n) = (V_R)N$$

or, $$V_a = (V_R)\, (N/2^n)$$

3.6 SAMPLE AND HOLD CIRCUIT:

A sample and hold circuit samples an input and holds on to its last sampled value until the input is sampled again.This type of circuit is very useful in digital interfacing, analog to digital conversion and pulse code modulation systems.One of the simplest practical sample and hold circuit is given here.The n-channel E-MOSFET works as a switch and is controlled by the control voltage Vc and the capacitor C stores the charge. The analog signal Vi to be sampled is applied to the drain of E-MOSFET and the control voltage Vc is applied to its gate.When Vc is



positive , the E-MOSFET turns on and the capacitor C charges to the instantaneous value of the input Vi with a time constant [R0+rDS]C.

Figure 3.6.1: Sample and Hold Circuit

Thus the input voltage Vi appears across, the capacitor C and then at the output through the voltage follower A2.The waveforms are shown in figureDuring the time when control voltage Vc is zero, the E-MOSFET is off. The capacitor C is now facing the high input impedance of the voltage follower A2 and hence cannot discharge.The capacitor holds the voltage across it. The time period Ts, the time during which voltage across the capacitor is equal to input voltage is called sample period.The time period TH of Vc during which the voltage across the capacitor is held constant is called hold period. The frequency of the control voltage should be kept higher than the input so as to retrieve the input from output waveform.

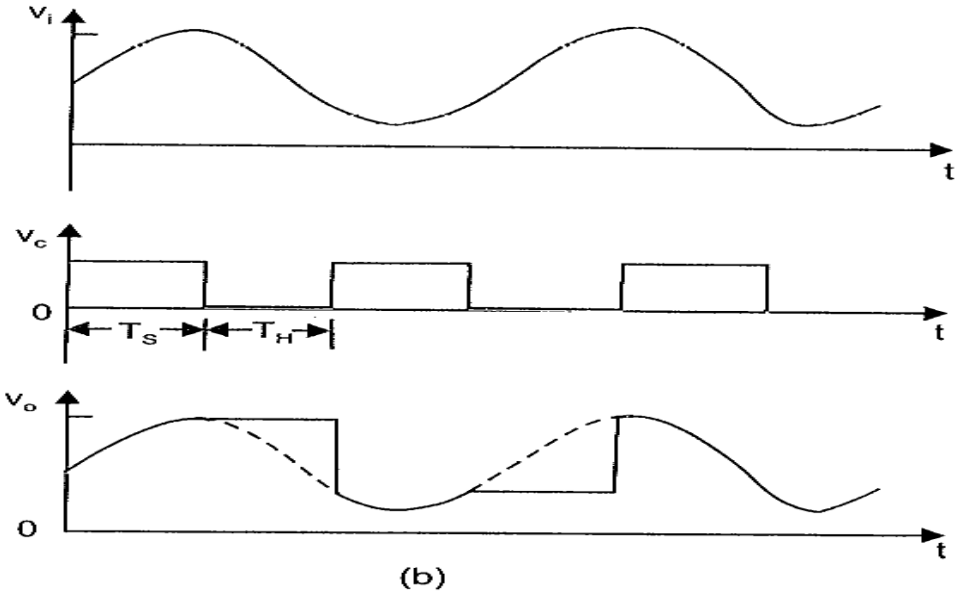


Figure 3.6.1: Waveforms of Sample and Hold Circuit

3.7 : DAC/ADC Specifications:

1.Resolutions

2. Linearity

3. Accuracy

4. Monotonicity

5. Settling Time

6. Stability

(i).RESOLUTION:

The resolution of a converter is the smallest change in voltage which may be produced at the output of the converter. For example, an 8-bit D/A converter has 2^8-1 = 255 equal intervals.Hence the smallest change in output voltage is (1/255) of the full scale output range. In short , the resolution is the vale of the LSB.

$$\text{Resolution (in volts)} = \frac{V_{FS}}{2^n - 1} = 1 \text{ LSB increment}$$

Resolution is stated in a number of different ways. An 8-bit DAC is said to have

- **8 bit resolution**
- **a resolution of 0.392 of full scale**
- **a resolution of 1 part in 255**

Similarly, the resolution of an A/D converter is defined as the smallest change in analog input for a one bit change at the output.

As an example the input range of an 8-bit A/D converter is divided into 255 intervals. So the resolution for a 10V input range is 39.2mV (=10V/255)

(ii) LINEARITY

The linearity of an A/D or D/A converter is an important measure of its accuracy and tells us how close the converter output is to its ideal transfer characteristics.In an ideal DAC, equal increment in the digital input should produce equal increment in the analog output and the transfer curve should be linear.

However, in an actual DAC, output voltage do not fall on a straight line because of gain and offset errors as shown by the solid line curve.The static performance of a DAC is determined by fitting a straight line through the measured output points The linearity error measures the deviation of the actual output from the fitted line and is given by

$$\varepsilon/\Delta$$

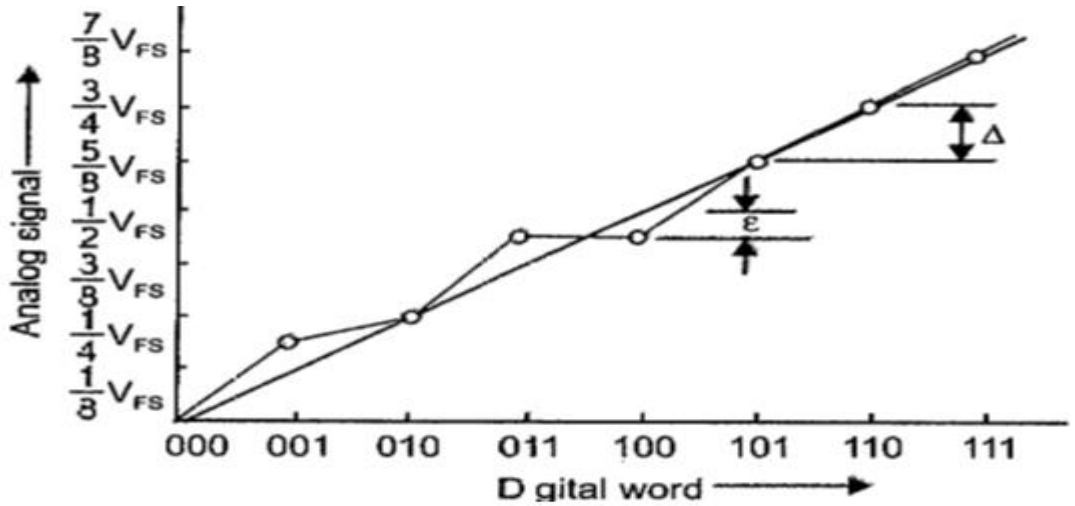


Figure 3.7.1: Linearity Error

(iii). ACCURACY:

Absolute accuracy is the maximum deviation between the actual converter output and the ideal converter output. Relative Accuracy is the maximum deviation after gain and offset errors have been removed. Data sheets normally specify relative accuracy rather than absolute accuracy.

The accuracy of a converter is also specified in terms of LSB increments or percentage of full scale voltage.

(iv). MONOTONICITY :

A monotonic DAC is the one whose analog output increases for an increase in digital input.The figure represents the transfer curve for a non-monotonic DAC, since the output decreases when input code changes from 001 to 010.A monotonic characteristic is essential in control applications, otherwise oscillations can results.In successive approximation ADCs, a non-monotonic characteristic may lead to missing codes .If a DAC has to be monotonic, the error should be less than

(1/2)LSB

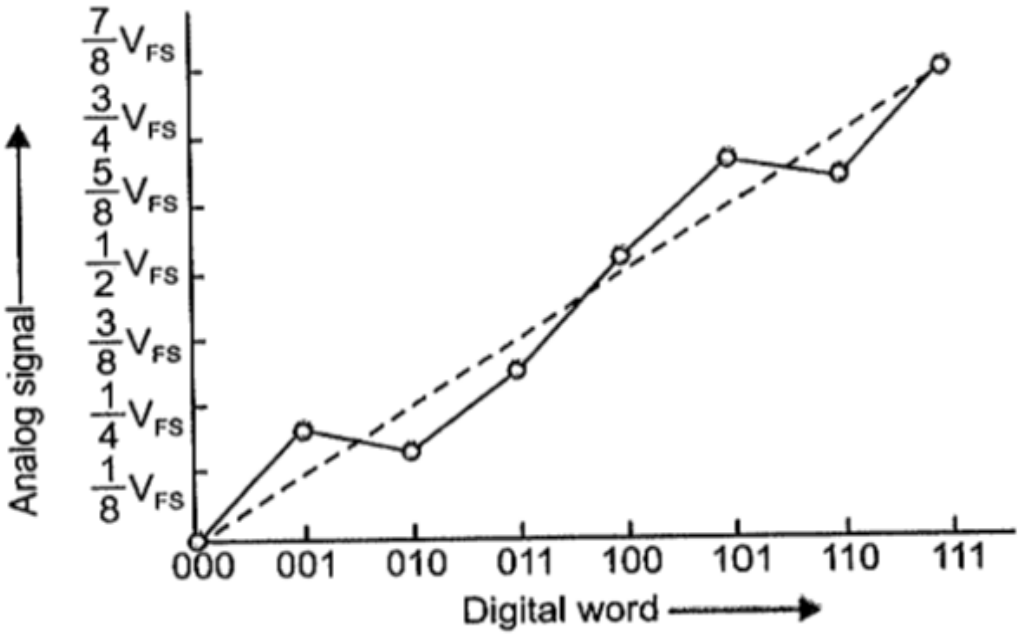


Figure 5.7.2: Monotonicity Error

(v). SETTLING TIME:

The most important dynamic parameter is the settling time. It represents the time it takes for the output to settle within a specified band (1/2) LSB of its final value following a code change at the input (usually a full scale change).It depends upon the switching time of the logic circuitry due to internal parasitic capacitances and inductances. Settling time ranges from 100ns to 10ns depending on word length and type of circuit used.

(vi). STABILITY:

The performance of converter changes with temperature, age and power supply variations.So all the relevant parameters such as offset , gain, linearity error and monotonicity must be specified over the full temperature and power supply ranges.

Text Book References:

1. Ramakant A.Gayakwad, "0P-AMP and Linear ICs", 4th Edition, Prentice Hall / Pearson Education, 1994.

2. D.Roy Choudary, Shail Jain, "Linear Integrated Circuits", New Age International Pvt. Ltd., 2000.

3. Grey and Meyer, "Analysis and Design of Analog Integrated Circuits, 4th Edition, Wiley International, 2001.

4. Michael Jacob, "Applications and Design with Analog Integrated Circuits, 2nd Edition, Prentice Hall of India, 1993.

5. S. Salivahanan, V.S. Kanchana Bhaaskaran, "Linear integrated circuits", 3rd Edition, McGraw-Hill, 2011.

6. William D.StanelY, "Operational Amplifiers with Linear Integrated Circuits", 4th Edition, Pearson Education, 2004.

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PLL AND TIMER CIRCUITS

UNIT 4

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UNIT 4 PLL AND TIMER CIRCUITS 9 Hrs.

Phase Locked Loop IC 565- Block schematic - Applications of PLL: FM demodulator and Frequency synthesizer-FSK Demodulator-VCO IC LM566-Timer IC LM555 and its applications: Astable and Monostable multivibrator.

4.1 Phase Locked Loop (PLL)

The phase-locked loop (PLL) is an important building block of linear systems. Electronic phase- locked loop (PLL) came into vogue in the 1930 when it was used for radar synchronization and communication applications. Now with the advanced IC technology, PLLs are available as inexpensive monolithic lCs. This technique for electronic frequency control is used today in satellite communication systems, air borne navigational systems, FM communication systems, computers etc. The basic principle of PLL, different lCs and important applications are discussed.

Basic Principles

The basic block schematic of the PLL is shown in Fig. 4.1.1. This feedback system consists of Phase detector/comparator, low pass filter, error amplifier and Voltage Controlled Oscillator (VCO).

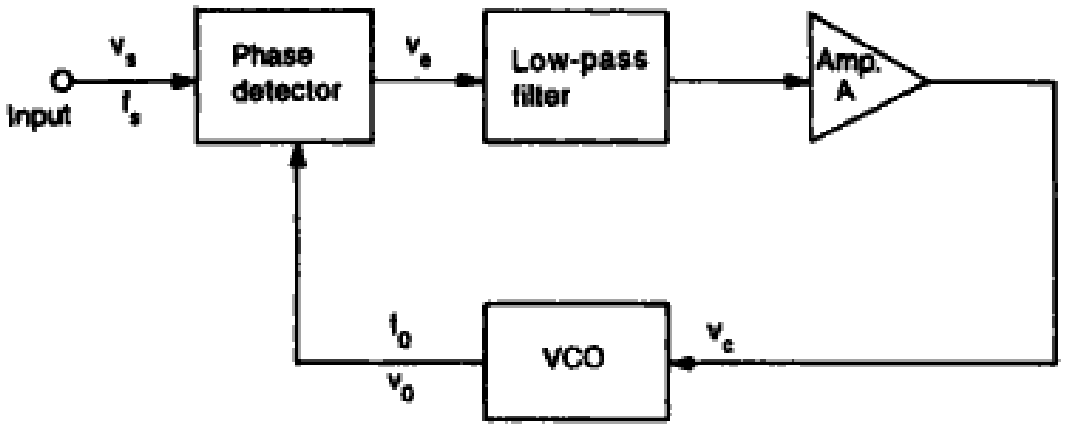


Fig. 4.1.1 Block schematic of the PLL

The VCO is a free running multivibrator and operates at a set frequency f_o called free running frequency. This frequency is determined by an external timing capacitor and an external resistor. It can also be shifted to either side by applying a dc control voltage v_C to an appropriate terminal of the IC. The frequency

deviation is directly proportional to the dc control voltage and hence it is called a "Voltage Controlled Oscillator" or, in short, VCO. If input signal v_S of frequency f_S is applied to the PLL, the phase detector compares the phase and frequency of the incoming signal to that of the output v_O of the VCO. If the two signals differ in frequency and /or phase, an error voltage v_e is generated.

The phase detector is basically a multiplier and produces the sum (f_S+f_O) and difference ($f_S- f_O$) components at its output. The high frequency component (f_S+f_O) is removed by the low pass filter and the difference frequency component is amplified and then applied as control voltage v_C to VCO. The signal v_C shifts the VCO frequency in a direction to reduce the frequency difference between f_S and f_O.

Once this action starts, we say that the signal is in the capture range. The VCO continues to change frequency till its output frequency is exactly the same as the input signal frequency. The circuit is then said to be locked. Once locked, the output frequency f_O of VCO is identical to f_S except for a finite phase difference ϕ. This phase difference ϕ generates a corrective control voltage v_C to shift the VCO frequency from f_O to f_S and thereby maintain the lock. Once locked, PLL tracks the frequency changes of the input signal.

Thus, a PLL goes through three stages (i) free running (ii) capture and (iii) locked or tracking.

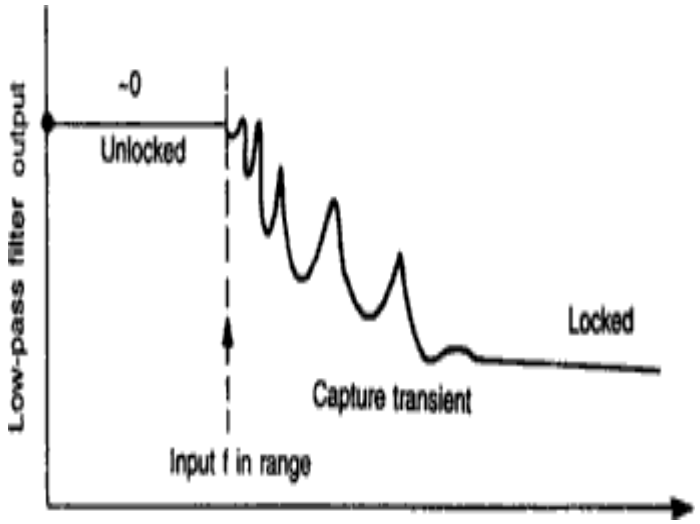


Fig. 4.1.2. The capture transient

Figure 4.1.2 shows the capture transient. As capture starts, a small sine wave appears. This is due to the difference frequency between the VCO and the input signal. The dc component of the beat drives the VCO towards the lock. Each successive cycle causes the VCO frequency to move closer to the input signal frequency. The difference in frequency becomes smaller and a large de component is passed by the filter, shifting the VCO frequency further. The process continues until the VCO locks on to the signal and the difference frequency is dc.

The low pass filter controls the capture range. If VCO frequency is far away, the beat frequencywillbe too high to pass through the filter and the PLL will not respond. We say that the signal is out of the capture band. However, once locked, the filter no longer restricts the PLL. The VCO can track the signal well beyond the capture band. Thus tracking range is always larger than the capture range.

Lock-in Range

Once the PLL is locked, it can track frequency changes in the incoming signals. The range of frequencies over which the PLL can maintain lock with the incoming signal is called the lock-in range or tracking range. The lock range is usually expressed as a percentage of f_0, the VCO frequency.

Capture Range

The range of frequencies over which the PLL can acquire lock with an input signal is called the capture range. This parameter is also expressed as percentage of f_0.

Pull-in. time

The total time taken by the PLL to establish lock is called pull-in time. This depends on the initial phase and frequency difference between the two signals as well as on the overall loop gain and loop filter characteristics.

4.2. Phase Locked Loop IC565

IC565 is available as a 14 pin DIP package and as 10 pin metal can package. The pin configuration and the block diagram are shown in Fig.4.2.1 (a, b). The output frequency of the VCO (both inputs 2, 3 grounded) is given by

$$f_o = \frac{0.25}{R_T C_T} \text{ Hz}$$

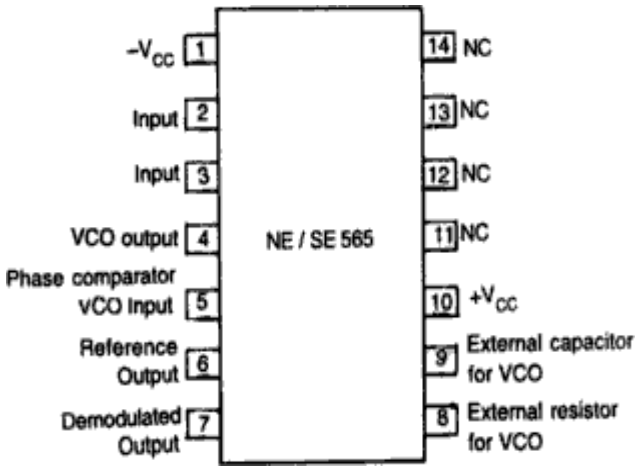


Fig. 4.2.1(a) Pin diagram

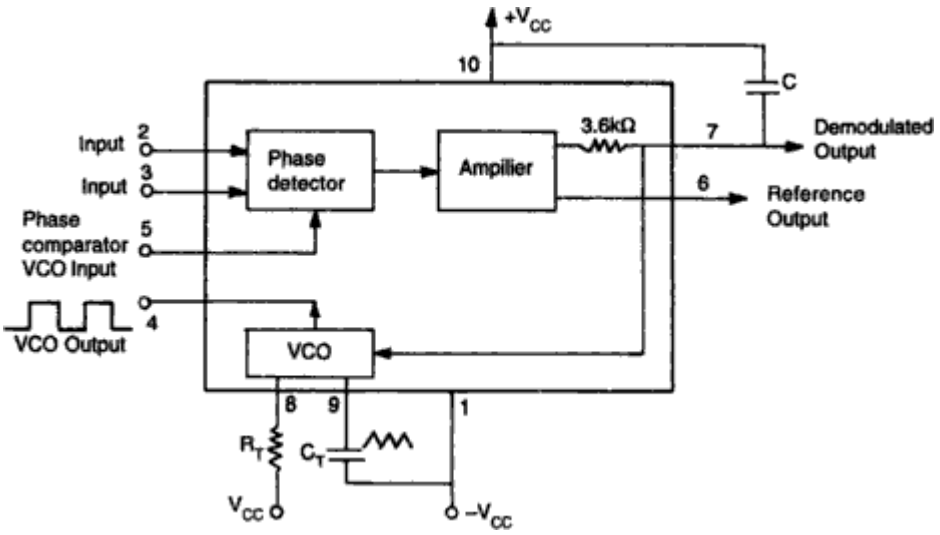


Fig. 4.2.1 (b) NE/SE565 PLL block diagram

Where RT and CT are the external resistor and capacitor connected to pin 8 and pin 9. A value between 2 KΩ and 20 KΩ is recommended for RT. The VCO free running frequency is adjusted with RT and CT to be at the centre of the input frequency range. It may be seen that phase locked loop is internally broken between the VCO output and phase comparator input. A short circuit between pins 4 and 5 connects the VCO output to the phase comparator so as to compare f_o with input signal f_s. A capacitor C is connected between pin 7 and pin 10 (supply terminal) to make a low pass filter with the internal resistance of 3.6 KΩ.

The important electrical parameters of 565 PLL are:

Operating frequency range	:	0.001 Hz to 500 KHz
Operating voltage range	:	±6V to ±12V
Input level	:	10 mV rms min. to 3V pp max.
Input impedance		10 KΩ
Triangle wave amplitude	:	2.4Vpp at ±6V supply voltage
Square wave amplitude	:	5.4Vpp at ±6V supply voltage

4.3 Applications of PLL

The output from a PLL system can be obtained either as the voltage signal *vC(t)* corresponding to the error voltage in the feedback loop or as a frequency signal at VCO output terminal. The voltage output is used in

frequency discriminator application whereas the frequency output is used in signal conditioning frequency synthesis or clock recovery applications.

4.3.1 FM demodulator

The PLL can be very easily used as an FM detector or demodulator. Fig 4.3.1 shows the block diagram of FM detector.

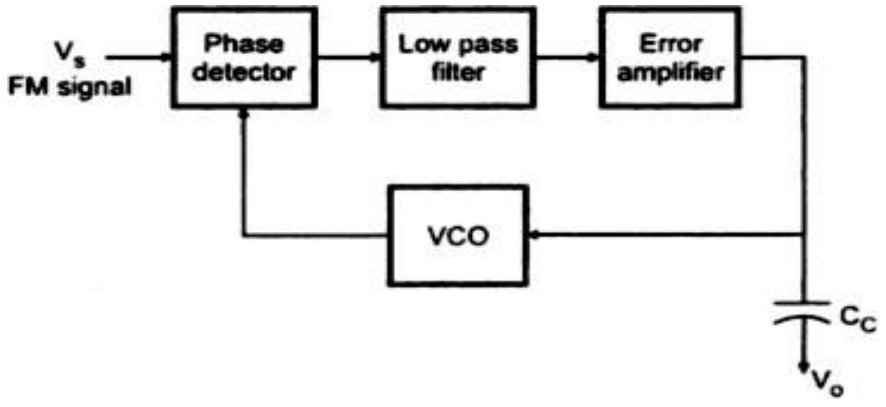


Fig.4.3.1 PLL as a FM Demodulator

When the PLL is locked in on the FM signal the VCO frequency follows the instantaneous frequency of the FM signal and the error voltage or VCO control voltage is proportional to the deviation of the input frequency from center frequency. Therefore the ac component of error voltage or control voltage of VCO will represent a true replica of the modulating voltage that is applied to the FM carrier at the transmitter.

The faithful reproduction of modulating voltage depends on the linearity will represent a true replica of the modulating voltage depends on the linearity between the instantaneous frequency deviation and the control voltage of VCO. It is also important to note that the FM frequency deviation and modulating frequency should remain in the locking range of PLL to get the faithful replica of the modulating signal. If the product of the modulation frequency f_m and the frequency deviation exceeds the $(\Delta f_C)^2$, the VCO will not be able to follow the instantaneous frequency of the FM signal.

4.3.2 Frequency synthesizer

The PLL can be used as the basis for the frequency synthesizer that can produce a precise series of frequencies that are derived from a stable crystal controlled oscillator. Fig. 4.3.2 shows the block diagram of frequency synthesizer. It is similar to frequency multiplier circuit except that divided by M network is added at the input of phase lock loop. The frequency of the crystal-controlled oscillator is divided by an integer factor M by divider network to produce a frequency f_{osc}/M, where f_{osc} is the frequency of the crystal controlled oscillator. The VCO frequency f_{vco} is similarly divided by factor N by divider network to give frequency equal to f_{vco}/N. when the PLL is licked in on the divided-down oscillator frequency we will have $f_{osc}/M = f_{vco}/N$, so that $f_{vco} = f_{osc}N/M$).

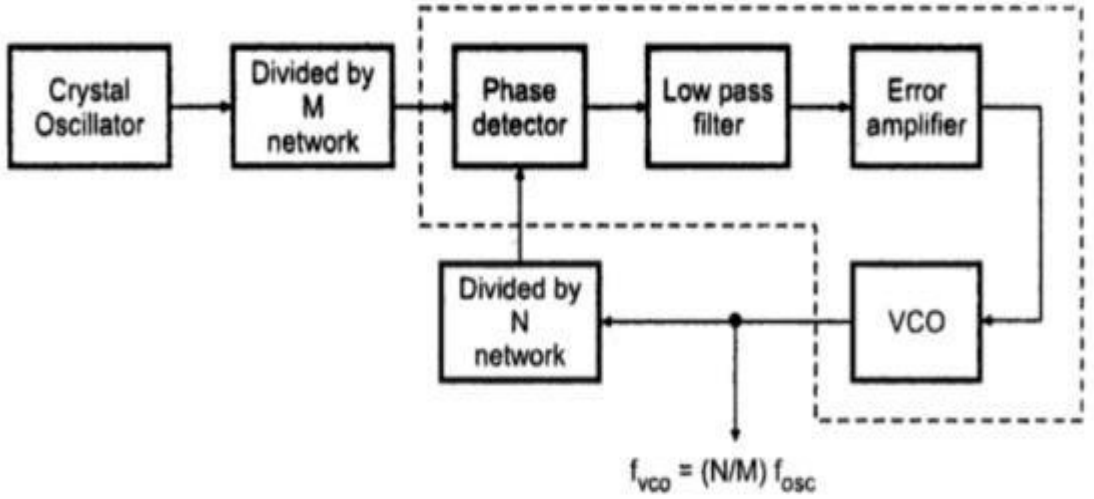


Fig. 4.3.2 Block diagram of Frequency synthesizer

By adjusting divider counts to desired values large number of frequencies can be produced, all derived from the crystal controlled oscillator.

4.4 VCO IC LM 566

A common type of VCO available in IC form is Signetics NE/SE566. The pin configuration and basic block diagram of 566 VCO are shown in Fig. 5.8(a, b). Referring to Fig. 5.8 (b), a timing capacitor C_T is linearly charged or discharged by a constant current source/sink. The amount of current can be controlled by changing the voltage v_c applied at the modulating input (pin 5) or by changing the timing resistor R_T external to IC chip. The voltage at pin 6 is held at the same voltage as pin 5. Thus, if the modulating voltage at pin 5 is increased, the voltage at pin 6 also increases, resulting in less voltage across R_T and thereby decreasing the charging current.

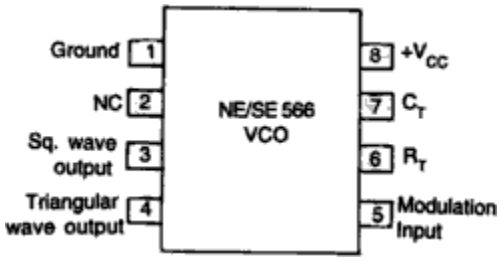


Fig. 4.4.1 Pin configuration of VCO

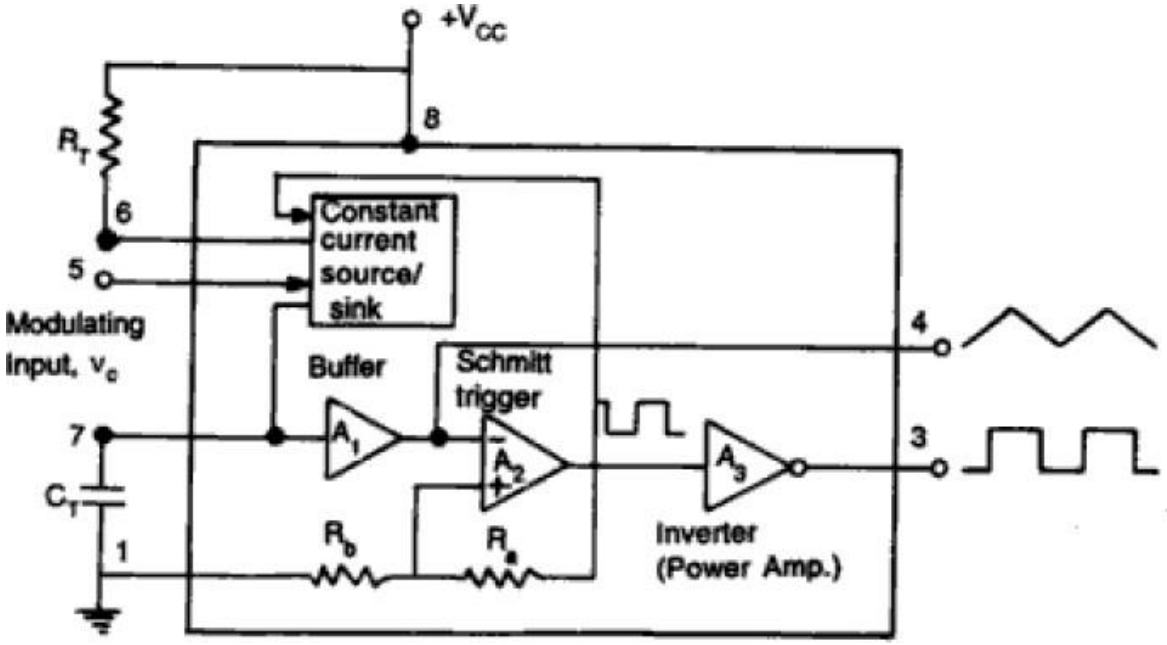


Fig.4.4.2 Block Diagram of VCO

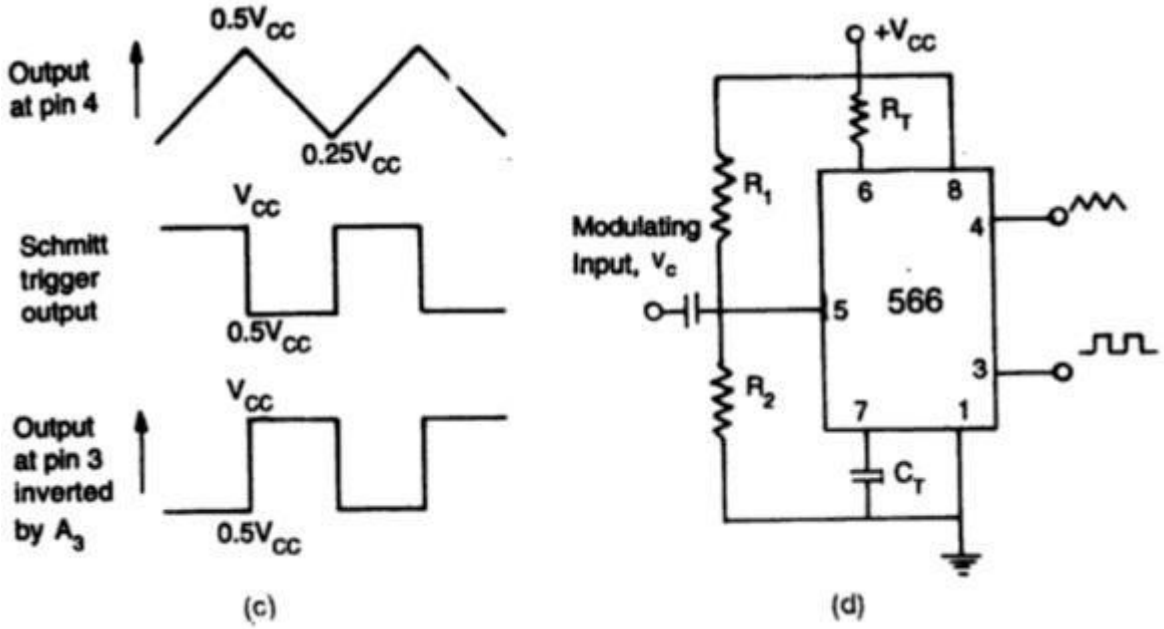


Fig. 4.4.3 Output Waveform (d) Typical connection

The voltage across the capacitor C_T is applied to the inverting input terminal of Schmitt trigger A_2 via buffer amplifier A_1. The output voltage swing of the Schmitt trigger is designed to V_{cc} and 0.5 V_{cc}. If $R_a = R_b$ in the positive feedback loop, the voltage at the non-inverting input terminal of A_2 swings from 0.5 V_{cc} to 0.25 V_{cc}. In Fig. 5.8 (c), when the voltage on the capacitor C_T exceeds 0.5 V_{cc} during charging, the output of the Schmitt trigger goes LOW (0.5 V_{cc}). The capacitor now discharges and when it is at 0.25 V_{cc}, the output of Schmitt trigger goes HIGH (V_{cc}). Since the source and sink currents are equal, capacitor charges and discharges for the same amount of time. This gives a triangular voltage waveform across C_T which is also available at pin 4. The square wave output of the Schmitt trigger is inverted* by inverter A_3 and is available at pin 3. The output waveforms are shown in Fig. 5.8 (c).

The output frequency of the VCO can be calculated as follows:

The total voltage on the capacitor changes from 0.25 V_{cc} to 0.5 V_{cc}. Thus $\Delta v = 0.25\ V_{cc}$. The capacitor chargers with a constant current source.

So
$$\frac{\Delta v}{\Delta t} = \frac{i}{C_T}$$

or,
$$\frac{0.25\,V_{cc}}{\Delta t} = \frac{i}{C_T}$$

or,
$$\Delta t = \frac{0.25\,V_{cc}C_T}{i}$$

The time period T of the triangular waveform = $2\Delta t$. The frequency of oscillator f_o is,

$$f_o = \frac{1}{T} = \frac{1}{2\,\Delta t}$$

$$= \frac{i}{0.5\,V_{cc}C_T}$$

But,
$$i = \frac{V_{cc} - v_c}{R_T}$$

where, v_c is the voltage at pin 5. Therefore,

$$f_o = \frac{2(V_{cc} - v_c)}{C_T R_T V_{cc}}$$

The output frequency of the VCO can be changed either by (i) R_T, (ii) C_T or (iii) the voltage v_c at the modulating input terminal pin 5. The voltage v_c can be varied by connecting a R_1R_2 circuit as shown in Fig. 5.8 (d). The components R_T and C_T are first selected so that VCO output frequency lies in the centre of the operating frequency range. Now the modulating input voltage is usually varied from 0.75 V_{cc} to V_{cc} which can produce a frequency variation of about 10 to 1. With no modulating input signal, if the voltage at pin 5 is biased† at (7/8) V_{cc}, Eq. gives the VCO output frequency as,

$$f_o = \frac{2(V_{cc} - (7/8)\,V_{cc})}{C_T R_T V_{cc}} = \frac{1}{4R_TC_T} = \frac{0.25}{R_TC_T}$$

4.5 Timer IC LM 555

The 555 is a monolithic timing circuit that can produce accurate & highly stable time delays or oscillation. The timer basically operates in one of two modes: either

(i) Monostable (one - shot) multivibrator or

(ii) Astable (free running) multivibrator

The important features of the 555 timer are these:

(i) It operates on +5V to +18 V supply voltages

(ii) It has an adjustable duty cycle

(iii) Timing is from microseconds to hours

(iv) It has a current o/p

(v) When the input is low:

The load current flows through the load connected between Pin 3 & +Vcc in to the output terminal & is called the sink current.

(vi) When the output is high:

The current through the load connected between Pin 3 & +Vcc (i.e. ON load) is zero. However the output terminal supplies current to the normally OFF load. This current is called the source current.

PIN CONFIGURATION OF 555 TIMER:

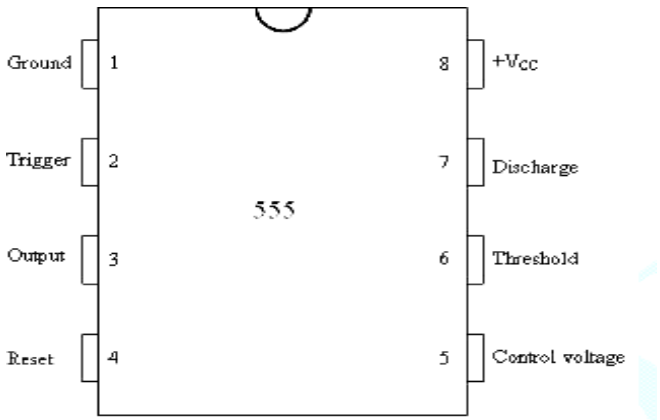


Figure 4.5.1: Pin diagram of IC555 Timer

Pin 4: Reset:

The 555 timer can be reset (disabled) by applying a negative pulse to this pin. When the reset function is not in use, the reset terminal should be connected to +Vcc to avoid any false triggering.

Pin 5: Control voltage:

An external voltage applied to this terminal changes the threshold as well as trigger voltage. In other words by connecting a potentiometer between this pin & GND, the pulse width of the output waveform can be varied. When not used, the control pin should be bypassed to ground with 0.01 capacitor to prevent any noise problems.

Pin 6: Threshold:

This is the non inverting input terminal of upper comparator which monitors the voltage across the external capacitor.

Pin 7: Discharge:

This pin is connected internally to the collector of transistor Q1. When the output is high Q1 is OFF. When the output is low Q is (saturated) ON.

Pin 8: +Vcc:

The supply voltage of +5V to +18V is applied to this pin with respect to ground.

FUNCTIONAL BLOCK DIAGRAM OF 555 TIMER

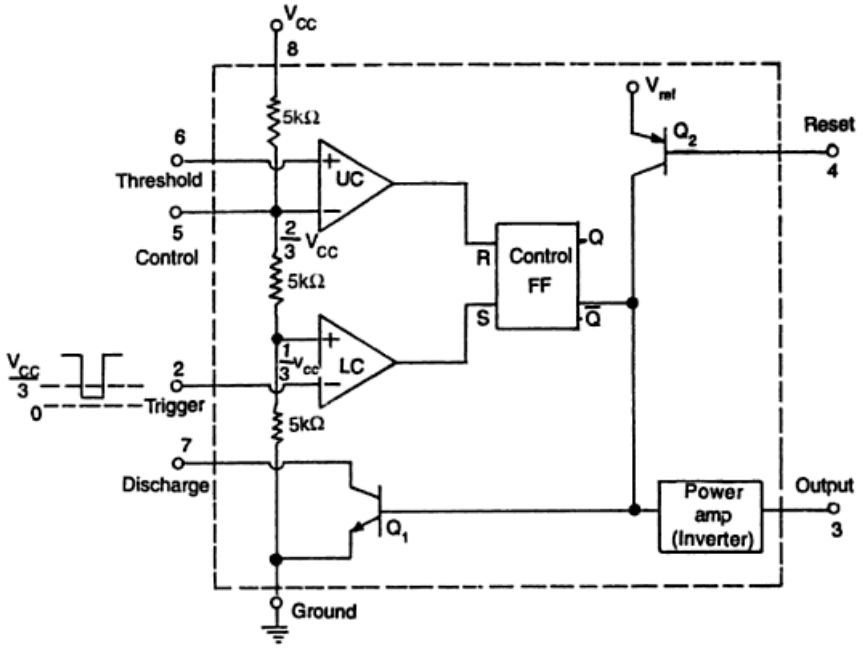


Figure: 4.5.2: Functional Block Diagram of 555 Timer

From the above figure, three 5k internal resistors act as voltage divider providing bias voltage of 2/3 Vcc to the upper comparator & 1/3 Vcc to the lower comparator. It is possible to vary time electronically by applying a modulation voltage to the control voltage input terminal (5).

(i) In the Stable state:

The output of the control FF is high. This means that the output is low because of power amplifier which is basically an inverter. Q = 1; Output = 0

(ii)At the Negative going trigger pulse:

The trigger passes through (Vcc/3) the output of the lower comparator goes high & sets the FF. Q = 1; Q = 0

(iii) At the Positive going trigger pulse: It passes through 2/3Vcc, the output of the upper comparator goes high and resets the FF. Q = 0; Q = 1

The reset input (pin 4) provides a mechanism to reset the FF in a manner which overrides the effect of any instruction coming to FF from lower comparator.

4.6 Monostable Operation:

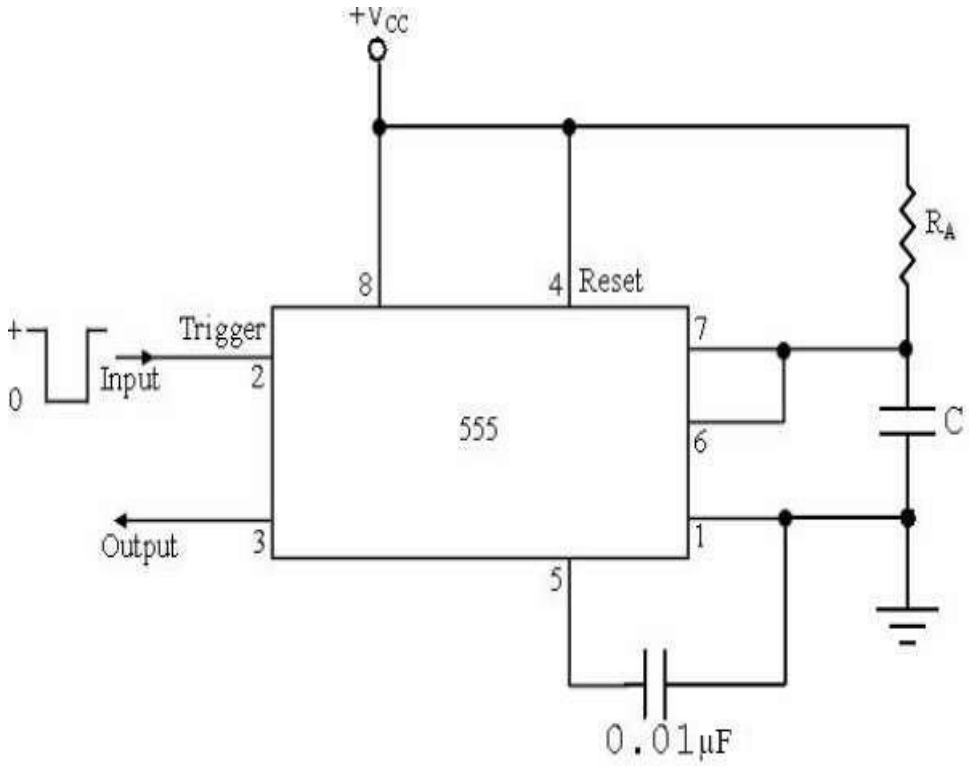


Figure 4.6.1: connected as a Monostable Multivibrator

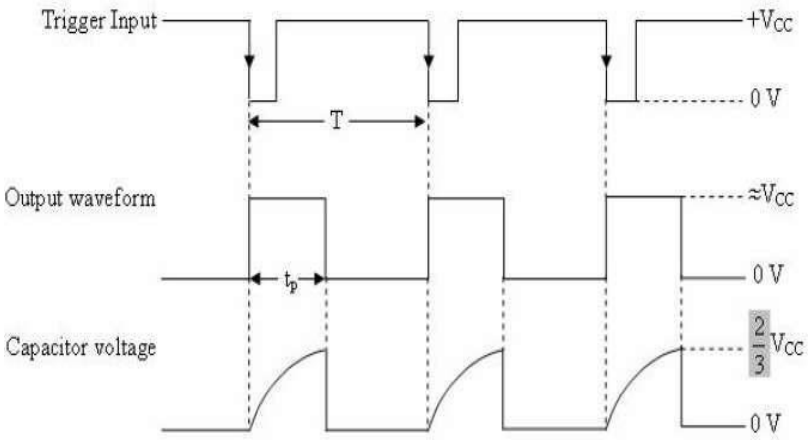


Figure 4.6.2.: Model Graph

Initially when the output is low, i.e. the circuit is in a stable state, transistor Q1 is ON & capacitor C is shorted to ground. The output remains low. During negative going trigger pulse, transistor Q1 is OFF, which releases the short circuit across the external capacitor C & drives the output high.

Now the capacitor C starts charging toward Vcc through RA.When the voltage across the capacitor equals 2/3 Vcc, upper comparator switches from low to high. i.e. Q = 0, the transistor Q1 = OFF ; the output is high.

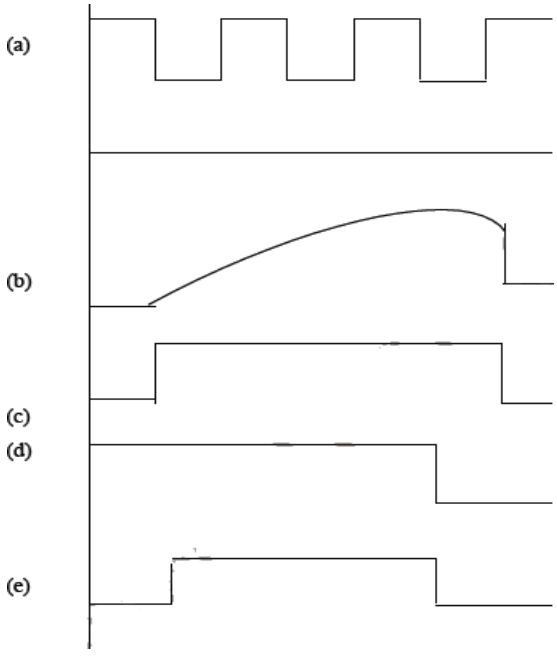


Figure 4.6.2: Output Waveform

Since C is unclamped, voltage across it rises exponentially through R towards Vcc with a time constant RC (fig b) as shown in below. After the time period, the upper comparator resets the FF,

i.e. Q = 1, Q1 = ON; the output is low.[i.e discharging the capacitor C to ground potential (fig c)]. The voltage across the capacitor as in fig (b) is given by

Vc = Vcc (1-e-t/RC) ..... (1)

Therefore At t = T,

Vc = 2/3 Vcc 2/3 Vcc = Vcc(1-e-

RC)

or

T = RC ln (1/3)

Or

T = 1.1RC seconds .....(2)

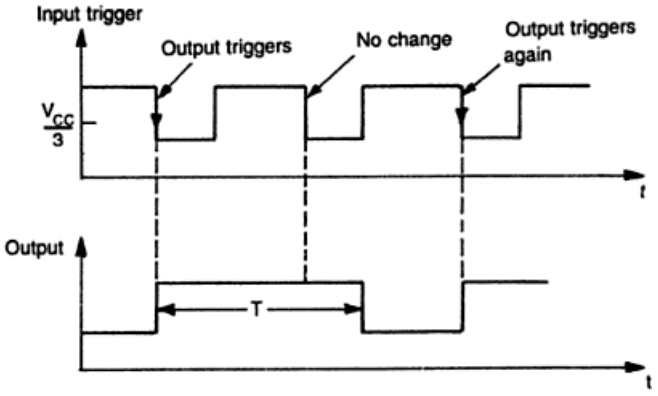
If the reset is applied Q2 = OFF, Q1 = ON, timing capacitor C immediately discharged. The output now will be as in figure (d & e). If the reset is released output will still remain low until a negative going trigger pulse is again applied at pin 2.

Applications of Monostable Mode of Operation:

(a).Frequency Divider:

The 555 timer as a monostable mode. It can be used as a frequency divider by adjusting the length of the timing cycle tp with respect to the time period T of the trigger input. To use the monostable multivibrator as a divide by 2 circuit, the timing interval tp must be a larger than the time period of the trigger input. [Divide by 2 tp > T of the trigger]

By the same concept, to use the monostable multivibrator as a divide by 3 circuit, tp must be slightly larger than twice the period of the input trigger signal & so on, [divide by 3 tp > 2T of trigger]



Frequency divider circuit

Figure 4.6.3: Output Waveform

(b).Pulse width modulation:

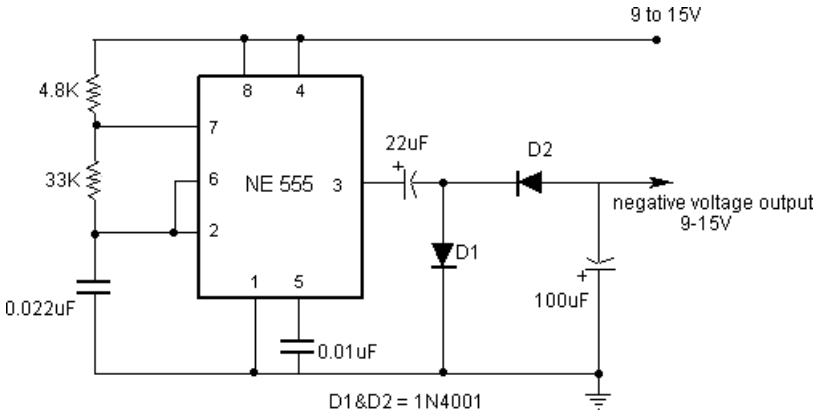


Figure 4.6.3:Pulse Width Modulation

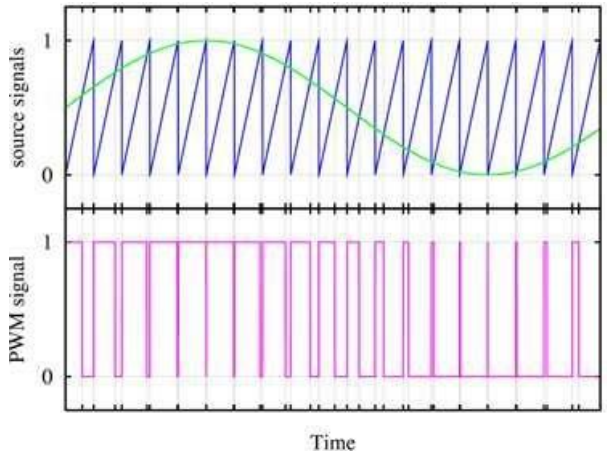


Figure 4.6.4:OutputWaveform

Pulse width of a carrier wave changes in accordance with the value of a incoming (modulating signal) is known as PWM. It is basically monostable multivibrator. A modulating signal is fed in to the control voltage (pin 5). Internally, the control voltage is adjusted to 2/3 Vcc externally applied modulating signal changes the control voltage level of upper comparator. As a result, the required to change the capacitor up to threshold voltage level changes, giving PWM output.

(a) Pulse Stretcher:

This application makes use of the fact that the output pulse width (timing interval) of the monostable multivibrator is of longer duration than the negative pulse width of the input trigger. As such, the output pulse width of the monostable multivibrator can be viewed as a stretched version of the narrow input pulse, hence the name — Pulse stretcher‖. Often, narrow –pulse width signals are not suitable for driving an LED display, mainly because of their very narrow pulse widths. In other words, the LED may be flashing but not be visible to

the eye because its on time is infinitesimally small compared to its off time. The 55 pulse stretcher can be used to remedy this problem. The LED will be ON during the timing interval tp = 1.1RAC which can be varied by

changing the value of RA &C.

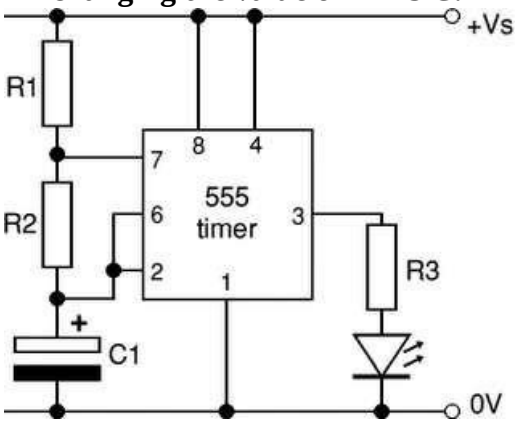


Fig: Pulse Stretcher

Figure 4.6.5: Pulse stretcher

4.7 :The 555 timer as an Astable Multivibrator:

An Astable multivibrator, often called a free running multivibrator, is a rectangular wave generating circuit. Unlike the monostable multivibrator, this circuit does not require an external trigger to change the state of the output, hence the name free running. However, the time during which the output is either high or low is determined by 2 resistors and capacitors, which are externally connected to the 55 timer.

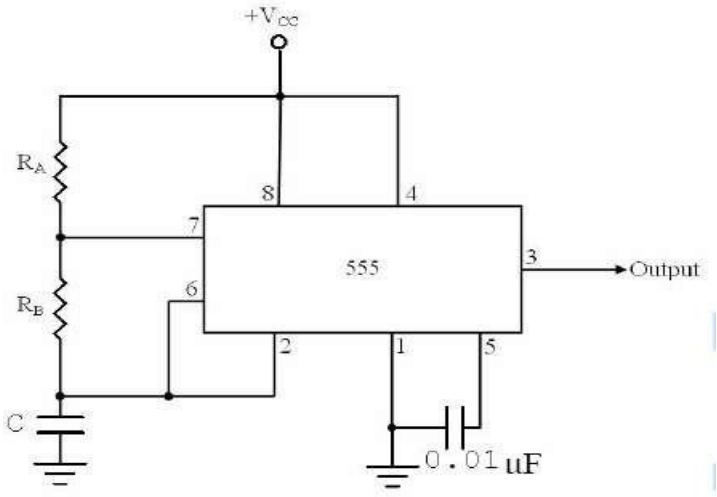


Figure 4.7.1: Astable Multivibrator

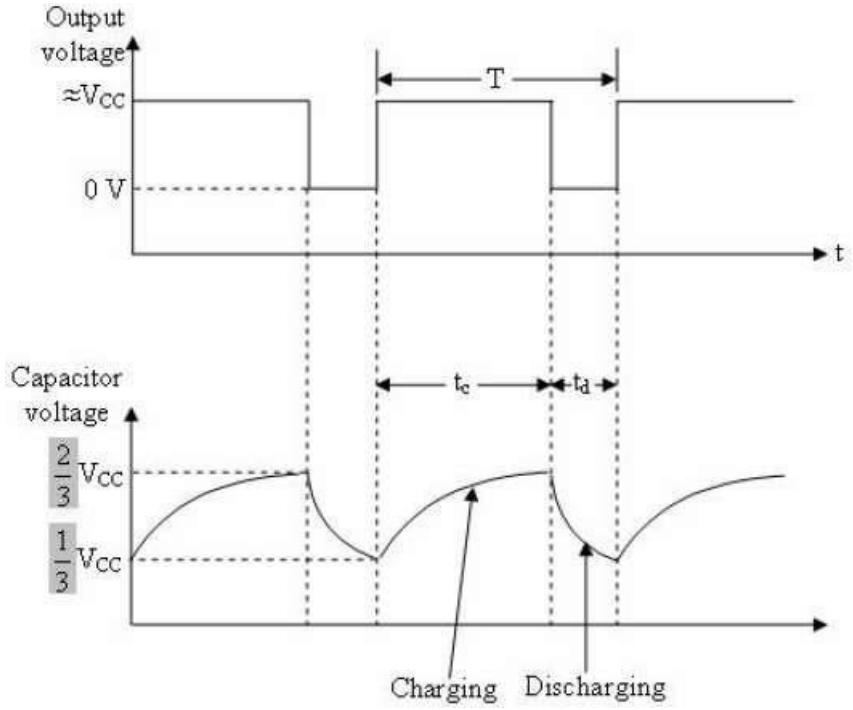


Figure 4.7.2: Model Graph

The above figure shows the 555 timer connected as an astable multivibrator and its model graph Initially, when the output is high:Capacitor C starts charging toward Vcc through RA & RB. However, as soon as voltage across the capacitor equals 2/3 Vcc. Upper comparator triggers the FF & output switches low.

When the output becomes Low:

Capacitor C starts discharging through RB and transistor Q1, when the voltage across C equals 1/3 Vcc, lower comparator output triggers the FF & the output goes High. Then cycle repeats. The capacitor is periodically charged & discharged between 2/3 Vcc & 1/3 Vcc respectively. The time during which the capacitor charges from 1/3 Vcc to 2/3 Vcc equal to the time the output is high & is given by tc = (RA+RB)C ln 2… (1) Where [ln 2 = 0.69]

= 0.69 (RA+RB)C

Where RA &RB are in ohms. And C is in farads.

Similarly, the time during which the capacitors discharges from 2/3 Vcc to 1/3 Vcc is equal to the time, the output is low and is given by,

tc = RB C ln 2

td = 0.69 RB C.....(2)

where RB is in ohms and C is in farads.

Thus the total period of the output waveform is T = tc + td = 0.69

(RA+2RB)C ..... (3)

This, in turn, gives the frequency of oscillation as,f 0 = 1/T = 1.45/(RA+2RB)C (4)

Equation 4 indicates that the frequency f 0 is independent of the supply voltage Vcc. Often the term duty cycle is used in conjunction with the astable multivibrator. The duty cycle is the ratio of the time tc during which the output is high to the total time period T. It is generally expressed as a percentage.

%duty cycle = (tc / T)* 100

%DC = [(RA+RB)/ /(RA+2RB)] * 100

Astable Multivibrator Applications:

Square wave oscillator:

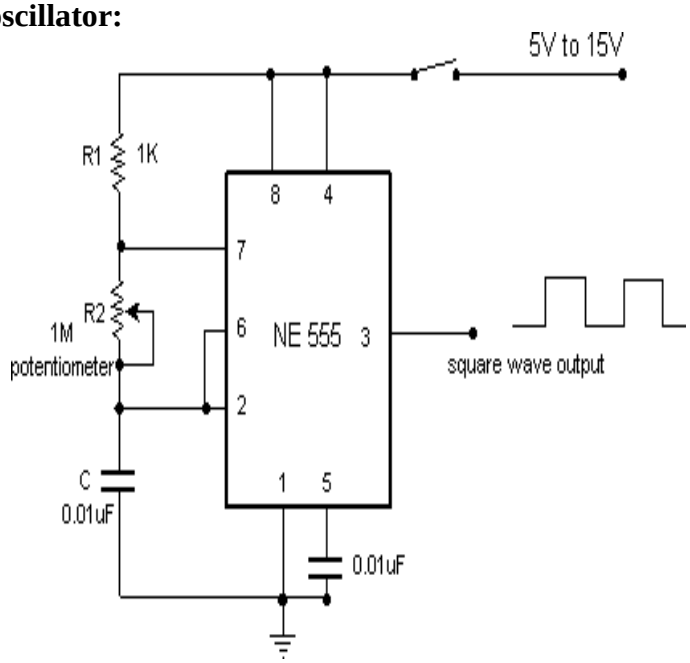
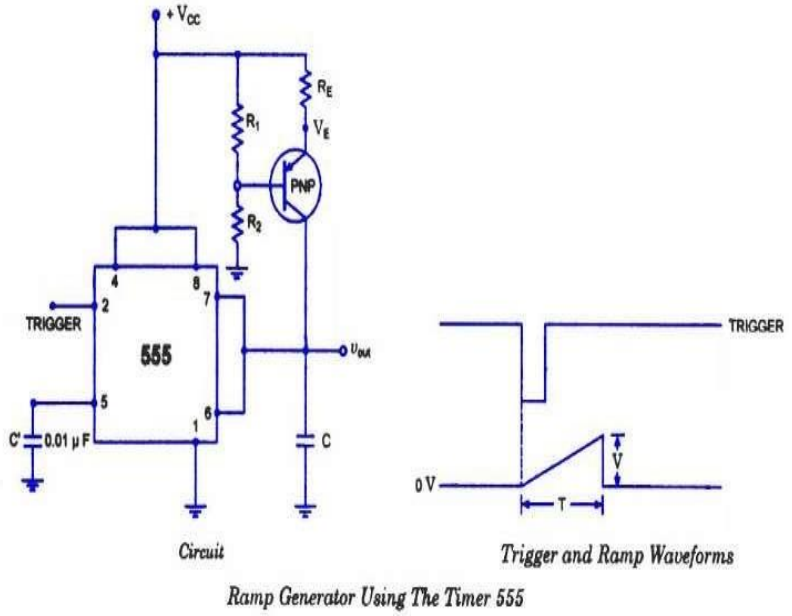


Figure 4.7.3: Square wave oscillator

With out reducing RA = 0 ohm, the astable multivibrator can be used to produce square wave output. Simply by connecting diode D across Resistor RB. The capacitor C charges through RA &diode D to approximately 2/3 Vcc & discharges through RB & Q1 until the capacitor voltage equals approximately 1/3 Vcc, then the cycle repeats.

To obtain a square wave output, RA must be a combination of a fixed resistor & potentiometer so that the potentiometer can be adjusted for the exact square wave.

(a) Free-running Ramp generator:



Ramp Generator Using The Timer 555

Figure 4.7.4: Free Running Ramp Generator

The astable multivibrator can be used as a free – running ramp generator when resistor RA &RB are replaced by a current mirror.

- **The current mirror starts charging capacitor C toward Vcc at a constant rate.**
- **When voltage across C equals to 2/3 Vcc, upper comparator turns transistor Q1 ON & C rapidly discharges through transistor Q1.**
- **When voltage across C equals to 1/3 Vcc, lower comparator switches transistor OFF & then capacitor C starts charging up again..**
- **Thus the charge – discharge cycle keeps repeating**
- **The discharging time of the capacitor is relatively negligible compared to its charging time.**

- **The time period of the ramp waveform is equal to the charging time & is approximately is given by,**

T = VccC/3IC ..... (1)
IC = (Vcc - VBE)/R = constant current

Therefore the free-running frequency of ramp generator is f 0 = 3IC/ Vcc C..... (2)

Pulse-Position Modulator

The pulse-position modulator can be constructed by applying a modulating signal to pin 5 of a 555 timer connected for astable operation

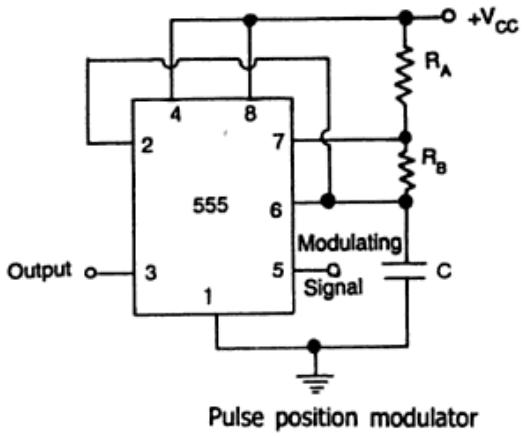
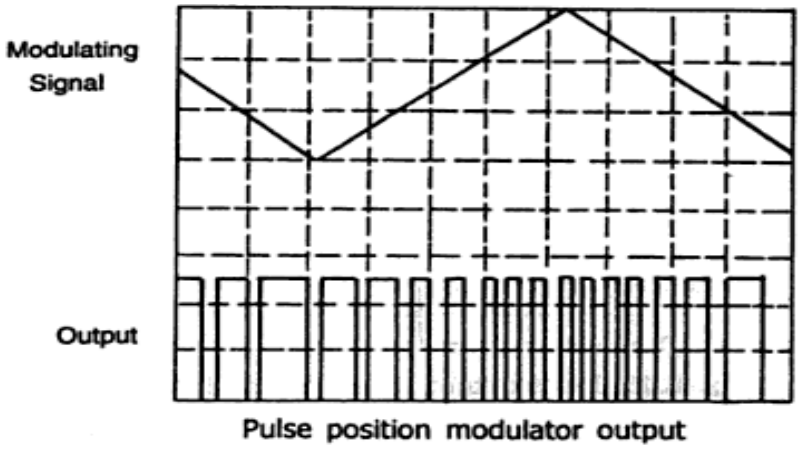


Figure 4.7.5: Pulse Position Modultor



as shown in Fig. 8.22. The output pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied. Figure 8.23 shows the output waveform generated for a triangle wave modulation signal. It may be noted from the output waveform that the frequency is varying leading to pulse position modulation. The typical practical component values may be noted as

$R_A = 3.9\ k\Omega,\ R_B = 3\ k\Omega,\ C = 0.01\ \mu F$

$V_{cc} = 5V$ (any value between 5V to 18V may be chosen)

4.8 :SCHMITT TRIGGER

The use of 555 timer as B Sehmitt Trigger ia shown in Fig. 8.24. Here the two internal coinparators are tied together and externally biased at YJ2 through 2t¿ and B$. Since the upper compazator will trip at *!2/3)* Vq and lower compsrator at (1/3) Vq, the bias provided by *R* and RJ is centered within these

two thresholds,

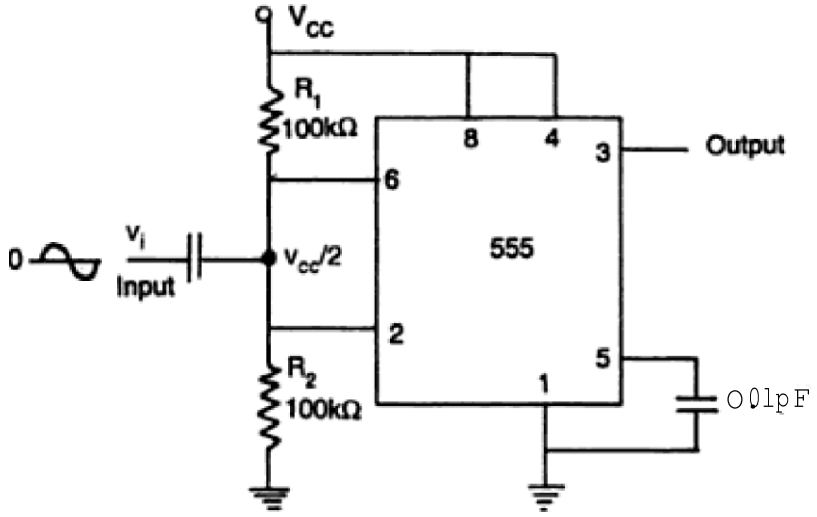


Fig. 4.8.1: Timer in Schmitt Trigger Operation

Thus, a sine wave of sufficient amplitude (> *Vfi6* —- 2f8 *V„* — UJ2) tn exceed the reference levels causea the internal flip-flop to alternately set and reset, providing a aquare wave output a8 shown in Fig. 8.25,

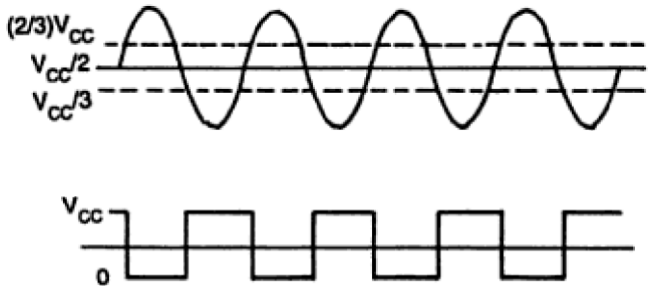


Figure 4.8.2: Input output waveforms of Schmitt Tñgger

It may be noted that unlike conventional multivibrator, no frequency division is taking place and frequency of square w•ve rerriairi6 the same as that of input signal.

Comparison of Monostable and astable multivibrator

S. No.	Monostable multivibrator	Astable multivibrator
1.	It has only one stable state and one quasi stable state	There is no stable state at all
2.	Trigger is required for the operation change its state from stable to quasi stable state	No trigger is required for change of state. Thus called *free-running*.
3.	Two components R and C are necessary with IC555.	Three components RA, RB and C are necessary with IC555.
4.	The pulse width of quasi-stable state is given by, $W=1.1\ RC$ seconds	The frequency is given by, $f=1.44/(RA+2RB)\ Hz$
5.	The frequency of operation is controlled by frequency of trigger pulse applied.	The frequency of operation is controlled by RA, RB and C.
6.	The applications are, timer, frequency divider, pulse width modulation etc.	The applications are, square wave generator, flasher VCO, FSK generator etc.

Text Book References:

1. Ramakant A.Gayakwad, "0P-AMP and Linear ICs", 4th Edition, Prentice Hall / Pearson Education, 1994.

2. D.Roy Choudary, Shail Jain, "Linear Integrated Circuits", New Age International Pvt. Ltd., 2000.

3. Grey and Meyer, "Analysis and Design of Analog Integrated Circuits, 4th Edition, Wiley International, 2001.

4. Michael Jacob, "Applications and Design with Analog Integrated Circuits, 2nd Edition, Prentice Hall of India, 1993.

5. S. Salivahanan, V.S. Kanchana Bhaaskaran, "Linear integrated circuits", 3rd Edition, McGraw-Hill, 2011.

6. William D.StaneIy, "Operational Amplifiers with Linear Integrated Circuits", 4th Edition, Pearson Education, 2004.

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5.1. Integrated circuit Tuned amplifier

The circuit shown in this section is an IC tuned amplifier that amplifies a signal over a narrow band of frequencies centered at f_r. here the input signal is applied through the tuned transformer T_1 to the base of Q_1. The load R_L is connected across the tuned transformer T_2 in the collector circuit of Q_3. The transistor Q_1 and Q_3 provides the amplification whereas Q_2 provides the control of magnitude of the gain. The combination of Q_1 and Q_3 acts as a common-emitter and common-base cascade (CE-CB) pair. The input resistance and the current gain of a cascade pair are essentially the same as those of a CE stage the output resistance is the same as that of a CB stage.

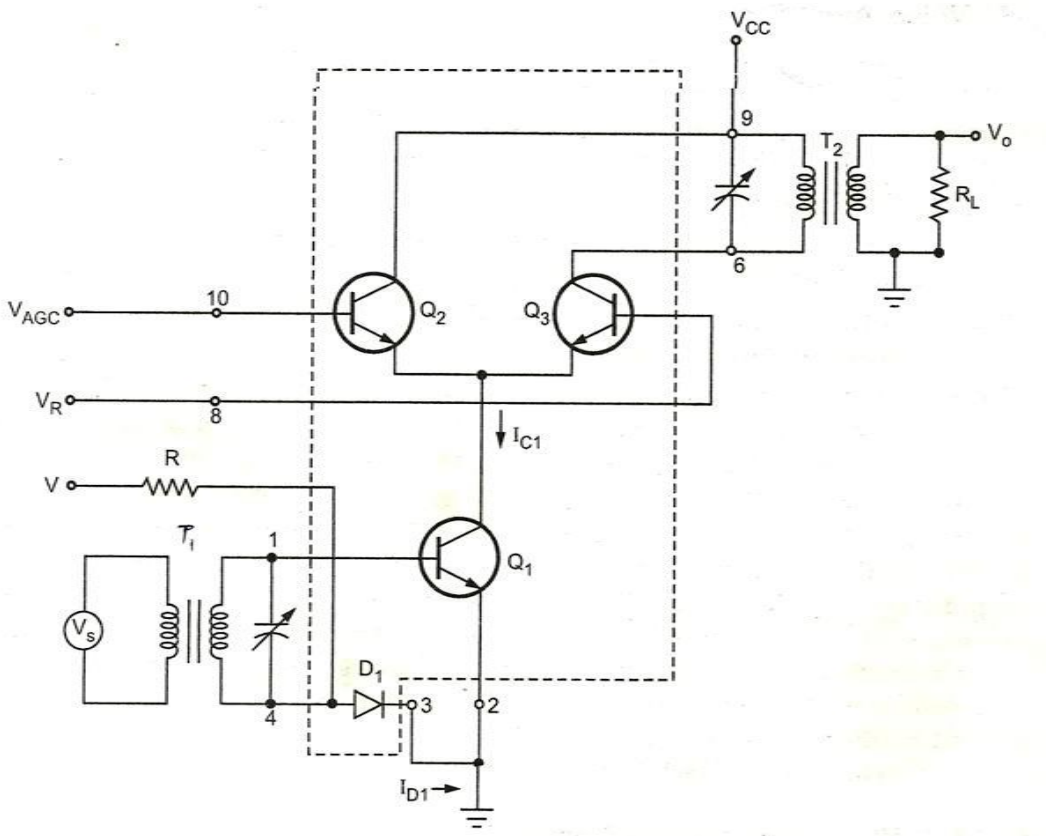

Fig. 5.1.Integrated Circuit tuned amplifier.

The voltage V_{AGC} applied to the base of transistor Q_2 is used to provide automatic gain control. The variation in V_{AGC} cause changes in the division of the current between transistors Q_2 and Q_3. When V_{AGC} is greater than V_R Q_2 conducts more than Q_3, reducing voltage gain. On the other hand when V_R greater than V_{AGC}, Q_3 conducts more than Q_2, which increases voltage gain.

V_R greater than V_{AGC}, Q_2 is cut-off and the collector current of Q_1 flows through Q_3 providing maximum voltage gain A_V. the change in V_{AGC} causes the change in the division of current and not the collector current of Q_1. Thus the input impedance of Q_1 remains constant and the input circuit is not tuned.

The voltage V and resistance R establish the dc current I_{D1} through the diode D1. The voltage V_{BE1} is nearly equal to V_{D1} and the collector current I_{C1} is within the ± 5% of I_{D1}.

Advantages of tuned amplifiers:

1. Signal to noise ratio is good
2. They are suited for radio transmitters and receivers.
3. Required bandwidth of amplification can be selected

Disadvantages of tuned amplifiers

1. Inductors and capacitors of tuned amplifiers become bulky and costly.
2. As the band of frequency is increased, the design is complex.
3. They are not suitable for amplifying audio frequencies.

5.2 Instrumentation Amplifier

Many instruments use sensors (transducers) for measurement of temperature, pressure, weight, humidity, viscosity etc. The sensors convert other form of energy to proportional electrical energy. But the sensor outputs are very low-level signals. These low-level signals cannot drive next stages of the system. And other external noises shall still reduce the signal level. So to enhance such signals to desired level using a special amplifier with high CMRR, high input impedance, and low power consumption termed **Instrumentation amplifier**.

The instrumentation amplifier is also called data amplifier and is a difference amplifier basically. The expression for its voltage gain is in the form shown below,

$$A = \frac{V_o}{V_2 - V_1}$$

Where

V_o = The amplifier output Voltage

$V_2 - V_1$ = Differential input voltage

oamplifier

Requirements of Instrumentation amplifier

1. Accurate and stable gain is the basic requirement. And the gain shall be finite.
2. Gain shall be easily adjusted and shall be precisely done.
3. High input impedance

4. Low output impedance
5. High CMRR
6. Low power consumption
7. Low temperature drifts
8. High Slew Rate

Two-op amp Instrumentation amplifier

The instrumentation amplifier with two op amp is shown below.

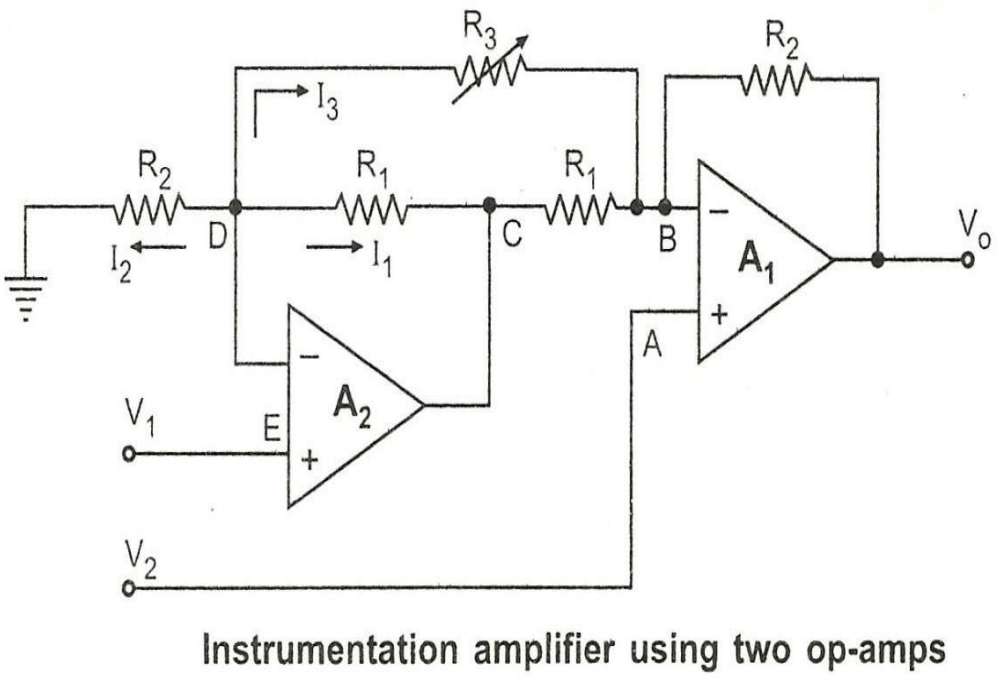

Fig. 5.2. Instrumentation amplifier using two op amps

The above circuit consists of two operational amplifiers A1 and A2.

Analysis:

For amplifier A1,

Node voltage at A shall be same as node B.

$$V_A = V_B = V_2$$

Similarly for amplifier A2, Node voltage at E shall be same as node D.

$$V_D = V_E = V_1$$

Now,

$$I_2 = \frac{V_D}{R_2} = \frac{V_1}{R_2}$$

$$I_1 = \frac{V_D - V_C}{R_1} = \frac{V_1 - V_C}{R_1}$$

$$I_3 = \frac{V_D - V_B}{R_3} = \frac{V_1 - V_2}{R_3}$$

Applying KCL at node D, $I_1 + I_2 + I_3 = 0$

$$\frac{V_1 - V_C}{R_1} + \frac{V_1}{R_2} + \frac{V_1 - V_2}{R_3} = 0$$

$$V_1\left[\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right] - \frac{V_2}{R_3} = \frac{V_C}{R_1}$$

Similarly applying KCL at node B and neglecting input current of op-amps we can write,

$$\frac{V_B - V_D}{R_3} + \frac{V_B - V_C}{R_1} + \frac{V_B - V_o}{R_2} = 0$$

$$\frac{V_2 - V_1}{R_3} + \frac{V_2 - V_C}{R_1} + \frac{V_2 - V_o}{R_2} = 0$$

$$V_2\left[\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right] - \frac{V_1}{R_3} - \frac{V_o}{R_2} = \frac{V_C}{R_1}$$

Equating both the expressions V_C/R_1, we get,

$$V_1\left[\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right] - \frac{V_2}{R_3} = V_2\left[\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right] - \frac{V_1}{R_3} - \frac{V_o}{R_2}$$

Simplifying we get

$$\frac{V_o}{V_2 - V_1} = 1 + \frac{R_2}{R_1} + \frac{2R_2}{R_3}$$

The differential input is $V_2 - V_1$ while V_o is the output voltage. Thus the voltage gain of this circuit is

$$A_V = 1 + \frac{R_2}{R_1} + \frac{2R_2}{R_3}$$

As the resistance R3 is variable, the circuit permits gain variation, precisely.

Advantages of two op amp Instrumentation amplifier

The instrumentation amplifier with two op amp has following advantages.

1. The gain variation is easy and precise
2. The CMRR value is completely independent of the setting of resistance R3. Hence with the precision ratios for R2/R1, the gain can be changed without degrading the performance of the amplifier.
3. The resistance R3 is separate from the accurately matched resistances R1 and R2, which are required for symmetric arrangement.

Limitations of two op amp Instrumentation amplifier

1. The problem is resistances R1 and R2 must be accurately matched.
2. The input V1 has to propagate through A2 before reaching A1. Due to this additional delay, common mode components of the two signals will no longer cancel out with each other, at high frequencies. Thus symmetry of input is not there where V1 has time delay than V2 to reach A1.
3. CMRR decreases with frequency because of the above asymmetrical input with time delay.

Three-op amp Instrumentation amplifier

The instrumentation amplifier with three op amp is shown below.

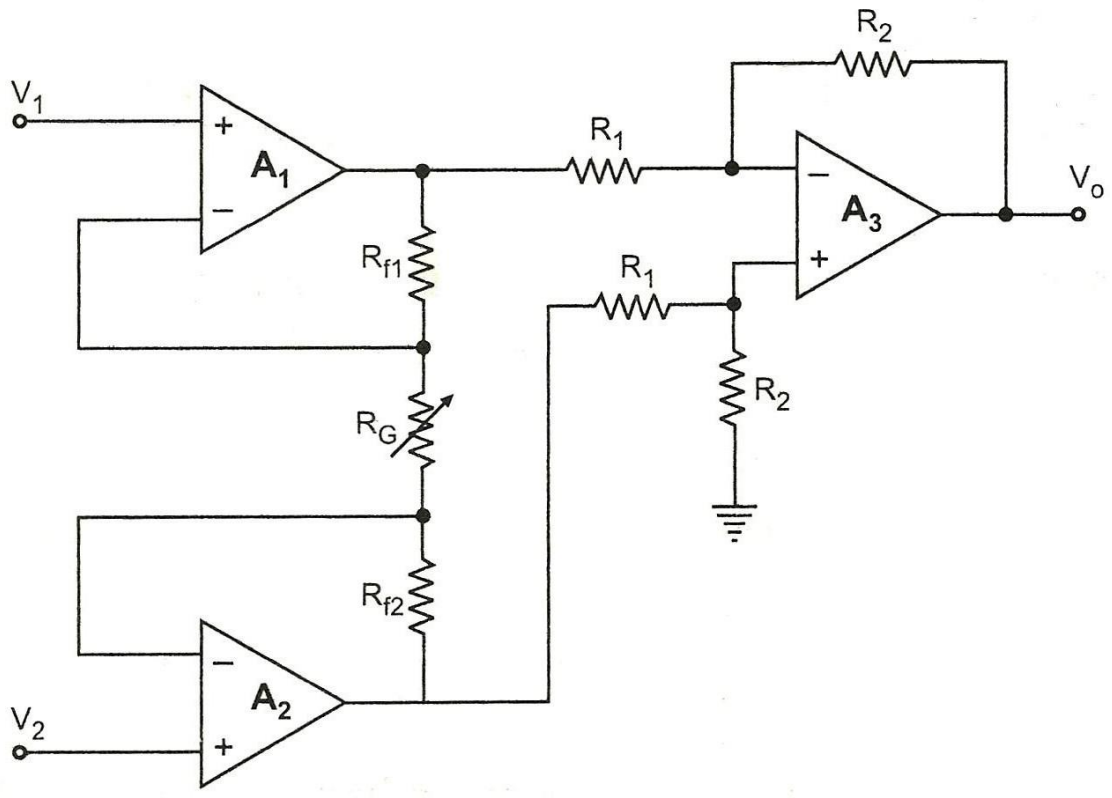

Fig. 5.2.2. Instrumentation amplifier using three op amps

The above circuit consists of three operational amplifiers A1, A2 and A3.

Since a non-inverting amplifier A3 is added to each of the basic difference amplifier inputs. The op-amps A1 and A2 are non-inverting amplifiers forming first stage of the amplifier. The op-amp A3 is a difference amplifier forming an output stage of the amplifier.

Analysis:

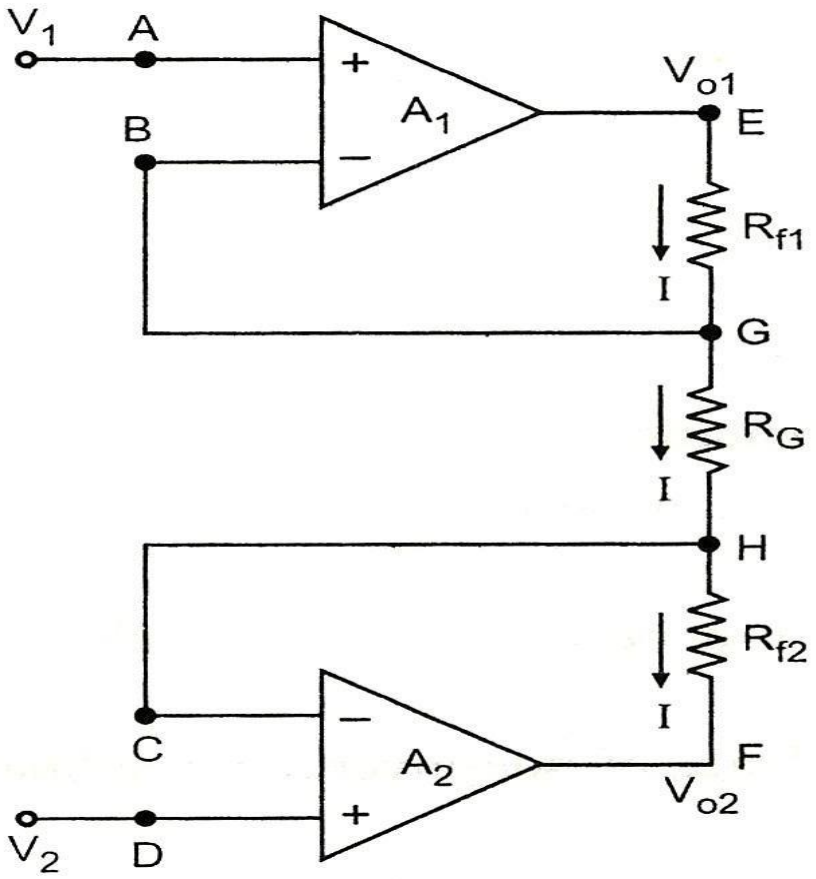

Fig. 5.2.3. Analysis of Three op-amp Instrumentation Amplifier

If the output of the op-amp A1

If the output of the op-amp A1 is V01 and op-amp A2 is V02,

$$V_o = \frac{R_2}{R_1}(V_{02} - V_{01})$$

Expression for V02, V01 in terms of V1, V2, Rf1, Rf2 and RG: From above Fig. 5.2.3 The node potential of op-amp A1 is V1 thus node B shall also B and G are V1. The node D potential of op-amp A2 is V2. Node C and H potential is also V2.

Input current of Op-amp A1 and A2, are zero. Hence current I remain the same through Rf1, Rf2, and RG.

Applying ohms law between the nodes E and F, we get,

$$I = \frac{V_{01} - V_{02}}{2R_f + R_G}$$

Now from observations of Nodes G and H,

$$I = \frac{V_G - V_H}{R_G} = \frac{V_1 - V_2}{R_G}$$

Equating above two equations,

$$\frac{V_{01} - V_{02}}{2R_f + R_G} = \frac{V_1 - V_2}{R_G}$$

$$V_{01} - V_{02} = \frac{(V_1 - V_2)(2R_f + R_G)}{R_G}$$

Substituting the above $V_{01} - V_{02}$ in the equation $V_o = \frac{R_2}{R_1}(V_{02} - V_{01})$, we get,

$$V_0 = \frac{R_2}{R_1}\frac{(V_1 - V_2)(2R_f + R_G)}{R_G}$$

$$V_0 = \frac{R_2}{R_1}\left[1 + \frac{2R_f}{R_G}\right](V_1 - V_2)$$

This is the overall gain of the circuit.

Advantages of three op-amp instrumentation amplifier.

Following are the advantages of three op-amp instrumentation amplifier circuit:

1. With the hep of variable resistor R_G, the gain of the amplifier can be easily varied.
2. Gain depends on external resistances and hence can be adjusted accurately and made stable by selecting high quality resistances.
3. The input impedance depends on the input impedace of non-inverting amplifiers which is extremely high.

5.3 Voltage Regulators

The voltage regulator in its simplest form consists of Voltage

reference, V_R

Error amplifier

Feedback network

Active series or shunt control element

The voltage reference generates a voltage level which is applied to the comparator circuit, which is generally an error amplifier. The second input to the error amplifier is obtained through feedback network. Generally using the potential divider, the feedback signal is derived by sampling the output voltage. The error amplifier converts the difference between the output sample and the reference voltage into an error signal. This error signal in-turn controls the active element of the regulator circuit in order to compensate the change in the output voltage. Such an active element is generally a transistor.

5.3.1 Types of voltage regulators

Depending upon where the control element is connected in the regulator circuit, the regulators are basically classified as

Series voltage regulator

Shunt voltage regulator

Each type provides a constant d.c. output voltage which is regulated.

5.3.2 Advantages of IC voltage Regulators

1. Easy to use
2. It greatly simplifies power supply design
3. Due to mass production, low in cost
4. IC voltage regulators are versatile
5. Conveniently used for local regulation
6. These are provided with features lime built-in protection programmable output, current/voltage boosting, internal short circuit current limiting etc.

5.3.3 Classification of IC voltage regulators

The IC voltage regulators are classified as shown in the figure below.

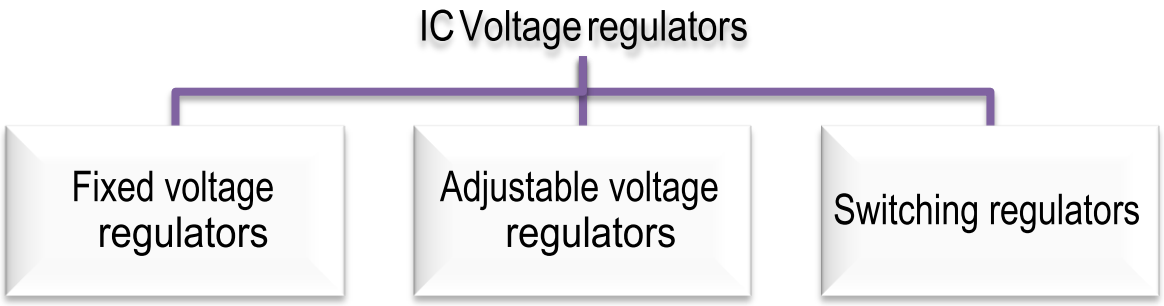

Fig. 5.3.3 Classification of IC regulators

5.3.4 Three terminal fixed voltage regulators

As the name suggest, three terminal voltage regulators have three terminals namely input which is unregulated (V_{in}), regulated output (V_o) and common or a ground terminal. These regulators do not require any feedback connections. The figure below shows the basic three terminal voltage regulators.

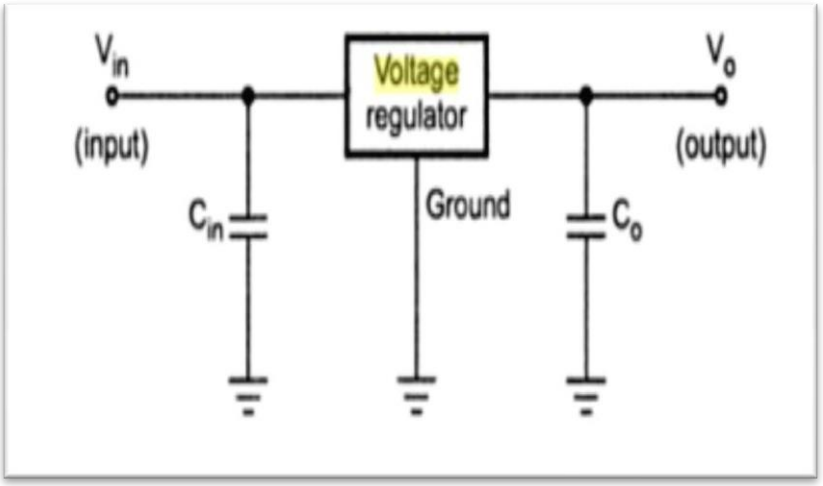

Fig.5.3.4. Basic regulator circuit (Three Terminals)

The capacitor C_{in} is required if regulator is located at appreciable distance more than 5 cm from a power supply filter. The output capacitor C_o may not be needed but if used it improves the transient response of the regulator i.e. regulator response to the transient changes in the load. This capacitor also reduces the noise present at the output. The difference between V_{in} and V_o ($V_{in} - V_o$) is called as dropout voltage and it must be typically 2.0V even during the low point on the input ripple voltage, for the proper functioning of the regulator.

5.3.5 IC series of three terminal fixed voltage regulators

The popular IC series of three terminal regulators is □A78XX and □A79XX. The series □A78XX is the series of three terminal positive voltage regulators while □A79XX is the series of three terminal negative voltage regulators. The last two digits denoted as XX indicate the output voltage rating of the IC.

Such series is available with seven voltage options as indicated in table below.

Device type	Output voltage	Device type	Output voltage
7805	5.0 V	7905	-5.0 V
7806	6.0 V	7906	-6.0 V
7808	8.0 V	7908	-8.0 V
7812	12.0 V	7912	-12.0 V
7815	15.0 V	7915	-15.0 V
7818	18.0 V	7918	-18.0 V
7824	24.0 V	7924	-24.0 V

The 79XX series voltage regulators are available with same seven options as 78XX series, as indicated in the above table. In addition, two extra voltages – 2 V and – 5.2 V are also available with ICs 7902 and 7905.2 respectively.

These ICs are provided with adequate heat sinking and can deliver output currents more than 1 A. these ICs do not require external components. These are provided with internal thermal protection, overload and short circuit protection.

The two series are available in various versions like low-power and high-power versions. The low-power versions are available in plastic or metal packages, like small signal transistors. The higher power versions are packaged in TO-3 type metal cans or in TO-220 type moulded plastic packages like power transistors.

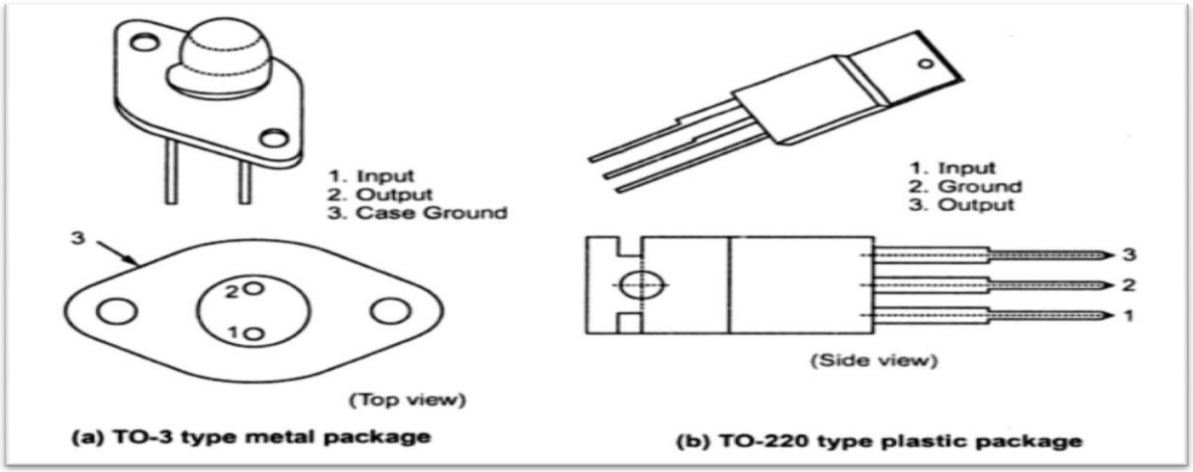

Fig. 5.3.5. Types of IC packages (Voltage Regulators)

5.4. Opto-coupler.

The combined package of an LED and a photo diode is termed as an optocoupler. It is otherwise called as opto-isolator or optically coupled isolator.

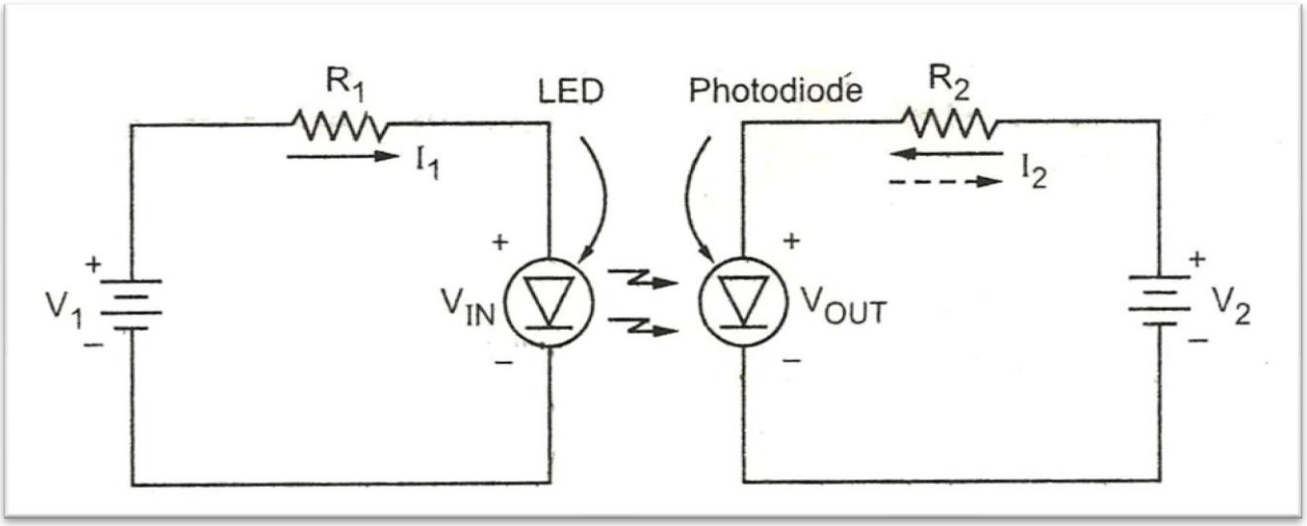

Fig. 5.4.1. Basic Opto-coupler.

The source V_1 and series resistance R_1 decide the forward current I_1 through the LED. Hence LED emits the light. This light is incident on a photodiode. Due to this a reverse current is set up in the output circuit. This current produces a drop across output resistance R_2, the output voltage is the difference between the supply voltage V_2 and the drop across the resistor R_2.

$$V_{out} = V_2 - I_2 R_2$$

Now if input voltage is changed the amount of light emitted by LED changes. This varies the reverse current in the output circuit and hence the output voltage. The output voltage is thus varying in step with the input voltage. This coupling between LED and photodiode is hence called optocoupler. As the name suggest his device can couple an input signal to the output circuit.

The figure 5.4.1 (a) shows the typical optoisolator. It consists of LED and phototransistor.

When the input voltage forward biases the LED light transmitted to the phototransistor turns it on resulting current through the external load as shown in the fig. 5.4.2 (b).

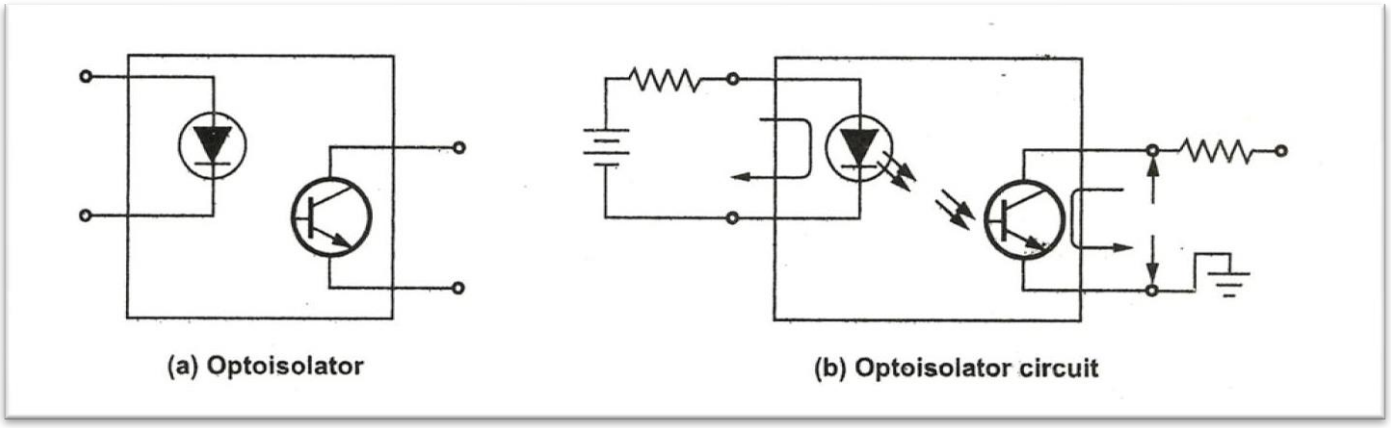

Fig.5.4.2. Optoisolator circuits with Phototransistor

5.4.1 Types of optocouplers

Other than the combination of LED and phototransistor two more types of optocouplers are available which are

1. LED-Photodiode
2. LED-Photodarlington
3. In both the circuits the input current which is the forward current of LED results in the emission of light by LED. This light is detected by photodiode and Photodarlington to produce the output current. These two optocouplers are shown in the fig.5.4.3 (a) and fig. 5.4.3(b)

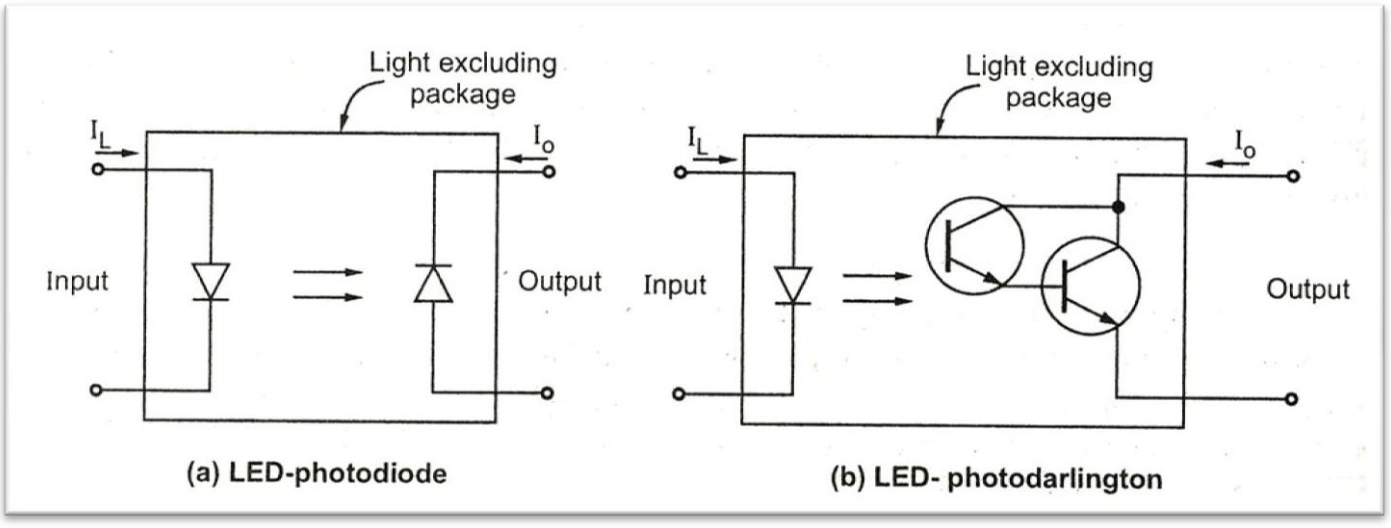

Fig.5.4.3. Types of Optoisolator circuits

The ratio of output current I_0 to the input LED current I_L is called current transfer ratio CTR). This CTR is different for different optocouplers as indicated in the below table.

Table. 5.4.1. Current transfer ratio (CTR) for different detectors

Device	CTR
LED-Photodiode	0.01 – 0.03
LED-Transistor	0.1 – 1
LED-Darlington	1 - 5

The most important point of above devices is that a circuit connected to its input can be electrically fully isolated from the output circuit and that a potential difference of hundreds or thousands of volts can safely exists between two circuits without adversely influencing the optocoupler action.

5.4.2 Characteristics of optocoupler

Following are important characteristics of an optocoupler:

(i)Current transfer ratio (CTR)
(ii) Response time
(iii)VCE (max)
(iv)Bandwidth
(v) Isolation voltage
(vi)Common mode rejection
(vii) IL (max)

1) Current transfer ratio (CTR):

The current transfer ration refers to the ratio of the output collector current (IC) to the input forward current (IF).

$$\text{Current transfer ratio} = \frac{I_C}{I_F} \times 100\%$$

The CTR greatly differs depending on the type of the phototransistor used in photocoupler. The photocoupler using Darlington phototransistor can provide a relatively large collector current from a small input current the CTR also varies with ambient temperature.

2) **Isolation voltage(V_{iso}) Between input and output:**

Isolation voltage (V_{iso}) between input and output is another important factor in choosing a photocoupler. This is because photocouplers are often used for signal transmission between circuits that have different potentials or as interfaces with actuator circuits which tend to generate impulsive voltage such as motor controllers or solenoid driver circuits. Isolation voltage is specified in KV_{rms} with a relative humidity of 40% to 60%.

3) **Response time:**

The response time of an optocoupler depends mainly on the output phototransistor. The response time also depends on the input forward current and load resistance. Since load resistance has a greater influence on the response time, careful setting is required while defining the circuit constant.

4) **Common mode rejection:**

While the photocouplers output is electrically isolated from its input for relatively low frequency signal an impulsive input voltage may cause a displacement current ($i_d = C_f . dv/dt$) to flow due to the floating capacitance (C_f) between the input and output of the optocoupler casing noise voltage to appear at the output.

5) **VCE (max):**

This is the maximum allowable d.c. voltage that can be applied across output transistor or output photodiode.

6) **IL (max):**

This is the maximum permissible d.c. current that can be allowed to flow in the input LED. Typical values vary from 40 mA to 100 mA.

7) **Bandwidth:**

This is the maximum signal frequency that can be usefully passed through the optocoupler when device is operated in its normal mode. Typical values vary from 20 KHz to 500 KHz.

The various advantages of optocouplers are,

1) The electrical isolation provides electrical insulation between input and output but data is transmitted from input to output through beam of light.
2) The response time of optocouplers is so small that they transmit data in Megahertz range.
3) It is capable of transmitting wide-band signal.
4) Unidirectional signal transfer means that output does not loop back to the input circuit.
5) Easy interfacing with logic devices.
6) Compact and light weight.

7) Must faster than the isolation transformers and relays.

8) As signal transfer is unilateral changing load do not affect input.

5.5 CMOS Operational Amplifier

- The bipolar op-amp IC 741 is capable of sourcing and sinking large load currents.
- This is facilitated by the emitter-follower output stage which achieves very low output resistance and this characteristic was used in IC 741 for minimising the loading effects.
- The CMOS op-amps are normally designed for particular applications, wherein only a few picofarads of capacitive load are required to be driven.
- Therefore, the most of the CMOS op-amps do not require a low resistance output stage.
- When the op-amp input terminals are not connected directly to the IC external terminals, they do not need electrostatic input protection devices also.
- The folded cascade op-amp involving a current mirror CMOS design is presented in this section.

Op amps are an important component of modern CMOS IC's. They used to designed as general purpose amplifiers that can meet a variety of requirements. The main target was extremely high gain (>1e5), high input impedance and low output impedance (like an ideal amplifier). This was done (to some extent) at the expense of different aspects of performance (e.g., speed, output voltage range, power, etc.). Designs these days are much more tailored to have (good enough) performance w.r.t. the specific needs of particular applications. Within an IC, often use Operation Transconductance Amplifiers (OTA).

5.5.1 Some performance parameters of op amps

– Gain and Bandwidth

• Want as large as possible

– Output Swing

• Maximize w.r.t. power supply (but supply shrinking in modern processes)

– Linearity

• Combat non-linearity with feedback

– Noise and Offset

• Can minimize by trading off other parameters

– Supply Rejection

• Strong dependence on current source output resistance

5.5.2 Simple One-Stage Op Amps

Two differential pair amplifiers that we have already seen can be used as op amps.

The low-frequency, small-signal gain of both is gmN(roN||roP). The capacitive loads (CL) usually determine their bandwidth

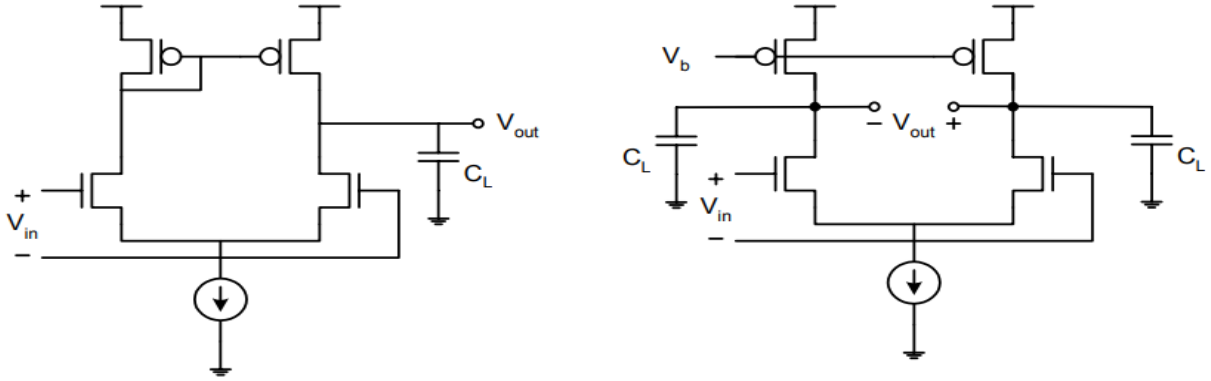

Figure 5.5.2: One Stage Op-amps

5.5.3Cascode Op Amps

In order to achieve higher gain, one can use cascoding. These amplifiers are often called 'telescopic' cascode amps. While gain increases, the output range of these devices are limited.

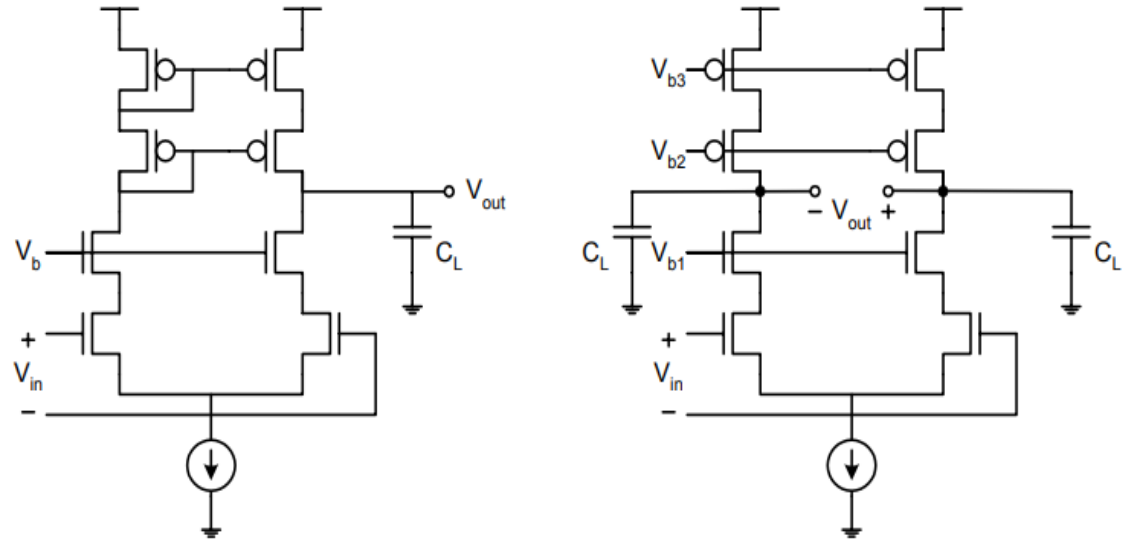

Figure:5.5.3: Two stage Op-amps

5.5.4 Folded Cascode Circuit

In order to alleviate some of the drawbacks of telescopic op amps (limited output range), a “folded cascode” can be used (we analyzed this circuit in HW7)

– M1 is common-source transconductance amp and M2 is common-gate transimpedance amp

– Advantage is M2 no longer stacks on top of M1

– Possible for either pMOS or nMOS cascodes

• The output resistance for cascode and folded cascode are roughly equivalent (gmro2)

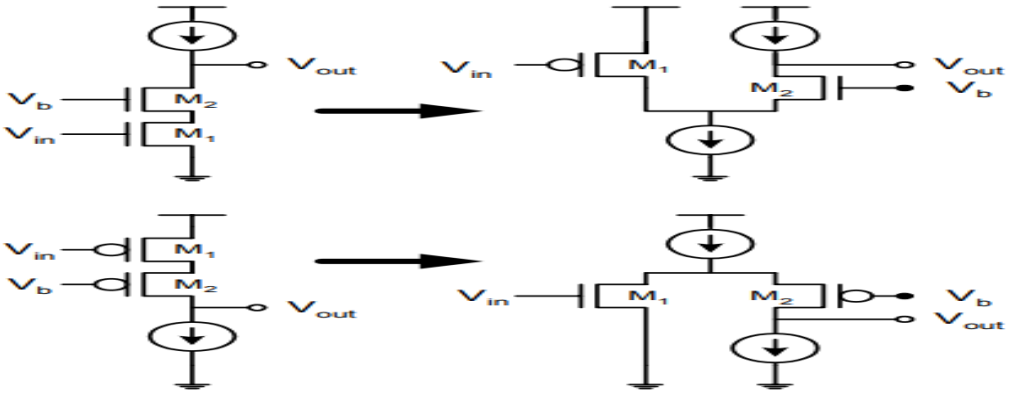

Figure 5.5.4: Folded Cascode Circuits

5.5.5.OPAMP SMALL SIGNAL AND DC ANALYSIS

The small signal differential voltage gain of the input stage is given by

$$A_d = \sqrt{2K_{p1}I_Q}\left(r_{o2} \| r_{o4}\right)$$

Where r_{02} and r_{04} are the output resistance of transistors M2 and M4 respectively.

The input impedance of the second stage is infinite due to the gate-channel oxide insulator. Therefore it results in zero loading effect by the second stage. Assuming the channel length Parameter coefficient λ to be the same for all transistors, we have,

$$r_{o2} = r_{o4} = \frac{1}{\lambda I_D}$$

Where ID , the quiescent drain current in M2 and M4 and is given by ID = IQ/2

The gain of the second stage is

$$A_{v2} = g_{m7}\left(r_{o7} \| r_{o8}\right)$$

$$g_{m7} = 2\sqrt{K_{n7} I_{D7}}$$

$$r_{o\,7} = r_{o8} = \frac{1}{\lambda I_{D7}}.$$

Text Book References:

1. Ramakant A.Gayakwad, "0P-AMP and Linear ICs", 4th Edition, Prentice Hall / Pearson Education, 1994.

2. D.Roy Choudary, Shail Jain, "Linear Integrated Circuits", New Age International Pvt. Ltd., 2000.

3. Grey and Meyer, "Analysis and Design of Analog Integrated Circuits, 4th Edition, Wiley International, 2001.

4. Michael Jacob, "Applications and Design with Analog Integrated Circuits, 2nd Edition, Prentice Hall of India, 1993.

5. S. Salivahanan, V.S. Kanchana Bhaaskaran, "Linear integrated circuits", 3rd Edition, McGraw-Hill, 2011.

6.William D.StanelY, "Operational Amplifiers with Linear Integrated Circuits", 4th Edition, Pearson Education, 2004.