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SCHOOL OF SCIENCE AND HUMANITIES

DEPARTMENT OF PHYSICS

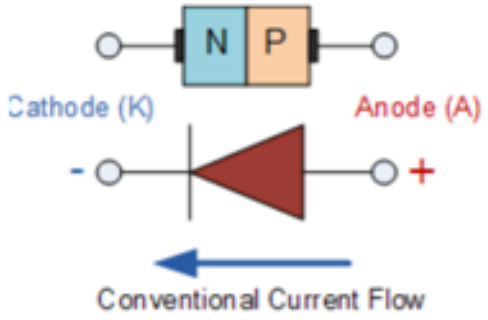
UNIT – I - Digital and Analog Electronics – SPH1216

UNIT – 1 P-N Junctions and Bipolar Junction Transistors

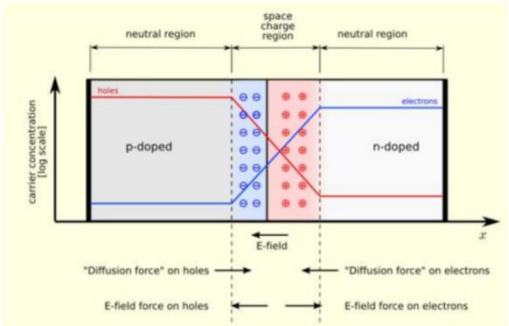
Diode theory, forward and reverse-biased junctions, reverse-bias breakdown, diode applications - clippers, clampers, voltage multipliers, half wave & full wave rectification, Special purpose diodes - Zener diode, Varactor, light emitting diodes, Laser diodes, Transistor fundamentals, transistor configurations, DC operating point, BJT characteristics & parameters.

PN JUNCTION

In a piece of sc, if one half is doped by p type impurity and the other half is doped by n typeimpurity, a PN junction is formed. At the junction there is a tendency of free electrons to diffuseover to the P side and the holes to the N side. This process is called diffusion. Thus a barrier is set up near the junction which prevents the further movement of charge carriers i.e.electrons and holes. As a consequence of induced electric field across the depletion layer, an electrostatic potential difference is established between P and N regions, which are called the potential barrier, junction barrier, diffusion potential or contact potential, Vo. The magnitude of the contact potential Vo varies with doping levels and temperature. Vo is 0.3V for Ge and 0.72 V for Si.



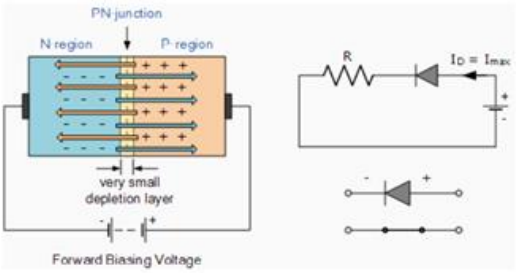
Symbol of PN Junction Diode



The depletion region is of the order of 0.5µm thick. There are no mobile carriers in this narrow depletion region. Hence no current flows across the junction and the system is in equilibrium.

FORWARD BIASED JUNCTION DIODE

When a diode is connected in a Forward Bias condition, a negative voltage is applied to the Ntype material and a positive voltage is applied to the P-type material. If this external voltage becomes greater than the value of the potential barrier, approx. 0.7 volts for silicon and 0.3 volts for germanium, the potential barriers opposition will be overcome and current will start to flow. This is because the negative voltage pushes or repels electrons towards the junction giving them the energy to cross over and combine with the holes being pushed in the opposite direction towards the junction by the positive voltage. This results in a characteristics curve of zero current flowing up to this voltage point, called the "knee" on the static curves and then a high current flow through the diode with little increase in the external voltage .



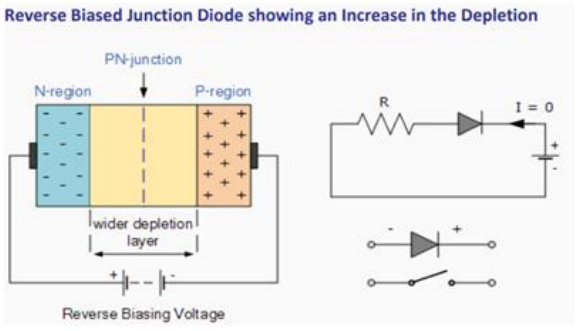
Diode Forward Bias

This condition represents the low resistance path through the PN junction allowing very large currents to flow

through the diode with only a small increase in bias voltage.

PN JUNCTION UNDER REVERSE BIAS CONDITION:

Reverse Biased Junction Diode When a diode is connected in a Reverse Bias condition, a positive voltage is applied to the N-type material and a negative voltage is applied to the P-type material. The positive voltage applied to the Ntype material attracts electrons towards the positive electrode and away from the junction, while the holes in the P-type end are also attracted away from the junction towards the negative electrode. The net result is that the depletion layer grows wider due to a lack of electrons and holes and presents a high impedance path, almost an insulator.



Diode Reverse Bias

This condition represents a high resistance value to the PN junction and practically zero current flows through the junction diode with an increase in bias voltage. However, a very small leakage

current does flow through the junction which can be measured in microamperes, (μA). One final point, if the reverse bias voltage Vr applied to the diode is increased to a sufficiently high enough value, it will cause the PN junction to overheat and fail due to the avalanche effect around the junction.

I-V CHARACTERISTICS AND THEIR TEMPERATURE DEPENDENCE

Diode terminal characteristics equation for diode junction current:.

$$I_D = I_0 (e^{\frac{v}{\eta v_T}} - 1)$$

η = empirical constant, 1 for Ge and 2 for Si

Where $V_T = KT/q$;

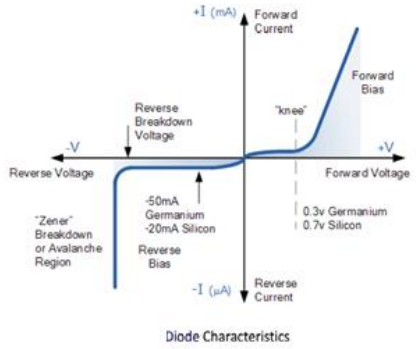
V_D_ diode terminal voltage, Volts

I_o _ temperature-dependent saturation current, μA

T _ absolute temperature of p-n junction, K

K _ Boltzmann's constant 1.38x 10 -23J/K)

q _ electron charge 1.6x10-19 C



Diode Characteristics

BREAK DOWN MECHANISMS

When an ordinary P-N junction diode is reverse biased, normally only very small reverse saturation current flows. This current is due to movement of minority carriers. It is almost independent of the voltage applied. However, if the reverse bias is increased, a point is reached when the junction breaks down and the reverse current increases abruptly. This current could be large enough to destroy the junction. If the reverse current is limited by means of a suitable series resistor, the power dissipation at the junction will not be excessive, and the device may be operated continuously in its breakdown region to its normal (reverse saturation) level. It is found that for a suitably designed diode, the breakdown voltage is very stable over a wide range of reverse currents. This quality gives the breakdown diode many useful applications as a voltage reference source.

The critical value of the voltage, at which the breakdown of a P-N junction diode occurs, is called the breakdown voltage. The breakdown voltage depends on the width of the depletion region, which, in turn, depends on the doping level. The junction offers almost zero resistance at the breakdown point.

There are two mechanisms by which breakdown can occur at a reverse biased P-N junction:

1. avalanche breakdown and

2. Zener breakdown.

Avalanche breakdown

The minority carriers, under reverse biased conditions, flowing through the junction acquire a kinetic energy which increases with the increase in reverse voltage. At a sufficiently high reverse voltage (say 5 V or more), the kinetic energy of minority carriers becomes so large that they

knock out electrons from the covalent bonds of the semiconductor material. As a result of collision, the liberated electrons in turn liberate more electrons and the current becomes very large leading to the breakdown of the crystal structure itself. This phenomenon is called the avalanche breakdown. The breakdown region is the knee of the characteristic curve. Now the current is not controlled by the junction voltage but rather by the external circuit.

Zener breakdown

Under a very high reverse voltage, the depletion region expands and the potential barrier increases leading to a very high electric field across the junction. The electric field will break some of the covalent bonds of the semiconductor atoms leading to a large number of free minority carriers, which suddenly increase the reverse current. This is called the Zener effect. The breakdown occurs at a particular and constant value of reverse voltage called the breakdown voltage, it is found that Zener breakdown occurs at electric field intensity of about 3 x 10^7 V/m.

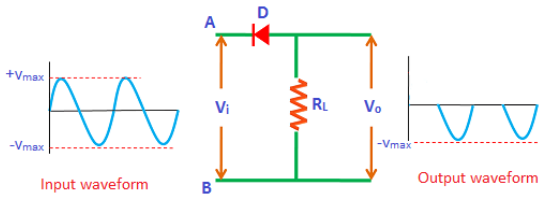
Diode characteristics with breakdown

Clipper Circuits

Electronic devices are very sensitive to voltage. If a large amplitude voltage is applied, it may permanently destroy the device. So, it is essential to protect the electronics devices.

The protection of the electronic devices can be achieved by using the clipper circuits.

A clipper is a device that removes either the positive half (top half) or negative half (bottom half), or both positive and negative halves of the input AC signal. In other words, a clipper is a device that limits the positive amplitude or negative amplitude or both positive and negative amplitudes of the input AC signal. In some cases, a clipper removes a small portion of the positive half cycle or negative half cycle or both positive and negative half cycles. In the below circuit diagram, the positive half cycles are removed by using the series positive clipper.



Series positive clipper

The clipper circuit does not contain energy storage elements such as capacitor but contains both linear and no-linear elements. The linear elements used in the clippers include resistors and the non-linear elements used in the clippers include diodes or transistors.

Types of clippers

The clipper circuits are generally categorized into three types: series clippers, shunt clippers and dual (combination) clippers. In series clippers, the diode is connected in series with the output load resistance. In shunt clippers, the diode is connected in parallel with the output load resistance.

The series clippers are again classified into four types: series positive clipper, series positive clipper with bias, series negative clipper and series negative clipper with bias. The shunt (parallel) clippers are again classified into four types: shunt positive clipper, shunt positive clipper with bias, shunt negative clipper, and shunt negative clipper with bias.

The various types of clippers are as follows:

- Series positive clipper
- Series positive clipper with bias
- Series negative clipper
- Series negative clipper with bias
- Shunt positive clipper
- Shunt positive clipper with bias
- Shunt negative clipper
- Shunt negative clipper with bias

Series positive clipper

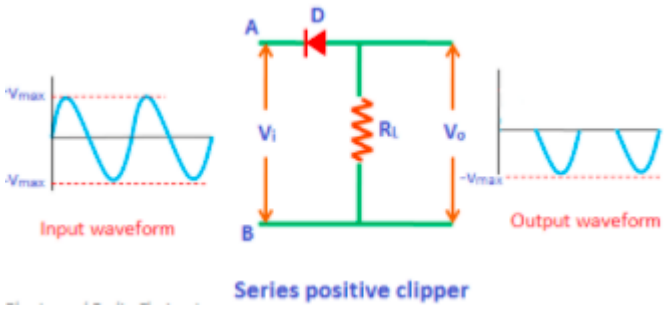
In series positive clipper, the positive half cycles of the input AC signal is removed.

If the diode is arranged in such a way that the arrowhead of the diode points towards the input and the diode is in series with the output load resistance, then the clipper is said to be a series positive clipper.

In the circuit diagram, the diode D is connected in series with the output load resistance RL and the arrowhead of the diode is pointing towards the input. So the circuit is said to be a series positive clipper.

The vertical line in the diode symbol represents the cathode (n-side) and the opposite end represents the anode (p-side).

During positive half cycle:



Series positive clipper

During the positive half cycle, terminal A is positive and terminal B is negative. That means the positive terminal A is connected to n-side and the negative terminal B is connected to p-side of the diode. As we already know that if the positive terminal is connected to n-side and the negative. Therefore, the diode D is reverse biased during the positive half cycle.

During reverse biased condition, no current flows through the diode. So the positive half cycle is blocked or removed at the output.

During negative half cycle:

During the negative half cycle, terminal A is negative and terminal B is positive.. Therefore, the diode D is forward biased during the negative half cycle.

During forward biased condition, electric current flows through the diode. So the negative half cycle is allowed at the output.

Thus, a series of positive half cycles are completely removed at the output.

Series positive clipper with bias

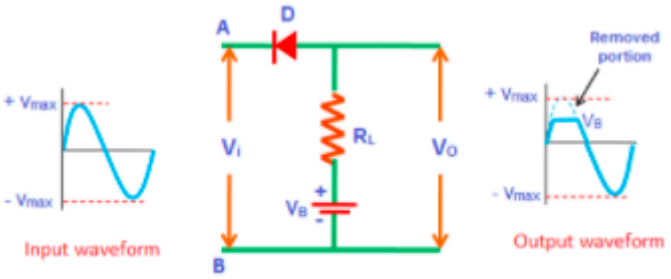
Sometimes it is desired to remove a small portion of positive or negative half cycles. In such cases, the biased clippers are used.

The construction of the series positive clipper with bias is almost similar to the series positive clipper. The only difference is an extra element called battery is used in series positive clipper with bias.

Series positive clipper with positive bias

During positive half cycle:

During the positive half cycle, terminal A is positive and terminal B is negative. That means the positive terminal is connected to n-side and the negative terminal is connected to p-side. Therefore, the diode is reverse biased by the input supply voltage Vi.



Series positive clipper with positive bias

However, we are supplying the voltage from another source called battery. Therefore, the diode is forward biased by the battery voltage V_B.

That means the diode is reverse biased by the input supply voltage (Vi) and forward biased by the battery voltage (V_B).

Initially, the input supply voltage Vi is less than the battery voltage V_B ($Vi < V_B$). So the battery voltage dominates the input supply voltage. Hence, the diode is forward biased by the battery voltage and allows electric current through it. As a result, the signal appears at the output.

When the input supply voltage Vi becomes greater than the battery voltage V_B, the diode D is reverse biased. So no current flows through the diode. As a result, input signal does not appear at the output.

Thus, the clipping (removal of a signal) takes place during the positive half cycle only when the input supply voltage becomes greater than the battery voltage.

During negative half cycle:

During the negative half cycle, terminal A is negative and terminal B is positive. So the diode is forward biased by both battery voltage V_B and input supply voltage V_i.

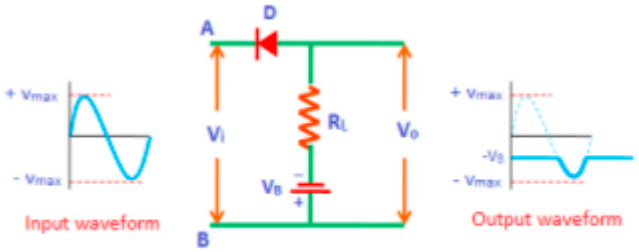
That means, during the negative half cycle, it doesn't matter whether the input supply voltage is greater or less than the battery voltage, the diode always remains forward biased. So the complete negative half cycle appears at the output.

Thus, the series positive clipper with positive bias removes a small portion of positive half cycles.

Series positive clipper with negative bias

During positive half cycle:

During the positive half cycle, the diode D is reverse biased by both input supply voltage Vi and battery voltage VB. So no signal appears at the output during the positive half cycle. Therefore, the complete positive half cycle is removed.



Series positive clipper with negative bias

During negative half cycle:

During the negative half cycle, the diode is forward biased by the input supply voltage Vi and reverse biased by the battery voltage VB. However, initially, the battery voltage VB dominates the input supply voltage Vi. So the diode remains to be reverse biased until the Vi becomes greater than VB. When the input supply voltage Vi becomes greater than the battery voltage VB, the diode is forward biased by the input supply voltage Vi. So the signal appears at the output.

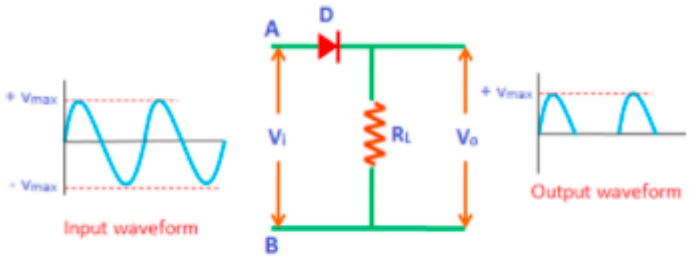
Series negative clipper

In series negative clipper, the negative half cycles of the input AC signal is removed at the output. The circuit construction of the series negative clipper is shown in the figure.

If the diode is arranged in such a way that the arrowhead of the diode points towards the output and the diode is in series with the output load resistance, then the clipper is said to be a series negative clipper.

During positive half cycle:

During the positive half cycle, terminal A is positive and terminal B is negative.. Therefore, the diode D is forward biased during the positive half cycle.



Series negative clipper

During forward biased condition, electric current flows through the diode. So the positive half cycle is allowed at the output. Therefore, a series of positive half cycles appears at the output.

During negative half cycle:

During the negative half cycle, the terminal A is negative and the terminal B is positive. d. Therefore, the diode D is reverse biased during the negative half cycle.

During reverse biased condition, no current flows through the diode. So the negative half cycle is completely blocked or removed at the output. In other words, a series of negative half cycles are removed at the output.

Series negative clipper with bias

Sometimes it is desired to remove a small portion of positive or negative half cycles of the input AC signal. In such cases, the biased clippers are used.

The construction of the series negative clipper with bias is almost similar to the series negative clipper. The only difference is an extra element called battery is used in series negative clipper with bias.

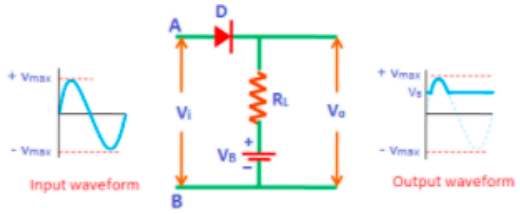
Series negative clipper with positive bias

During positive half cycle:

During the positive half cycle, terminal A is positive and terminal B is negative. That means the diode is said to be forward biased. However, we are also supplying the voltage from another source called battery. As shown in the figure, the positive terminal of the battery is connected to n-side and the negative terminal of the battery is connected to p-side of the diode.

That means the diode is forward biased by input supply voltage Vi and reverse biased by battery voltage VB. Initially, the battery voltage is greater than the input supply voltage. Hence, the diode is reverse biased and does not allow electric current. Therefore, no signal appears at the output.

When the input supply voltage Vi becomes greater than the battery voltage VB, the diode is forward biased and allows electric current. As a result, the signal appears at the output.



Series negative clipper with positive bias

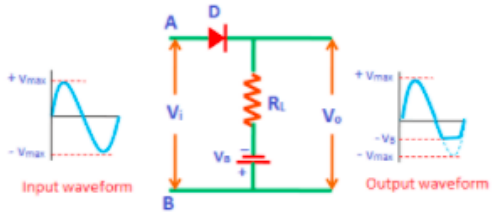
During negative half cycle:

During the negative half cycle, the diode is reverse biased by both input supply voltage Vi and battery voltage VB. So it doesn't matter whether the input supply voltage is greater or less than the battery voltage VB, the diode always remains reverse biased. Therefore, during the negative half cycle, no signal appears at the output.

Series negative clipper with negative bias

During positive half cycle:

During the positive half cycle, the diode D is forward biased by both input supply voltage Vi and the battery voltage VB. So it doesn't matter whether the input supply voltage is greater or less than battery voltage VB, the diode always remains forward biased. Therefore, during the positive half cycle, the signal appears at the output.



Series negative clipper with negative bias

During negative half cycle:

During the negative half cycle, the diode D is reverse biased by the input supply voltage Vi and forward biased by the battery voltage VB. Initially, the input supply voltage Vi is less than the battery voltage VB. So the diode is forward biased by the battery voltage VB. As a result, the signal appears at the output.

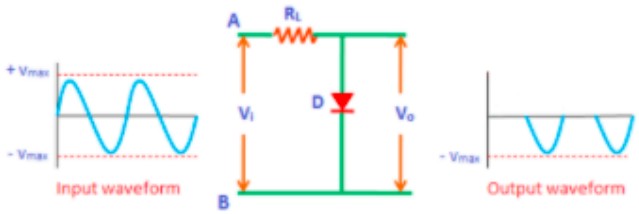
When the input supply voltage Vi becomes greater than the battery voltage VB, the diode will become reverse biased. As a result, no signal appears at the output.

Shunt positive clipper

In shunt clipper, the diode is connected in parallel with the output load resistance. The operating principles of the shunt clipper are nearly opposite to the series clipper.

The series clipper passes the input signal to the output load when the diode is forward biased and blocks the input signal when the diode is reverse biased.

The shunt clipper on the other hand passes the input signal to the output load when the diode is reverse biased and blocks the input signal when the diode is forward biased.

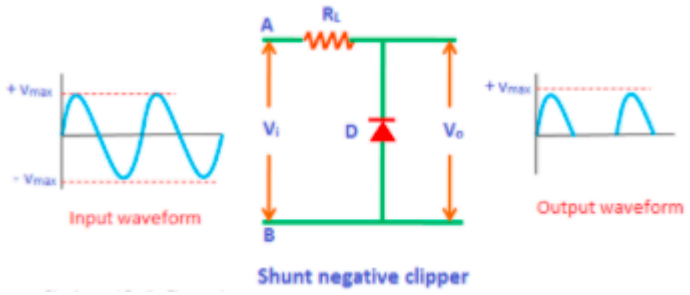


Shunt positive clipper

In shunt positive clipper, during the positive half cycle the diode is forward biased and hence no output is generated. On the other hand, during the negative half cycle the diode is reverse biased and hence the entire negative half cycle appears at the output.

Shunt negative clipper

In shunt negative clipper, during the positive half cycle the diode is reverse biased and hence the entire positive half cycle appears at the output. On the other hand, during the negative half cycle the diode is forward biased and hence no output signal is generated.



Shunt negative clipper

Applications of clippers

- Clippers are commonly used in power supplies.
- Used in TV transmitters and Receivers
- They are employed for different wave generation such as square, rectangular, or trapezoidal waves.
- Series clippers are used as noise limiters in FM transmitters.

Clamper circuits

A clamper is an electronic circuit that changes the DC level of a signal to the desired level without changing the shape of the applied signal. In other words, the clamper circuit moves the whole signal up or down to set either the positive peak or negative peak of the signal at the desired level.

Types of clampers

Clamper circuits are of three types:

- Positive clampers
- Negative clampers
- Biased clampers

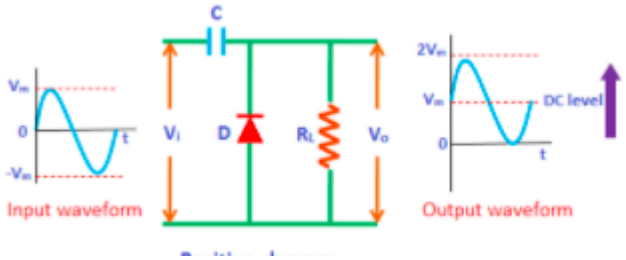
Positive clamper

The positive clamper is made up of a voltage source Vi, capacitor C, diode D, and load resistor RL. In the below circuit diagram, the diode is connected in parallel with the output load. So the positive clamper passes the input signal to the output load when the diode is reverse biased and blocks the input signal when the diode is forward biased.

During the negative half cycle of the input AC signal, the diode is forward biased and hence no signal appears at the output.

During negative half cycle:

During the negative half cycle of the input AC signal, the diode is forward biased and hence no signal appears at the output. In forward biased condition, the diode allows electric current through it. This current will flows to the capacitor and charges it to the peak value of input voltage Vm. The capacitor charged in inverse polarity (positive) with the input voltage. As input current or voltage decreases after attaining its maximum value -Vm, the capacitor holds the charge until the diode remains forward biased.



During positive half cycle:

During the positive half cycle of the input AC signal, the diode is reverse biased and hence the signal appears at the output. In reverse biased condition, the diode does not allow electric current through it. So the input current directly flows towards the output.

When the positive half cycle begins, the diode is in the non-conducting state and the charge stored in the capacitor is discharged (released). Therefore, the voltage appeared at the output is equal to the sum of the voltage stored in the capacitor (Vm) and the input voltage (Vm) { I.e. Vo = Vm+ Vm = 2Vm} which have the same polarity with each other. As a result, the signal shifted upwards.

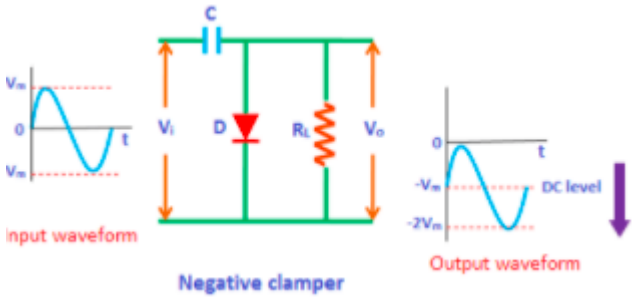
The peak to peak amplitude of the input signal is 2Vm, similarly the peak to peak amplitude of the output signal is also 2Vm. Therefore, the total swing of the output is same as the total swing of the input.

The basic difference between the clipper and clamper is that the clipper removes the unwanted portion of the input signal whereas the clamper moves the input signal upwards or downwards.

Negative clamper

During positive half cycle:

During the positive half cycle of the input AC signal, the diode is forward biased and hence no signal appears at the output. In forward biased condition, the diode allows electric current through it. This current will flows to the capacitor and charges it to the peak value of input voltage in inverse polarity -Vm. As input current or voltage decreases after attaining its maximum value Vm, the capacitor holds the charge until the diode remains forward biased.



During the positive half cycle of the input AC signal, the diode is forward biased and hence no signal appears at the output.

During negative half cycle:

During the negative half cycle of the input AC signal, the diode is reverse biased and hence the signal appears at the output. In reverse biased condition, the diode does not allow electric current through it. So the input current directly flows towards the output.

When the negative half cycle begins, the diode is in the non-conducting state and the charge stored in the capacitor is discharged (released). Therefore, the voltage appeared at the output is equal to the sum of the voltage stored in the capacitor (-Vm) and the input voltage (-Vm) {I.e. Vo = -Vm- Vm = -2Vm} which have the same polarity with each other. As a result, the signal shifted downwards.

Voltage Multiplier

Voltage multiplier definition

The voltage multiplier is an electronic circuit that delivers the output voltage whose amplitude (peak value) is two, three, or more times greater than the amplitude (peak value) of the input voltage.

The voltage multiplier is an AC-to-DC converter, made up of diodes and capacitors that produce a high voltage DC output from a low voltage AC input.

Types of voltage multipliers

Voltage multipliers are classified into four types:

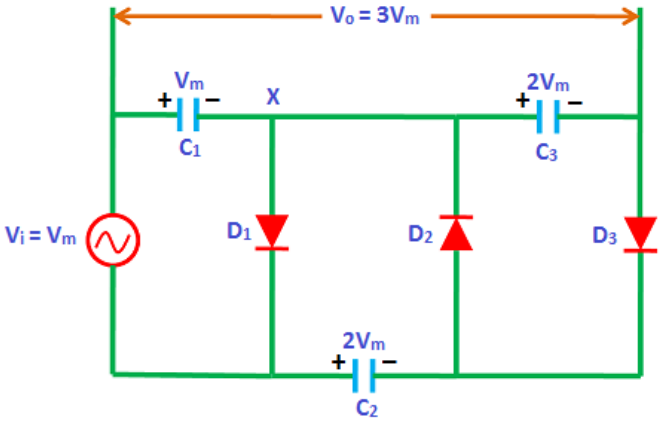
- Voltage doubler
- Voltage Tripler
- Voltage quadrupler

Voltage Tripler

The voltage tripler can be obtained by adding one more diode-capacitor stage to the half-wave voltage doubler circuit.

During first positive half cycle:

During the first positive half cycle of the input AC signal, the diode D_1 is forward biased whereas diodes D_2 and D_3 are reverse biased. Hence, the diode D_1 allows electric current through it. This current will flows to the capacitor C_1 and charges it to the peak value of the input voltage I.e. V_m.



Voltage Tripler

During negative half cycle:

During the negative half cycle, diode D_2 is forward biased whereas diodes D_1 and D_3 are reverse biased. Hence, the diode D_2 allows electric current through it. This current will flows to the capacitor C_2 and charges it. The capacitor C_2 is charged to twice the peak voltage of the input signal ($2V_m$). This is because the charge (V_m) stored in the capacitor C_1 is discharged during the negative half cycle.

Therefore, the capacitor C_1 voltage (V_m) and the input voltage (V_m) is added to the capacitor C_2 I.e Capacitor voltage + input voltage = $V_m + V_m = 2V_m$. As a result, the capacitor C_2 charges to $2V_m$.

During second positive half cycle:

During the second positive half cycle, the diode D_3 is forward biased whereas diodes D_1 and D_2 are reverse biased. Diode D_1 is reverse biased because the voltage at X is negative due to charged voltage V_m, across C_1 and diode D_2 is reverse biased because of its orientation. As a result, the voltage ($2V_m$) across capacitor C_2 is discharged. This charge will flow to the capacitor C_3 and charges it to the same voltage $2V_m$.

The capacitors C_1 and C_3 are in series and the output voltage is taken across the two series connected capacitors C_1 and C_3. The voltage across capacitor C_1 is V_m and

capacitor C_3 is $2V_m$. So the total output voltage is equal to the sum of capacitor C_1 voltage and capacitor C_3 voltage I.e. $C_1 + C_3 = V_m + 2V_m = 3V_m$.

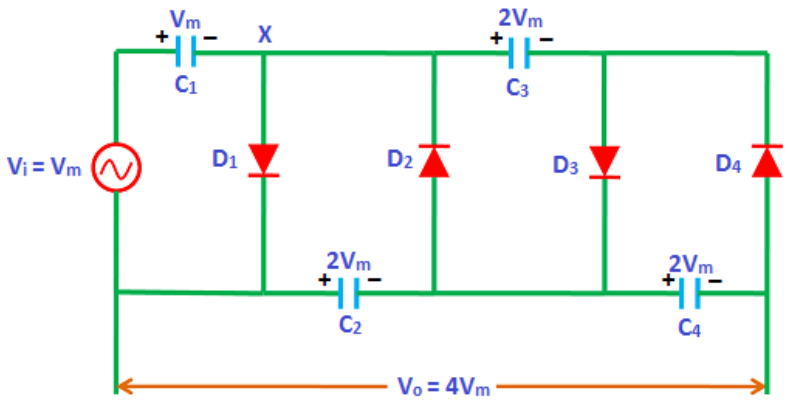
Therefore, the total output voltage obtained in voltage tripler is $3V_m$ which is three times more than the applied input voltage.

Voltage quadrupler

The voltage quadrupler can be obtained by adding one more diode-capacitor stage to the voltage tripler circuit.

During first positive half cycle:

During the first positive half cycle of the input AC signal, the diode D_1 is forward biased whereas diodes D_2, D_3 and D4 are reverse biased. Hence, the diode D_1 allows electric current through it. This current will flows to the capacitor C_1 and charges it to the peak value of the input voltage I.e. V_m.



Voltage Quadrupler

During first negative half cycle:

During the first negative half cycle, diode D_2 is forward biased and diodes D_1, D_3 and D_4 are reverse biased. Hence, the diode D_2 allows electric current through it. This current will flows to the capacitor C_2 and charges it. The capacitor C_2 is charged to twice the peak voltage of the input signal ($2V_m$). This is because the charge (V_m) stored in the capacitor C_1 is discharged during the negative half cycle.

Therefore, the capacitor C_1 voltage (V_m) and the input voltage (V_m) is added to the capacitor C_2 I.e Capacitor voltage + input voltage = $V_m + V_m = 2V_m$. As a result, the capacitor C_2 charges to $2V_m$.

During second positive half cycle:

During the second positive half cycle, the diode D_3 is forward biased and diodes D_1, D_2 and D_4 are reverse biased. Diode D_1 is reverse biased because the voltage at X

is negative due to charged voltage V_m, across C_1 and, diode D_2 and D_4 are reverse biased because of their orientation. As a result, the voltage ($2V_m$) across capacitor C_2 is discharged. This charge will flow to the capacitor C_3 and charges it to the same voltage $2V_m$.

During second negative half cycle:

During the second negative half cycle, diodes D_2 and D_4 are forward biased whereas diodes D_1 and D_3 are reverse biased. As a result, the charge ($2V_m$) stored in the capacitor C_3 is discharged. This charge will flow to the capacitor C_4 and charges it to the same voltage ($2V_m$).

The capacitors C_2 and C_4 are in series and the output voltage is taken across the two series connected capacitors C_2 and C_4. The voltage across capacitor C_2 is $2V_m$ and capacitor C_4 is $2V_m$. So the total output voltage is equal to the sum of capacitor C_2 voltage and capacitor C_4 voltage I.e. $C_2 + C_4 = 2V_m + 2V_m = 4V_m$.

Therefore, the total output voltage obtained in voltage quadrupler is $4V_m$ which is four times more than the applied input voltage.

Applications of voltage multipliers

Voltage multipliers are used in:

- Cathode Ray Tubes (CRTs)
- Traveling wave tubes
- Laser systems
- X-ray systems
- LCD backlighting
- hv power supplies
- Power supplies
- Oscilloscopes
- Particle accelerators
- Ion pumps
- Copy machines

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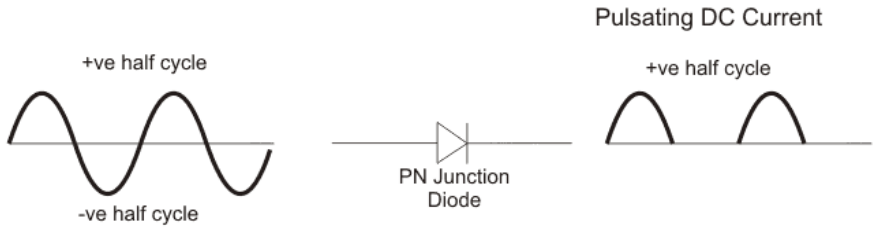
Rectifier

A rectifier is a device that converts alternating current (AC) to direct current (DC). It is done by using a diode or a group of diodes. Half wave rectifiers use one diode, while a full wave rectifier uses multiple diodes.
The working of a half wave rectifier takes advantage of the fact that diodes only allow current to flow in one direction.

Half Wave Rectifier Theory

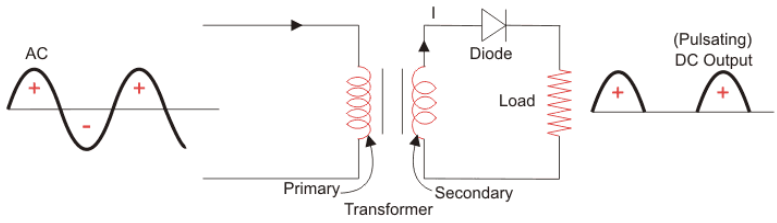
The diagram below illustrates the basic principle of a half-wave rectifier. When a standard AC waveform is passed through a half-wave rectifier, only half of the AC waveform remains. Half-wave rectifiers only allow one half-cycle (positive or negative half-cycle) of the AC voltage through and will block the other half-cycle on the DC side, as seen below.



Half-wave rectifier circuit consists of 3 main parts:

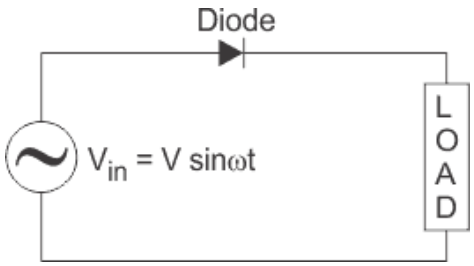
1. A transformer
2. A resistive load
3. A diode

First, a high AC voltage is applied to the to the primary side of the step-down transformer and we will get a low voltage at the secondary winding which will be applied to the diode.



During the positive half cycle of the AC voltage, the diode will be forward biased and the current flows through the diode. During the negative half cycle of the AC voltage, the diode will be reverse biased and the flow of current will be blocked..

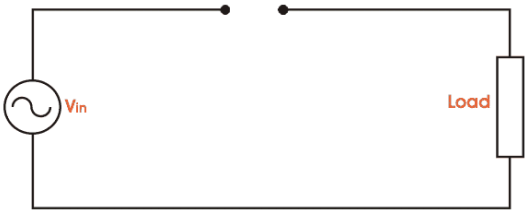
. If we replace the secondary transformer coils with a source voltage, we can simplify the circuit diagram of the half-wave rectifier as:



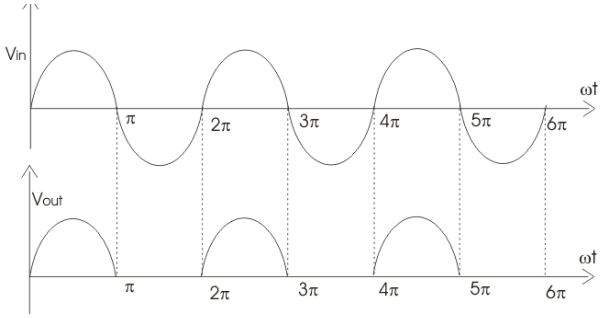
For the positive half cycle of the AC source voltage, the equivalent circuit effectively becomes:

This is because the diode is forward biased, and is hence allowing current to pass through. So we have a closed circuit.

But for the negative half cycle of the AC source voltage, the equivalent circuit becomes:



Because the diode is now in reverse bias mode, no current is able to pass through it. As such, we now have an open circuit. Since current can not flow through to the load during this time, the output voltage is equal to zero.



The graph above actually shows a positive half wave rectifier. This is a half-wave rectifier which only allows the positive half-cycles through the diode, and blocks the negative half-cycle.

Mathematical Analysis:

Let $V_i = V_p \sin \omega t \quad ---(1)$ be the input voltage to the rectifier, where $\mathbf{V_p}$ is the peak input voltage. While the diode is conducting, let $\mathbf{i_d}$ be the current flowing through the circuit and $\mathbf{V_d}$ be the voltage across the diode.

For a half wave rectifier, we have

$$I_d = \begin{cases} I_m \sin \omega t & \text{for } 0 < \omega t < \pi \\ 0 & \text{for } \pi < \omega t < 2\pi \end{cases}$$

Average dc Value of a Half-wave rectifier.

The average of all the instantaneous values of an alternating voltage and currents over one complete cycle is called **Average Value. It is calculated as,**

$$I_{dc} = \frac{1}{2\pi} \int_0^{2\pi} I_d \, d(\omega t)$$

$$= \frac{1}{2\pi} \left[\int_0^{\pi} i_d \, d(\omega t) + \int_{\pi}^{2\pi} i_d \, d(\omega t) \right]$$

$$= \frac{1}{2\pi} \int_0^{\pi} i_d \, d(\omega t)$$

[$\because$ id=0 in the range π to 2π]

$$= \left(\frac{1}{2\pi} \right) \int_0^{\pi} I_m \sin \omega t \; d(\omega t)$$

$$= \frac{I_m}{2\pi} \left[-\cos(\omega t) \right]_0^{\pi}$$

$$\therefore I_{dc} = \frac{I_m}{\pi}$$

RMS value of output current($\mathbf{I_{rms}}$):

$$I_{rms} = \sqrt{\frac{1}{2\pi} \int_0^{2\pi} i_d^2 \, d(\omega t)}$$

$$= \sqrt{\frac{1}{2\pi} \left[\int_0^{\pi} i_d^2 \, d(\omega t) + \int_{\pi}^{2\pi} i_d^2 \, d(\omega t) \right]}$$

$$= \sqrt{\frac{1}{2\pi} \int_0^{\pi} i_d^2 \, d(\omega t)}$$

$$= \sqrt{\frac{1}{2\pi}\int_0^{\pi} I_m^2 \sin^2 \omega t \, d(\omega t)}$$

$$= \sqrt{\frac{I_m^2}{2\pi}\left[\frac{\omega t}{2} - \frac{\sin 2\omega t}{4}\right]_0^{\pi}} \qquad [\because \text{ id=0 in the range } \pi \text{ to } 2\pi]$$

$$= \sqrt{\frac{I_m^2}{2\pi}\frac{\pi}{2}}$$

$$= \sqrt{\frac{I_m^2}{4}}$$

$$\therefore I_{rms} = \frac{I_m}{2}$$

$$\therefore I_{rms} > I_{dc}$$

Ripple Factor of Half Wave Rectifier

'Ripple' is the unwanted AC component remaining when converting the AC voltage waveform into a DC waveform. Even though we try out best to remove all AC components, there is still some small amount left on the output side which pulsates the DC waveform. This undesirable AC component is called 'ripple'.

For a Half Wave Rectifier

$$Ripple\ factor(r) = \frac{(I_{rms}^2 - I_{dc}^2)}{I_{dc}} = 1.21$$

Efficiency of Half Wave Rectifier

Rectifier efficiency (η) is the ratio between the output DC power and the input AC power. The formula for the efficiency is equal to:

$$\eta = \frac{P_{dc}}{P_{ac}}$$

The efficiency of a half wave rectifier is equal to 40.6% (i.e. η_{max} = 40.6%)

Peak Inverse Voltage (PIV)

It is the maximum voltage that the diode can withstand during reverse bias condition. If a voltage is applied more than the PIV, the diode will be destroyed.V = Vm

Applications of Half Wave Rectifier

Half wave rectifiers are not as commonly used as full-wave rectifiers.

- For rectification applications

- For signal demodulation applications
- For signal peak applications
-

Advantages of Half Wave Rectifier

The main advantage of half-wave rectifiers is in their simplicity. As they don't require as many components, they are simpler and cheaper to setup and construct.

As such, the main advantages of half-wave rectifiers are:

- Simple (lower number of components)
- Cheaper up front cost (as their is less equipment. Although there is a higher cost over time due to increased power losses)

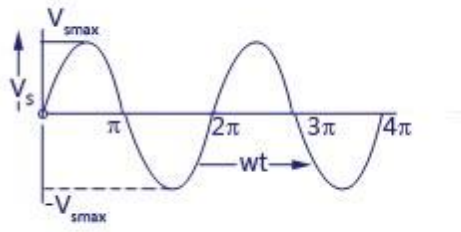
Disadvantages of Half Wave Rectifier

The disadvantages of half-wave rectifiers are:

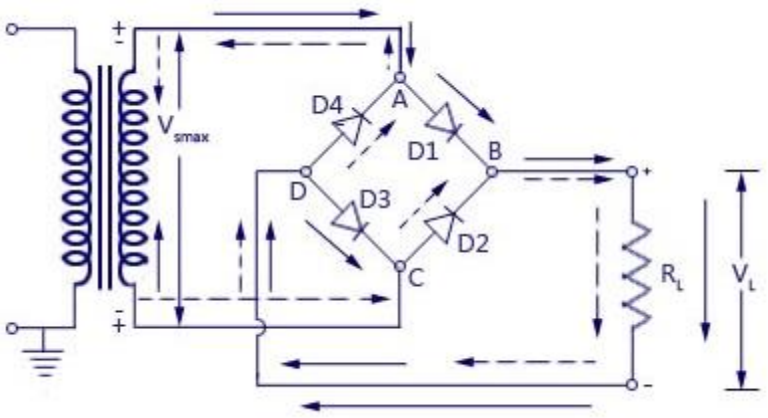
- They only allow a half-cycle through per sinewave, and the other half-cycle is wasted. This leads to power loss.
- They produces a low output voltage.
- The output current we obtain is not purely DC, and it still contains a lot of ripple (i.e. it has a high ripple factor)

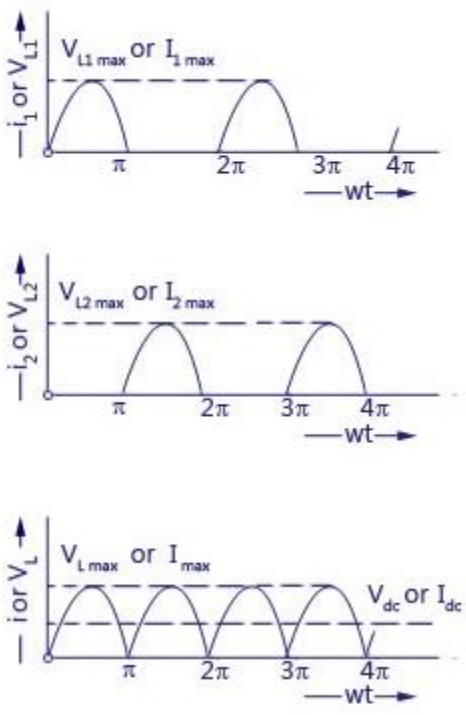
Full Wave Rectifiers

The working & operation of a full wave bridge rectifier is pretty simple. In the circuit diagram, 4 diodes are arranged in the form of a bridge. The transformer secondary is connected to two diametrically opposite points of the bridge at points A & C. The load resistance R_L is connected to bridge through points B and D.



Input Voltage Waveform





Rectified Output Voltage/Current Waveforms

BRIDGE RECTIFIER

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During the first half cycle

During the first half cycle of the input voltage, the upper end of the transformer secondary winding is positive with respect to the lower end. Thus during the first half cycle diodes D1 and D_3 are forward biased and current flows through arm AB, enters the load resistance R_L, and returns back flowing through arm DC. During this half of each input cycle, the diodes D_2 and D_4 are reverse biased and current is not allowed to flow in arms AD and BC.

During the second half cycle

During the second half cycle of the input voltage, the lower end of the transformer secondary winding is positive with respect to the upper end. Thus diodes D_2 and D_4 become forward biased and current flows through arm CB, enters the load resistance R_L, and returns back to the source flowing through arm DA. The flow of current has been shown by dotted arrows in the figure. Thus the direction of flow of current through the load resistance R_L remains the same during both half cycles of the input supply voltage.

Characteristics of full wave rectifier

Ripple factor

The ripple factor is used to measure the amount of ripples present in the output DC signal. A high ripple factor indicates a high pulsating DC signal while a low ripple factor indicates a low pulsating DC signal.

Ripple factor is defined as the ratio of ripple voltage to the pure DC voltage

The ripple factor is given by

$$\gamma = \sqrt{\left(\frac{V_{rms}}{V_{DC}}\right)^2 - 1}$$

Finally, we get

$$\gamma = 0.48$$

Rectifier efficiency

Rectifier efficiency indicates how efficiently the rectifier converts AC into DC. A high percentage of rectifier efficiency indicates a good rectifier while a low percentage of rectifier efficiency indicates an inefficient rectifier.

Rectifier efficiency is defined as the ratio of DC output power to the AC input power.

It can be mathematically written as

$$\eta = \text{output } P_{DC} / \text{input } P_{AC}$$

The rectifier efficiency of a full wave rectifier is 81.2%.

The rectifier efficiency of a full wave rectifier is twice that of the half wave rectifier. So the full wave rectifier is more efficient than a half wave rectifier

Peak inverse voltage (PIV)

Peak inverse voltage or peak reverse voltage is the maximum voltage a diode can withstand in the reverse bias condition. If the applied voltage is greater than the peak inverse voltage, the diode will be permanently destroyed.

The peak inverse voltage (PIV) = $2V_{smax}$

DC output current

At the output load resistor R_L, both the diode D_1 and diode D_2 currents flow in the same direction. So the output current is the sum of D_1 and D_2 currents.

The current produced by D_1 is I_{max} / π and the current produced by D_2 is I_{max} / π.

So the output current $I_{DC} = 2I_{max} / \pi$

Where,

I_{max} = maximum DC load current

DC output voltage

The DC output voltage appeared at the load resistor R_L is given as

$V_{DC} = 2V_{max} / \pi$

Where,

V_{max} = maximum secondary voltage

Root mean square (RMS) value of load current I_{RMS}

The root mean square (RMS) value of load current in a full wave rectifier is

$$I_{RMS} = \frac{I_m}{\sqrt{2}}$$

Root mean square (RMS) value of the output load voltage V_{RMS}

The root mean square (RMS) value of output load voltage in a full wave rectifier is

$$V_{RMS} = I_{RMS} R_L = \frac{I_m}{\sqrt{2}} R_L$$

Advantages of Full Wave Rectifiers

- Full wave rectifiers have higher rectifying efficiency than half-wave rectifiers. This means that they convert AC to DC more efficiently.
- They have low power loss because no voltage signal is wasted in the rectification process.
- The output voltage of centre-tapped full wave rectifier has lower ripples than a halfwave rectifiers.

Disadvantages of Full Wave Rectifiers

- The centre-tapped rectifier is more expensive than half-wave rectifier and tends to occupy a lot of space.

$$= \frac{40.6\ R_L}{R_f + R_L}\ \%$$

If $R_f << R_L$, $\eta = 40.6\%$
If $R_f = R_L$, $\eta = 20.3\%$

Ripple factor(**r**):
At the output of half wave rectifier, periodically varying components are still present even though we have achieved a unidirectional current. Filters are used in the rectifier to reduce the varying components. A measure of the varying component is given by the ripple factor as follows:

$$r = \frac{I'_{rms}}{I_{dc}} = \frac{E'_{rms}}{E_{dc}}$$

where I'_{rms} and E'_{rms} represent the RMS value of ripple current and voltage respectively.

Instantaneous value of ripple current $I' = i_d - I_{dc}$

where I'_{rms} and E'_{rms} represent the RMS value of ripple current and voltage respectively.

Instantaneous value of ripple current $I' = i_d - I_{dc}$

$$\therefore I'_{rms} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} i_d'^2(\omega t)}$$

$$= \sqrt{\frac{1}{2\pi}\int_0^{2\pi} (i_d - I_{dc})^2\, d(\omega t)}$$

$$= \sqrt{\frac{1}{2\pi}\int_0^{2\pi} (i_d^2 - 2 i_d I_{dc} + I_{dc}^2)\, d(\omega t)}$$

Using equations

$$I_{dc} = \frac{1}{2\pi}\int_0^{2\pi} I_d\, d(\omega t) \quad \& \quad I_{rms} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} i_d^2\, d(\omega t)}$$

we have,

$$I'_{rms} = \sqrt{(I_{rms}^2 - 2I_{dc}^2 + I_{dc}^2)}$$

$$= \sqrt{(I_{rms}^2 - I_{dc}^2)}$$

Ripple factor is given by

$$r = \frac{I'_{rms}}{I_{dc}}$$

$$= \sqrt{\frac{(I_{rms}^2 - I_{dc}^2)}{I_{dc}^2}}$$

$$= \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1}$$

$$= \sqrt{\left(\frac{I_m/2}{I_m/\pi}\right)^2 - 1}$$

$$\therefore r = \sqrt{\left(\frac{\pi}{2}\right)^2 - 1}$$

$$\therefore r = \sqrt{\left(\frac{\pi}{2}\right)^2 - 1}$$

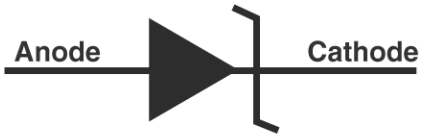
$$\therefore r = 1.21$$

The above calculation shows that the RMS value of the ripple exceeds that of the DC potential of the output. This shows that the half wave rectifier without a filter is relatively a poor device for converting AC into DC.

Peak Inverse Voltage:
It is defined as the maximum voltage applied across the diode when the diode is reverse biased. In the case of half wave rectifier, the maximum voltage across the diode when it is not conducting is equal to V_p, the peak

Zener Diode

A Zener diode is a heavily doped semiconductor device that is designed to operate in the reverse direction.



Zener Diode Specifications

- **Zener/Breakdown Voltage** – The Zener or the reverse breakdown voltage ranges from 2.4 V to 200 V, sometimes it can go up to 1 kV while the maximum for the surface-mounted device is 47 V.
  - **Current Iz (max)** – It is the maximum current at the rated Zener Voltage

    (Vz – 200μA to 200 A)

How does a Zener Diode work in reverse bias?

A Zener diode operates just like a normal diode when it is forward-biased. However, when connected in reverse biased mode, a small leakage current flows through the diode. As the reverse voltage increases to the predetermined breakdown voltage (Vz), current starts flowing through the diode. The current increases to a maximum, which is determined by the series resistor, after which it stabilizes and remains constant over a wide range of applied voltage.

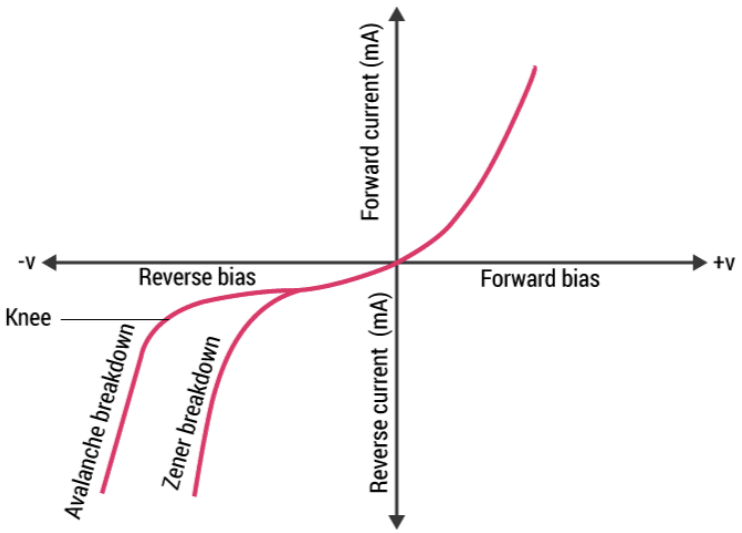
V-I Characteristics of Zener Diode

The diagram given below shows the V-I characteristics of the Zener diode.

The V-I characteristics of a Zener diode can be divided into two parts as follows:
(i) Forward Characteristics
(ii) Reverse Characteristics

Forward Characteristics of Zener Diode

The first quadrant in the graph represents the forward characteristics of a Zener diode. From the graph, we understand that it is almost identical to the forward characteristics of any other P-N junction diode.



When reverse-biased voltage is applied to a Zener diode, it allows only a small amount of leakage current until the voltage is less than Zener voltage.

Reverse Characteristics of Zener Diode

When a reverse voltage is applied to a Zener voltage, initially a small reverse saturation current Io flows across the diode. This current is due to thermally generated minority carriers. As the reverse voltage is increased, at a certain value of reverse voltage, the reverse current increases drastically and sharply. This is an indication that the breakdown has occurred. We call this voltage breakdown voltage or Zener voltage and it is denoted by Vz.

Zener Breakdown in Zener Diode

When the applied reverse bias voltage reaches closer to the Zener voltage, the electric field in the depletion region gets strong enough to pull electrons from their valence band. The valence electrons that gain sufficient energy from the strong electric field of the depletion region break free from the parent atom. At the Zener breakdown region, a small increase in the voltage results in the rapid increase of the electric current.

Advantages of zener diode

- Power dissipation capacity is very high
- High accuracy
- Small size

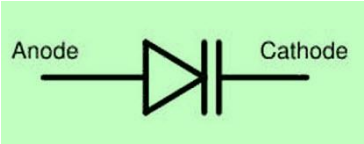
- Low cost

Applications of zener diode

- It is normally used as voltage reference
- Zener diodes are used in voltage stabilizers or shunt regulators.
- Zener diodes are used in switching operations
- Zener diodes are used in clipping and clamping circuits.
- Zener diodes are used in various protection circuits

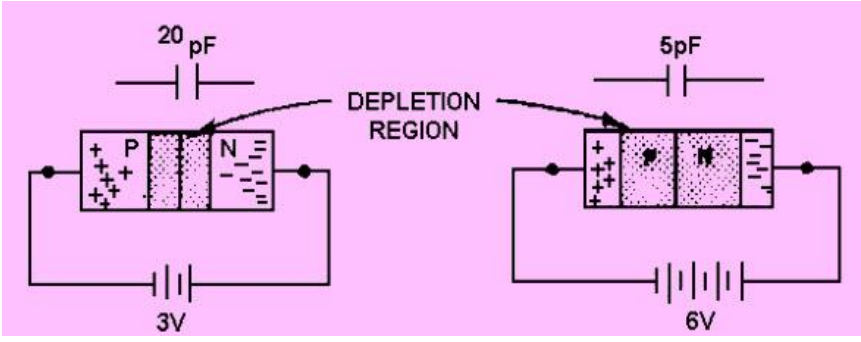
Varactor Diode or Varicap Diode

Varactor diode is one kind of semiconductor microwave solid-state device and the applications of this diode mainly involve in where variable capacitance is preferred which can be accomplished by controlling voltage. These diodes are also named as varicap diodes. Even though the outcome of the variable capacitance can be shown by the normal P-N junction diodes, but these diodes are chosen for giving the desired capacitance changes as they are special types of diodes.



Working of a Varactor Diode:

When the diode is in the reverse biased mode, where the two regions of P-type and N-type are able to conduct and thus can be treated as two terminals. The depletion area between the P-type & N-type regions can be considered as the insulating dielectric. Therefore, it is similar to the capacitor shown above.



Working of a Varactor Diode

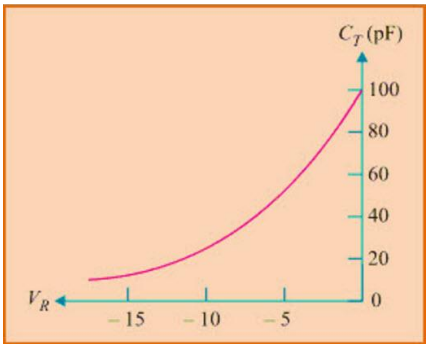
The volume of the depletion region of the diode varies with change in reverse bias. If the reverse voltage of the diode is increased, then the size of the depletion region

increases. Likewise, if the reverse voltage of the Varactor diode is decreased, then the size of the depletion region decreases. Hence, by changing the reverse bias of the diode the capacitance can be changed.

Characteristics of Varactor Diode:

The characteristics of Varactor diode have the following:

- These diodes significantly generate less noise compared to other diodes.
- The cost of these diodes is available at lower and more reliable also.
- These diodes are very small in size and very lightweight.
- There is no use when it is operated in forwarding bias.
- In reverse bias mode, the Varactor diode enhances the capacitance as shown in the graph below.



$$C_T = \frac{\varepsilon A}{W}$$

where ε = Permittivity of semiconductor

A = Area of cross section

W = Width of depletion region

As the reverse biased applied to the diode increases, the width of the depletion region (W) increases. Thus the transition capacitance C_T decreases. In short, the capacitance can be controlled by the applied voltage.

Applications of Varactor Diode

1. Tuned circuits
2. FM modulators
3. Automatic frequency control devices
4. Adjustable bandpass filters
5. Parametric amplifiers
6. Television receivers

Example 1.2 : *Determine the transition capacitance of a diffused junction varactor diode at a reverse bias voltage of 4.2 V if C(0) = 80 pF and junction potential of 0.7 V. Also calculate constant K for diode.*

Solution : The transition capacitance is given by,

$$C_T = \frac{C(0)}{\left[1+\left|\frac{V_R}{V_J}\right|\right]^n}$$

Now $C(0) = 80$ pF, $n = \frac{1}{3}$ as diffused junction

$V_R = 4.2$ V , $V_J = 0.7$ V

$$\therefore \quad C_T = \frac{80\times10^{-12}}{\left[1+\left|\frac{4.2}{0.7}\right|\right]^{1/3}} = 41.82 \text{ pF}$$

The transition capacitance is also given by,

$$C_T = \frac{K}{[V_R + V_J]^n}$$

$$\therefore \quad 41.82\times10^{-12} = \frac{K}{[4.2+0.7]^{1/3}}$$

$$K = 71.03 \times 10^{-12}$$

Laser Diode

A Laser Diode is a semiconductor device similar to a light-emitting diode (LED). It uses p-n junction to emit coherent light in which all the waves are at the same frequency and phase. This coherent light is produced by the laser diode using a process termed as "Light Amplification by Stimulated Emission of Radiation", which is abbreviated as LASER. And since a p-n junction is used to produce laser light, this device is named as a laser diode. Before we learn more about the working process of a laser diode, let's look at how laser light is different from other types of light, and its advantages.

INJECTION LASER DIODE (ILD)

Injection Laser Diode is basically laser source that makes use of double hetero junction direct band gap semi conductors as the active medium in order to achieve laser light of high quantum efficiency and high power output.

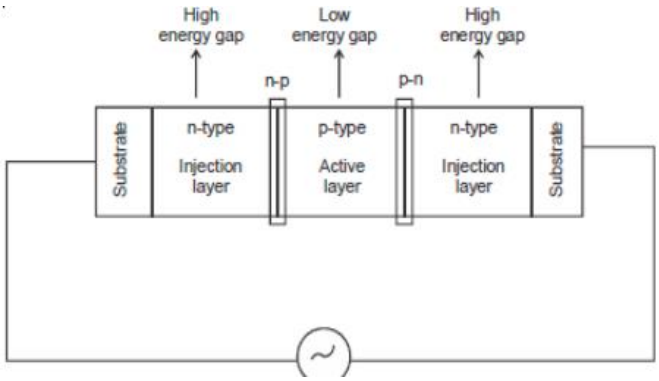
Hetero junction means a direct band gap p-n junction formed by two different semiconducting materials with different band gap energies. The material on one side of the junction differs from that on the other side of the junction.

Double hetero junction has two such hetero junctions.

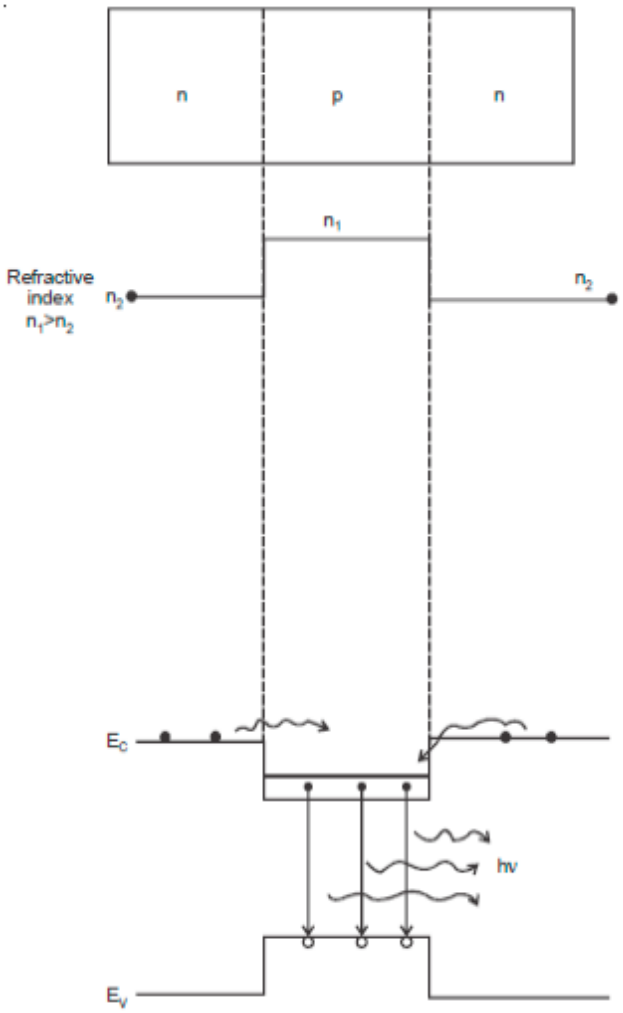
Structure of ILD

It uses double hetero junction semi conductors. There are three layers, one is the central active layer and the other two are the two adjacent layers. Active layer is of p-type material, usually $Ga_{(1-y)}Al_yAs$ of thickness 0.1 to 0.3 μm and of low energy band gap. The adjacent layers are made up of n-type $Ga_{(1-x)}$ Al_xAs of high energy band gap. Here x is not equal to y and they determine the band gap of alloys. The adjacent layers are also known as injection layers/confinement layers,

WORKING OF INJECTION Laser Diode



When drive current (I) is given to ILD, the excess electrons are moved from Ec of adjacent layer to Ec of active layer in order to achieve population inversion, a necessary condition to be satisfied for laser action to start. Electron transition occurs in the active layer from Ec to Ev, since only less energy has to be crossed in the active layer. Due this transition, electron-hole recombination takes place in the active layer; thereby photon is released from the active layer. This photon can then stimulate the release of coherent photons. Optical confinement that is necessary for amplification is obtained by choosing n1>n2, where n1 is the refractive index of the active layer and n2 is that of the adjacent layer. The photon released in the active layer moves and gets totally internally reflected on hitting the n-p and p-n junction, since n1 > n2. Number of times it gets amplified and finally it results in the emission of light in 800 - 900 nm wavelength range



Merits of ILD

i. High directivity, coherent radiation, monochromatic, high output power.
ii. Acts as narrow spectral width source.
iii. Coupling efficiency is high hence used to couple laser light into the optical fiber.
iv. Used for long distance optical communication at higher bit rate > 200 Mb / sec.
v. Reduces chromatic dispersion

Demerits of ILD

i. Shorter life time; 10 times expensive than LEDS.

ii. Wavelength of the output laser light is governed by the semiconductor bandgap.

iii. More temperature dependent.

iv. In order to maintain population inversion, high power consumption is needed and it consequently increases the temperature of the laser.

v. Due to increase in temperature, (i) Efficiency of the laser decreases rapidly as the electron populations are smeared out through the wide band structure of available

states. (ii) As the threshold (^{Jth}) current density depends on temperature, J^{th} also increases consequently.

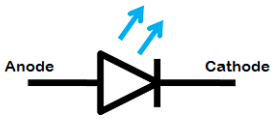
Light Emitting Diode (LED)

A light Emitting Diode (LED) is an optical semiconductor device that emits light when voltage is applied. In other words, LED is an optical semiconductor device that converts electrical energy into light energy.

When Light Emitting Diode (LED) is forward biased, free electrons in the conduction band recombines with the holes in the valence band and releases energy in the form of light.

The process of emitting light in response to the strong electric field or flow of electric current is called electroluminescence.

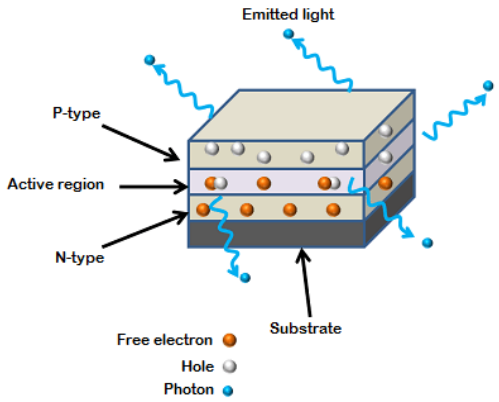
Symbol:



LED symbol

LED construction:

One of the methods used to construct LED is to deposit three semiconductor layers on the substrate. The three semiconductor layers deposited on the substrate are n-type semiconductor, p-type semiconductor and active region. Active region is present in between the n-type and p-type semiconductor layers.



When LED is forward biased, free electrons from n-type semiconductor and holes from p-type semiconductor are pushed towards the active region.

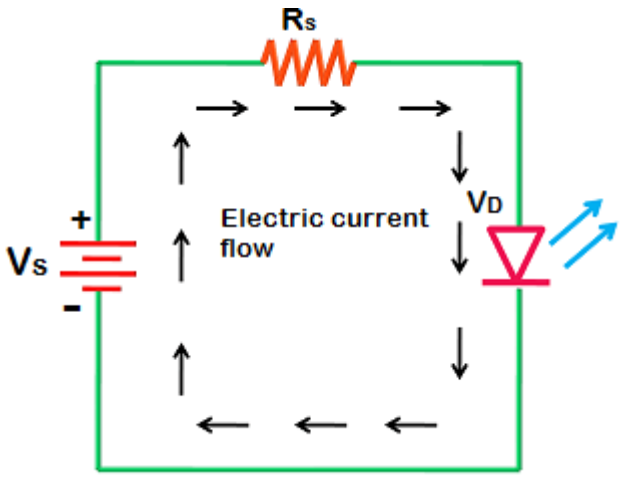
When free electrons from n-side and holes from p-side recombine with the opposite charge carriers (free electrons with holes or holes with free electrons) in active region, an invisible or visible light is emitted.

In LED, most of the charge carriers recombine at active region. Therefore, most of the light is emitted by the active region. The active region is also called as depletion region.

Biasing of LED

The safe forward voltage ratings of most LEDs is from 1V to 3 V and forward current ratings is from 200 mA to 100 mA.

To avoid breakdown a resistor (Rs) in series with the LED.



The current flowing through the LED is mathematically written as

$$I_F = \frac{V_s - V_D}{R_s}$$

Where,

IF = Forward current

VS = Source voltage or supply voltage

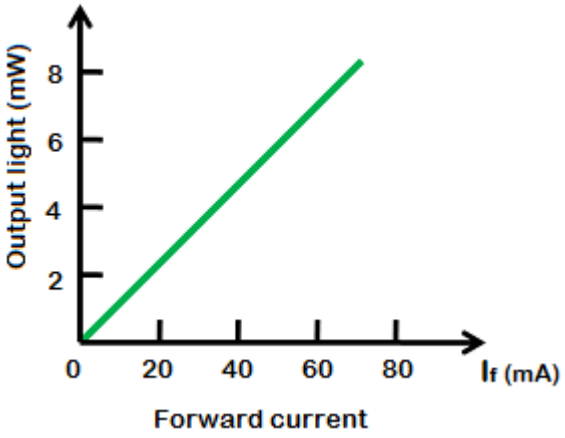
VD = Voltage drop across LED

R_S = Resistor or current limiting resistor

The voltage drop of LED is 2 to 3V whereas silicon or germanium diode is 0.3 or 0.7 V. Light emitting diodes consume more energy than silicon or germanium diodes to operate.

Output characteristics of LED

The amount of output light emitted by the LED is directly proportional to the amount of forward current flowing through the LED. More the forward current, the greater is the emitted output light.



The **material used for constructing LED** determines its color. In other words, the wavelength or color of the emitted light depends on the forbidden gap or energy gap of the material.

No.	Mixture used	Symbol	Colour
1.	Gallium arsenide	GaAs	Infrared, Invisible
2.	Gallium phosphide	GaP	Red or green
3.	Gallium arsenide phosphide	GaAsP	Red or yellow

Advantages of LED

1. The brightness of light emitted by LED is depends on the current flowing through the LED. Hence, the brightness of LED can be easily controlled by varying the current. This makes possible to operate LED displays under different ambient lighting conditions.

2. Light emitting diodes consume low energy.

3. LEDs are very cheap and readily available.

4. LEDs are light in weight.

5. Smaller size.

6. LEDs have longer lifetime.

7. LEDs operates very fast. They can be turned on and off in very less time.

8. LEDs do not contain toxic material like mercury which is used in fluorescent lamps.

9. LEDs can emit different colors of light.

Disadvantages of LED

1. LEDs need more power to operate than normal p-n junction diodes.

2. Luminous efficiency of LEDs is low.

Applications of LED

The various applications of LEDs are as follows

1. Burglar alarms systems
2. Calculators
3. Picture phones
4. Traffic signals
5. Digital computers
6. Multimeters
7. Microprocessors
8. Digital watches
9. Automotive heat lamps
10. Camera flashes

Example 1.1 : *What is the current through LED used in a circuit shown in the Fig. 1.11.*

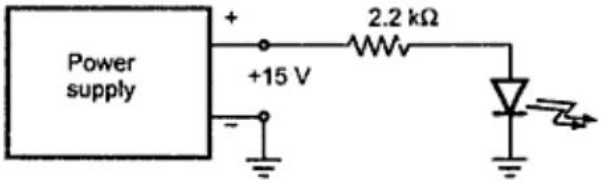


Fig. 1.11

Solution : Assume the drop across the LED as 2 V.

$\therefore \quad V_D = 2\ V$

From Fig. 1.11, $R_S = 2.2\ k\Omega$ and $V_S = 15\ V$

$$\therefore \quad I_S = \frac{V_S - V_D}{R_S} = \frac{15-2}{2.2\times10^3} = 5.91\ mA$$

Transistor

A **Transistor** is a three terminal semiconductor device that regulates current or voltage flow and acts as a switch or gate for signals.

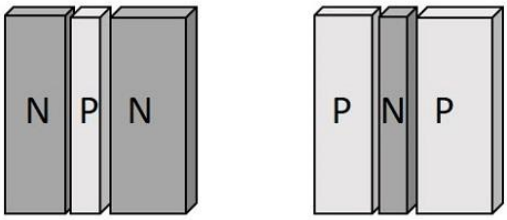
Uses of a transistor

- A transistor acts as **an Amplifier**, where the signal strength has to be increased.
- A transistor also acts as a **switch** to choose between available options.
- It also **regulates** the incoming **current and voltage** of the signals.

Constructional Details of a Transistor

The Transistor is a three terminal solid state device which is formed by connecting two diodes back to back. Hence it has got **two PN junctions**. Three terminals are drawn out of the three semiconductor materials present in it. This type of connection offers two types of transistors. They are **PNP** and **NPN** which means an N-type material between two Ptypes and the other is a P-type material between two N-types respectively.

The following illustration shows the basic construction of transistors



The three terminals drawn from the transistor indicate **Emitter,**
base and **Collector** terminals. They have their functionality as discussed below.

Emitter

- The left-hand side of the above shown structure can be understood as **Emitter**.
- This has a **moderate size** and is **heavily doped** as its main function is to **supply** a number of **majority carriers**, i.e. either electrons or holes.
- As this emits electrons, it is called as an Emitter.
- This is simply indicated with the letter **E**.

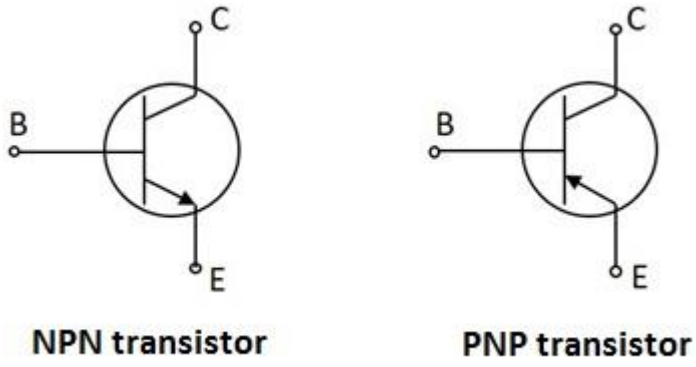
Base

- The middle material in the above figure is the **Base**.
- This is **thin** and **lightly doped**.
- Its main function is to **pass** the majority carriers from the emitter to the collector.
- This is indicated by the letter **B**.

Collector

- The right side material in the above figure can be understood as a **Collector**.
- Its name implies its function of **collecting the carriers**.
- This is a **bit larger** in size than emitter and base. It is **moderately doped**.
- This is indicated by the letter **C**.

The symbols of PNP and NPN transistors are as shown below.



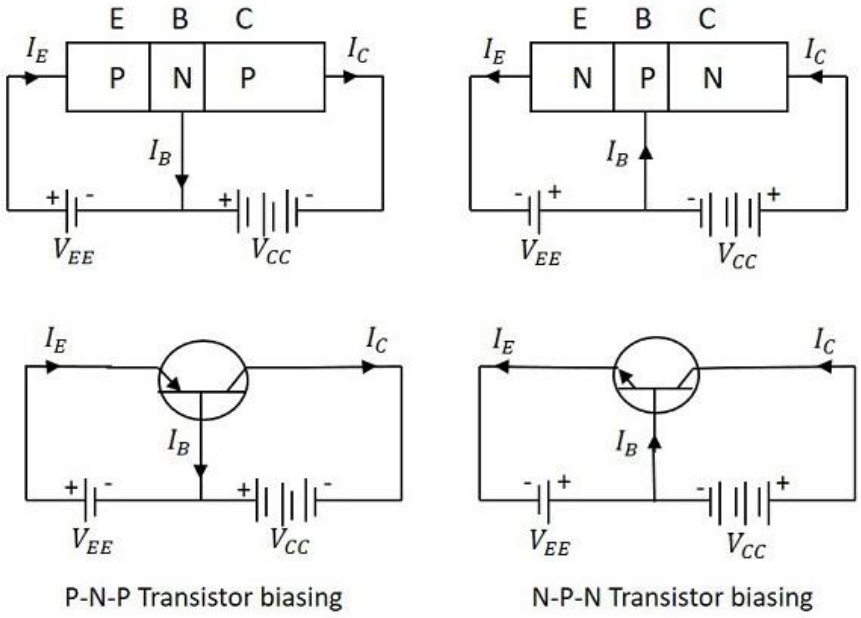
The **arrow-head** in the above figures indicated the **emitter** of a transistor. As the collector of a transistor has to dissipate much greater power, it is made large. Due to the specific functions of emitter and collector, they are **not interchangeable**. Hence the terminals are always to be kept in mind while using a transistor.

In a Practical transistor, there is a notch present near the emitter lead for identification. The PNP and NPN transistors can be differentiated using a Multimeter. The following image shows how different practical transistors look like.

Transistor Biasing

As we know that a transistor is a combination of two diodes, we have two junctions here. As one junction is between the emitter and base, that is called as **Emitter-Base junction** and likewise, the other is **Collector-Base junction**.

Biasing is controlling the operation of the circuit by providing power supply. The function of both the PN junctions is controlled by providing bias to the circuit through some dc supply. The figure below shows how a transistor is biased.



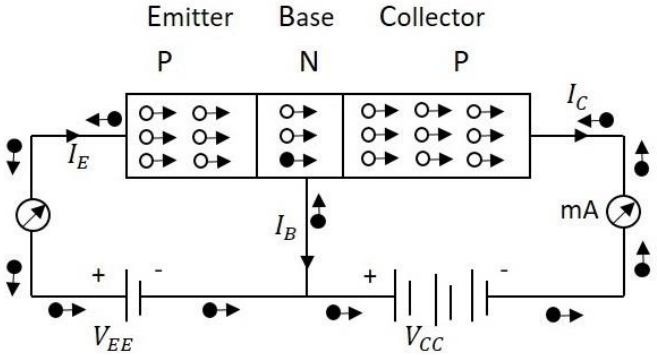
- The N-type material is provided negative supply and P-type material is given positive supply to make the circuit **Forward bias**.
- The N-type material is provided positive supply and P-type material is given negative supply to make the circuit **Reverse bias**.

By applying the power, the **emitter base junction** is always **forward biased** as the emitter resistance is very small. The **collector base junction** is **reverse biased** and its resistance is a bit higher. A small forward bias is sufficient at the emitter junction whereas a high reverse bias has to be applied at the collector junction.

The direction of current indicated in the circuits above, also called as the **Conventional Current**, is the movement of hole current which is **opposite to the electron current**.

Operation of PNP Transistor

The operation of a PNP transistor can be explained by having a look at the following figure, in which emitter-base junction is forward biased and collector-base junction is reverse biased.



The voltage **V_{EE}** provides a positive potential at the emitter which repels the holes in the P-type material and these holes cross the emitter-base junction, to reach the base region. There a very low percent of holes re-combine with free electrons of N-region. This provides very low current which constitutes the base current **I_B**. The remaining holes cross the collector-base junction, to constitute collector current **I_C**, which is the hole current.

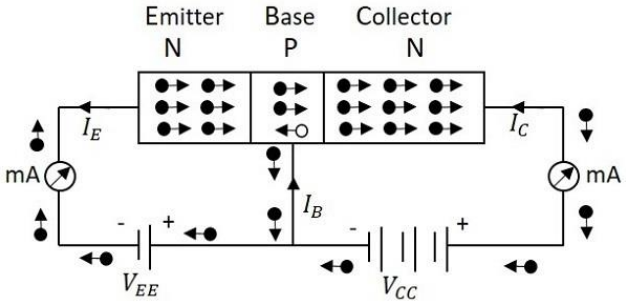
As a hole reaches the collector terminal, an electron from the battery negative terminal fills the space in the collector. This flow slowly increases and the electron minority current flows through the emitter, where each electron entering the positive terminal of **V_{EE}**, is replaced by a hole by moving towards the emitter junction. This constitutes emitter current **I_E**.

Hence we can understand that −

- The conduction in a PNP transistor takes place through holes.
- The collector current is slightly less than the emitter current.
- The increase or decrease in the emitter current affects the collector current.

Operation of NPN Transistor

The operation of an NPN transistor can be explained by having a look at the following figure, in which emitter-base junction is forward biased and collector-base junction is reverse biased.



The voltage **V_{EE}** provides a negative potential at the emitter which repels the electrons in the N-type material and these electrons cross the emitter-base junction, to reach the base region. There, a very low percent of electrons re-combine with free holes of P-region. This provides very low current which constitutes the base current **I_B**. The remaining holes cross the collector-base junction, to constitute the collector current **I_C**.

As an electron reaches out of the collector terminal, and enters the positive terminal of the battery, an electron from the negative terminal of the battery **V_{EE}** enters the emitter region. This flow slowly increases and the electron current flows through the transistor.

Hence,

- The conduction in a NPN transistor takes place through electrons.
- The collector current is higher than the emitter current.

- The increase or decrease in the emitter current affects the collector current.

Advantages of Transistors

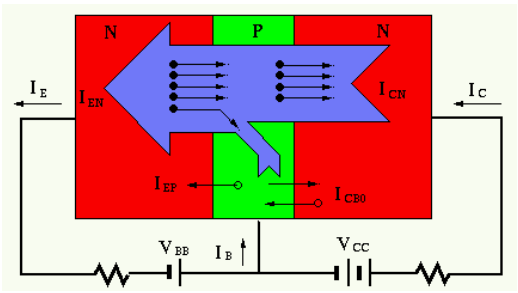
There are many advantages of using a transistor, such as −

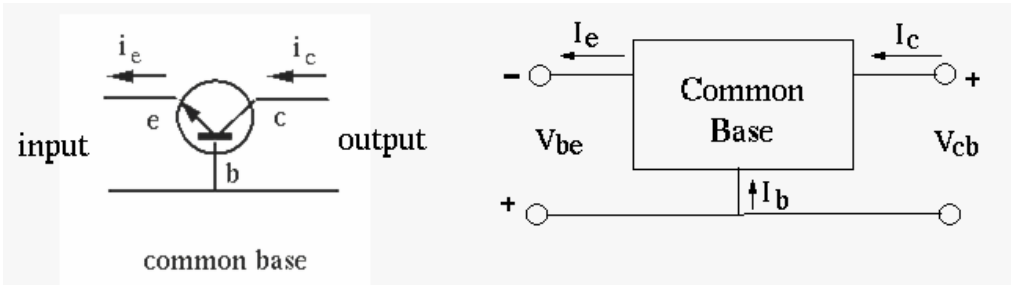
- High voltage gain.
- Lower supply voltage is sufficient.
- Most suitable for low power applications.
- Smaller and lighter in weight.
- Mechanically stronger than vacuum tubes.
- No external heating required like vacuum tubes.
- Very suitable to integrate with resistors and diodes to produce ICs.

There are few disadvantages such as they cannot be used for high power applications due to lower power dissipation. They have lower input impedance and they are temperature dependent

Common-Base (CB) configuration

The CB configuration can be considered as a 2-port circuit. The input port is formed by the emitter and base, the output port is formed by the collector and base. Two voltages V_{BE} and V_{CB} are applied respectively to the emitter E and collector C, with respect to the common base B, so that the BE junction is forward biased while the CB junction is reverse biased.





The polarity of V_{BE} and direction of I_B associated with the PN-junction between E and B are the same as those associated with a diode, voltage polarity: positive on P, negative on N, current direction: from P to N, but V_{CB} and the direction of I_C associated with the PN-junction between the base and collector are defined oppositely.

The behavior of the NPN-transistor is determined by its two PN-junctions:

- The forward biased base-emitter (BE) PN-junction allows the majority charge carriers, the electrons, in N-type emitter to go through the PN-junction to arrive at the P-type base, forming the emitter current I_E.
- As the base is thin and lightly doped, only a small number of the electrons from the emitter (e.g., 1%) are combined with the majority carriers, the holes, in the P-type base to form the base current I_B. The percentage depends on the doping and geometry of the material.
- Most of the electrons from the emitter (e.g., 99%), now the minority carriers in the P-type base, can go through the reverse biased collector-base PN junction to arrive at the N-type collector forming the collector current $I_C = I_E - I_B$.

The *current gain* or *current transfer ratio* of this CB circuit, denoted by α, is defined as the ratio between collector current I_C treated as the output and the emitter current I_E treated as the input:

$$\alpha = \frac{I_C}{I_E} < 1, \quad \text{e.g.} \quad \alpha = 99\% \approx 1 \tag{8}$$

i.e.,

$$\begin{aligned} I_C &= \alpha I_E \\ I_B &= I_E - I_C = I_E - \alpha I_E = (1-\alpha) I_E \\ I_E &= \frac{I_C}{\alpha} = \frac{I_B}{1-\alpha} \end{aligned} \tag{9}$$

The relationships between the current and voltage of both the input and output ports are described by the following input and output characteristics.

- **Input characteristics:**

  The input current I_E is a function of V_{CE} as well as the input voltage V_{BE}, which is much more dominant:

$$I_E = f(V_{BE}, V_{CB}) \approx f(V_{BE}) = \frac{I_B}{1-\alpha} = \frac{1}{1-\alpha} I_0 (e^{V_{BE}/V_T} - 1) \tag{10}$$

  Note that V_{CB} has little effect on I_E. Here I_B and V_{BE} associated with the emitter-base PN-junction satisfy the relationship for a diode:

$$I_B = I_0 (e^{V_{BE}/V_T} - 1) \tag{11}$$

  The voltage across the forward biased PN junction can be approximated by $V_{BE} = 0.7\,V$.

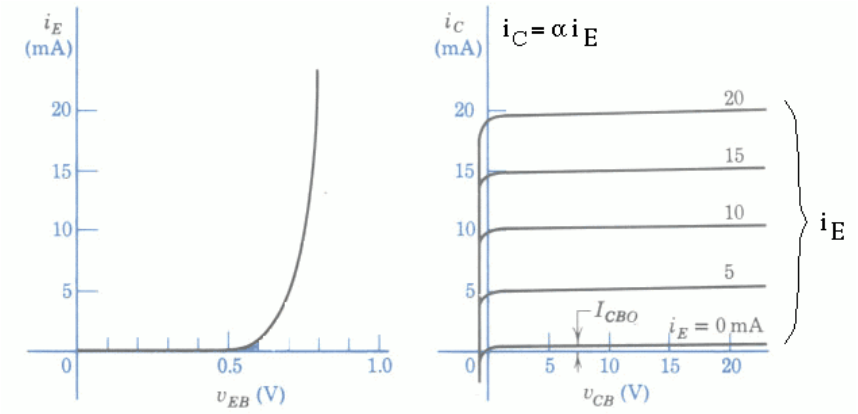
- **Output characteristics:**

The output current I_C is a function of the output voltage V_{CE} as well as the input current I_E, which is much more dominant:

$$I_C = f(I_E, V_{CB}) \approx f(I_E) = \alpha I_E \tag{12}$$

As $V_{CB} > 0$, i.e., the CB junction is reverse biased, the current I_C only depends on I_E. When $I_E = 0$, $I_C = I_{CB0}$ is the current caused by the minority carriers crossing the PN-junction. This is similar to the diode current-voltage characteristics seen before, except both axes are reversed (the polarity of V_{CB} and the direction I_C are oppositely defined). When I_E is increased, $I_C = \alpha I_E + I_{CB0} \approx \alpha I_E$ is increased correspondingly. However, as higher V_{CB} does not cause more electrons from the emitter, it has little effect on I_C.

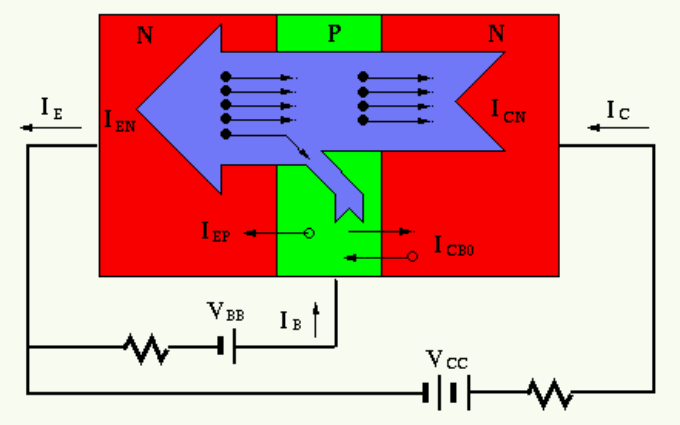
Note that when $V_{CB} = 0$, the PN-junction between base and collector is not biased (short circuited), there is still a non-zero collector current $I_C > 0$, formed by the electrons coming from the emitter, through both PN-junctions to form a closed loop current.

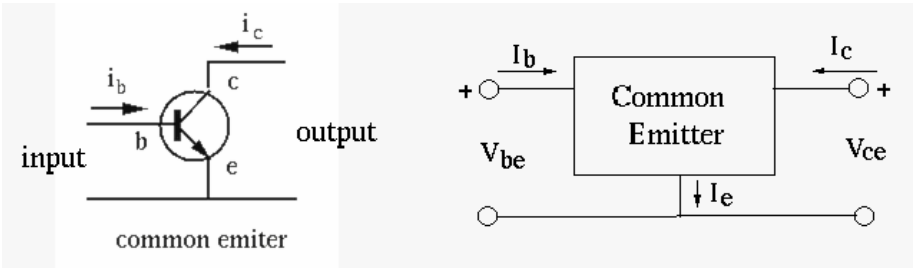


Common-Emitter (CE) configuration

Two voltages V_{BE} and V_{CE} are applied respectively to the base B and collector C with respect to the common emitter E. Typically $V_{CE} > V_{BE}$, i.e., the BE junction is forward biased while the CB junction is reverse biased, same as the CB configuration. The voltages of CB and CE configurations are related by:

$$V_{CE} = V_{CB} + V_{BE}, \quad \text{or} \quad V_{CB} = V_{CE} - V_{BE} \tag{13}$$





The CE configuration can be considered as a 2-port circuit. The input port is formed by the emitter and base, the output port is formed by the collector and emitter. The current gain of the CE circuit, denoted by β, is defined as the ratio between the collector current I_C treated as the output and the base current I_B treated as the input:

$$\beta = \frac{I_C}{I_B} = \frac{\alpha I_E}{(1-\alpha)I_E} = \frac{\alpha}{1-\alpha}, \tag{14}$$

For example, if $\alpha = 0.99$, then $\beta = 0.99/(1-0.99) = 99$.

The two parameters α and β are related by any of the following:

$$\beta = \frac{\alpha}{1-\alpha}, \quad \alpha = \frac{\beta}{1+\beta}, \quad 1+\beta = \frac{1}{1-\alpha}, \quad 1-\alpha = \frac{1}{1+\beta} \tag{15}$$

The relationships between the current and voltage of both the input and output ports are described by the following input and output characteristics.

- **Input characteristics:**

  Same as in the case of common-base configuration, the EB junction of the common-emitter configuration can also be considered as a forward biased diode, the current-voltage characteristics is similar to that of a diode:

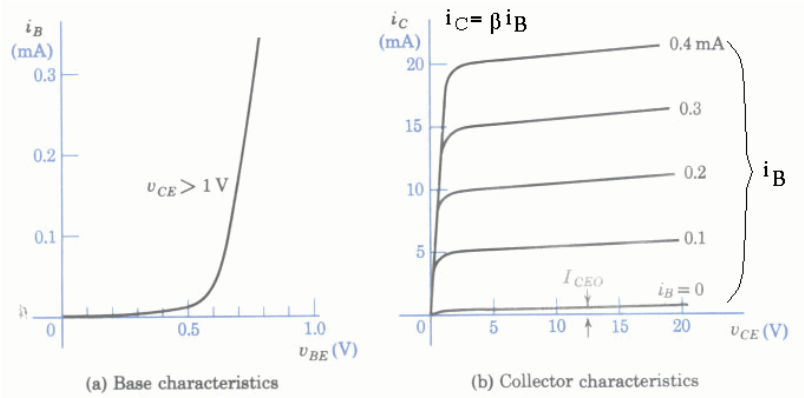
  $$I_B = f(V_{BE}, V_{CE}) \approx f(V_{BE}) = I_0(e^{V_{BE}/V_T} - 1) \tag{16}$$

  The voltage across the forward biased PN junction is approximately $V_{BE} = 0.7\,V$. V_{CE} has little effect on I_B.

- **Output characteristics:**

  $$I_C = f(I_B, V_{CE}) \approx f(I_B) = \beta I_B \qquad \text{(in linear region)} \tag{17}$$

  The current $I_C = \beta I_B$ depends on the current I_B, which in turn depends on V_{BE}. However, as higher V_{CE} does not cause more electrons from the emitter, it has little effect on I_C.

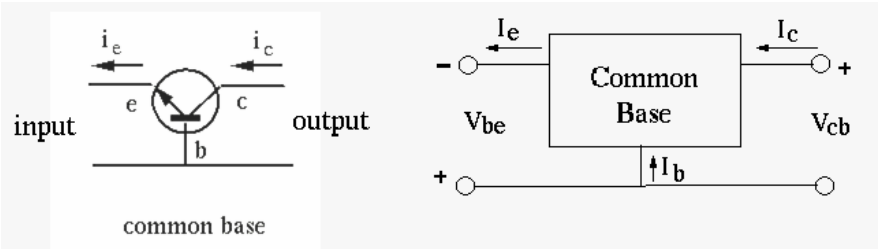


(a) Base characteristics (b) Collector characteristics

The relationship between the input and output currents of both CB and CE configurations is summarized below:

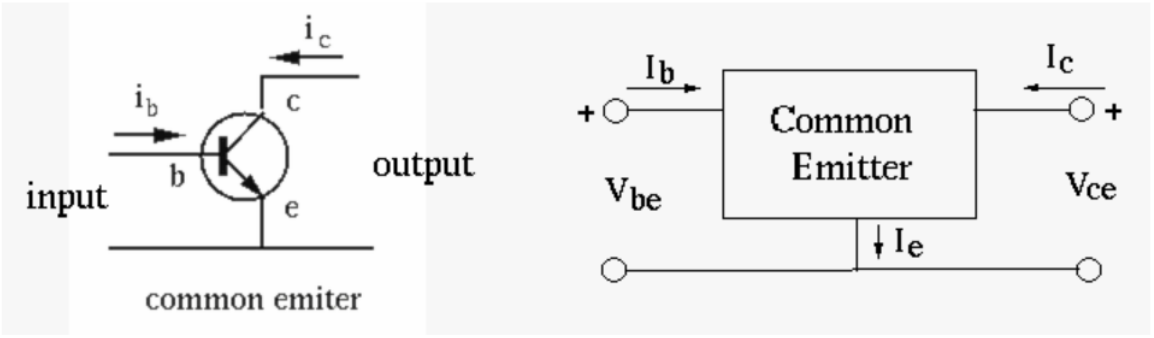
$$I_E = I_C + I_B, \qquad V_{CE} = V_{CB} + V_{BE} \tag{18}$$

Common Base:



$$\alpha = \frac{I_{out}}{I_{in}} = \frac{I_C}{I_E}, \quad \text{i.e.,} \quad I_C = \alpha I_E$$
$$I_E = I_C + I_B = \alpha I_E + (1-\alpha) I_E$$

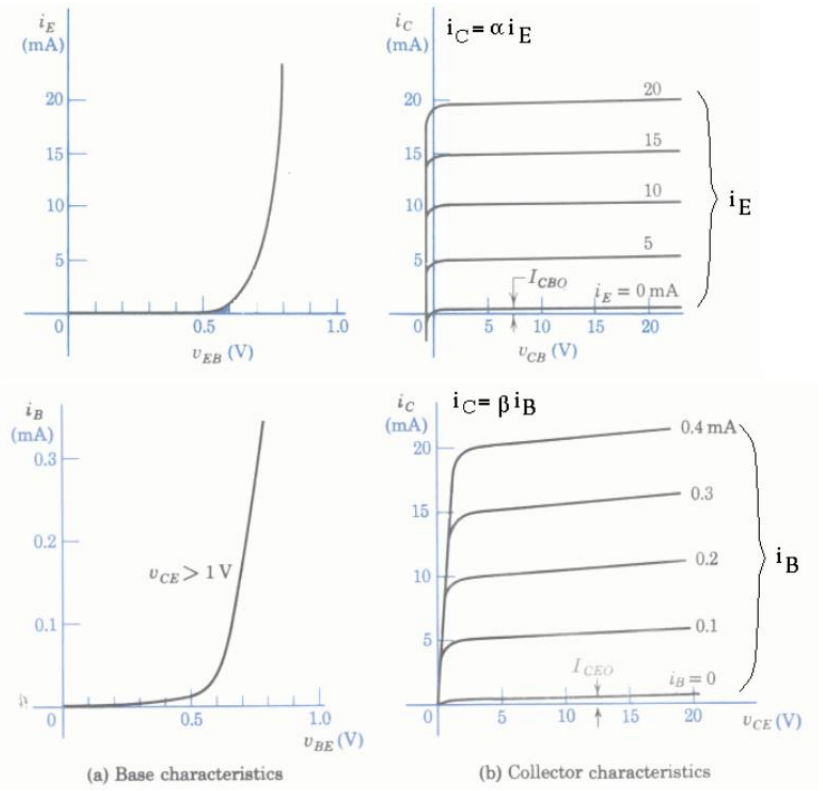
- Common Emitter:

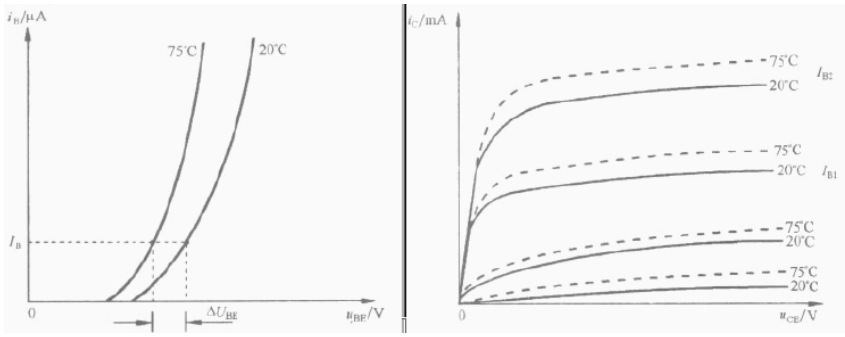


$$\beta = \frac{I_{out}}{I_{in}} = \frac{I_C}{I_B}, \quad \text{i.e.,} \quad I_C = \beta I_B$$
$$I_E = I_C + I_B = \beta I_B + I_B$$

The collector characteristics of the common-base (CB) and common-emitter (CE) configurations have the following differences:

- In CB circuit $I_C = \alpha I_E$ is slightly less than I_E, while in CE circuit $I_C = \beta I_B$ is much greater than I_B.
- In CB circuit, $I_C > 0$ when $V_{CB} = 0$; while in CE circuit $I_C = 0$ when $V_{CE} = 0$ (as $V_{CB} = -V_{BE}$ has the effect of suppressing I_C).
- Increased V_{CE} will slightly increase α but more greatly increase $\beta = \alpha/(1-\alpha)$, thereby causing more significantly increased I_C.
- I_E in CB is a function of two variables V_{BE} and V_{CB}, but the former is much more significant then the latter. I_B in CE is a function of two variables V_{BE} and V_{CE}, but the former is much more significant then the latter.
- I_C in CB is a function of two variables V_{CB} and I_E. When V_{CB} is small, its slight increase will cause significant increase of I_C. But its further increase will not cause much change in I_C due to saturation (all available charge carriers travel at the saturation velocity to arrive at collector C), $I_C = \alpha I_E$ is mostly determined by I_E.
- I_C in CE is a function of two variables V_{CE} and I_B. When V_{CE} is small ($\approx 0.3V$), its slight increase will cause significant increase of I_C. But when $V_{CE} > 0.3V$, its further increase will not cause much change in I_C due to saturation (all available charge carriers travel at the saturation velocity to arrive at collector C), $I_C = \beta I_B$ is mostly determined by I_B.





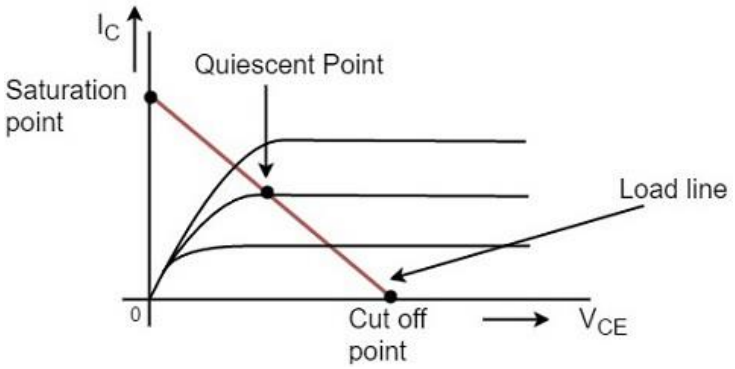
Various parameters of a transistor change as functions of temperature. For example, increases along with temperature.

Operating point.

When a line is drawn joining the saturation and cut off points, such a line can be called as **Load line**. This line, when drawn over the output characteristic curve, makes contact at a point called as **Operating point**.

This operating point is also called as **quiescent point** or simply **Q-point**. There can be many such intersecting points, but the Q-point is selected in such a way that irrespective of AC signal swing, the transistor remains in the active region.

The following graph shows how to represent the operating point.



The operating point should not get disturbed as it should remain stable to achieve faithful amplification. Hence the quiescent point or Q-point is the value where the **Faithful Amplification** is achieved.

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SCHOOL OF SCIENCE AND HUMANITIES

DEPARTMENT OF PHYSICS

UNIT – II - Digital and Analog Electronics – SPH1216

UNIT 2 - Field-Effect Transistors (FET) and Transistors Amplifier

JFET- current-voltage characteristics, Small Signal BJT amplifiers: AC equivalent circuit, hybrid, re model and their use in amplifier design, Multistage amplifiers, frequency response of basic & compound configuration, Power amplifiers: Class A, B, AB, C and D stages, IC output stages.

Amplifier

An Amplifier circuit is one which strengthens the signal. The amplifier action and the important considerations for the practical circuit of transistor amplifier were also detailed in previous chapters.

Let us now try to understand the classification of amplifiers. Amplifiers are classified according to many considerations.

Based on number of stages

Depending upon the number of stages of Amplification, there are Single-stage amplifiers and Multi-stage amplifiers.

- **Single-stage Amplifiers** − This has only one transistor circuit, which is a singlestage amplification.
- **Multi-stage Amplifiers** − This has multiple transistor circuit, which provides multi-stage amplification.

Based on its output

Depending upon the parameter that is amplified at the output, there are voltage and power amplifiers.

- **Voltage Amplifiers** − The amplifier circuit that increases the voltage level of the input signal, is called as Voltage amplifier.
- **Power Amplifiers** − The amplifier circuit that increases the power level of the input signal, is called as Power amplifier.

Based on the input signals

Depending upon the magnitude of the input signal applied, they can be categorized as Small signal and large signal amplifiers.

- **Small signal Amplifiers** − When the input signal is so weak so as to produce small fluctuations in the collector current compared to its quiescent value, the amplifier is known as Small signal amplifier.
- **Large signal amplifiers** − When the fluctuations in collector current are large i.e. beyond the linear portion of the characteristics, the amplifier is known as large signal amplifier.

Based on the frequency range

Depending upon the frequency range of the signals being used, there are audio and radio amplifiers.

- **Audio Amplifiers** − The amplifier circuit that amplifies the signals that lie in the audio frequency range i.e. from 20Hz to 20 KHz frequency range, is called as audio amplifier.
- **Power Amplifiers** − The amplifier circuit that amplifies the signals that lie in a very high frequency range, is called as Power amplifier.

Based on Biasing Conditions

Depending upon their mode of operation, there are class A, class B and class C amplifiers.

- **Class A amplifier** − The biasing conditions in class A power amplifier are such that the collector current flows for the entire AC signal applied.
- **Class B amplifier** − The biasing conditions in class B power amplifier are such that the collector current flows for half-cycle of input AC signal applied.
- **Class C amplifier** − The biasing conditions in class C power amplifier are such that the collector current flows for less than half cycle of input AC signal applied.
- **Class AB amplifier** − The class AB power amplifier is one which is created by combining both class A and class B in order to have all the advantages of both the classes and to minimize the problems they have.

Based on the Coupling method

Depending upon the method of coupling one stage to the other, there are RC coupled, Transformer coupled and direct coupled amplifier.

- **RC Coupled amplifier** − A Multi-stage amplifier circuit that is coupled to the next stage using resistor and capacitor (RC) combination can be called as a RC coupled amplifier.

- **Transformer Coupled amplifier** − A Multi-stage amplifier circuit that is coupled to the next stage, with the help of a transformer, can be called as a Transformer coupled amplifier.
- **Direct Coupled amplifier** − A Multi-stage amplifier circuit that is coupled to the next stage directly, can be called as a direct coupled amplifier.

Based on the Transistor Configuration

Depending upon the type of transistor configuration, there are CE CB and CC amplifiers.

- **CE amplifier** − The amplifier circuit that is formed using a CE configured transistor combination is called as CE amplifier.
- **CB amplifier** − The amplifier circuit that is formed using a CB configured transistor combination is called as CB amplifier.
- **CC amplifier** − The amplifier circuit that is formed using a CC configured transistor combination is called as CC amplifier.

Field Effect Transistor

The **Field Effect Transistor**, or simply **FET** however, uses the voltage that is applied to their input terminal, called the Gate to control the current flowing through them resulting in the output current being proportional to the input voltage. As their operation relies on an electric field (hence the name field effect) generated by the input Gate voltage, this then makes the **Field Effect Transistor** a "VOLTAGE" operated device.

The **Field Effect Transistor** is a three terminal unipolar semiconductor device that has very similar characteristics to those of their *Bipolar Transistor* counterparts. For example, high efficiency, instant operation, robust and cheap and can be used in most electronic circuit applications to replace their equivalent bipolar junction transistors (BJT) cousins.

Field effect transistors can be made much smaller than an equivalent BJT transistor and along with their low power consumption and power dissipation makes them ideal for use in integrated circuits such as the CMOS range of digital logic chips.

We remember from the previous tutorials that there are two basic types of bipolar transistor construction, NPN and PNP, which basically describes the physical arrangement of the P-type and N-type semiconductor materials from which they are made. This is also true of FET's as there are also two basic classifications of Field Effect Transistor, called the N-channel FET and the P-channel FET.

The field effect transistor is a three terminal device that is constructed with no PN-junctions within the main current carrying path between the Drain and

the Source terminals. These terminals correspond in function to the Collector and the Emitter respectively of the bipolar transistor. The current path between these two terminals is called the "channel" which may be made of either a P-type or an N-type semiconductor material.

The control of current flowing in this channel is achieved by varying the voltage applied to the Gate. As their name implies, Bipolar Transistors are "Bipolar" devices because they operate with both types of charge carriers, Holes and Electrons. The Field Effect Transistor on the other hand is a "Unipolar" device that depends only on the conduction of electrons (N-channel) or holes (P-channel).

The **Field Effect Transistor** has one major advantage over its standard bipolar transistor cousins, in that their input impedance, (Rin) is very high, (thousands of Ohms), while the BJT is comparatively low. This very high input impedance makes them very sensitive to input voltage signals, but the price of this high sensitivity also means that they can be easily damaged by static electricity.

There are two main types of field effect transistor, the **Junction Field Effect Transistor** or **JFET** and the **Insulated-gate Field Effect Transistor** or **IGFET)**, which is more commonly known as the standard **Metal Oxide Semiconductor Field Effect Transistor** or **MOSFET** for short.

The Junction Field Effect Transistor

We saw previously that a bipolar junction transistor is constructed using two PN-junctions in the main current carrying path between the Emitter and the Collector terminals. The **Junction Field Effect Transistor** (JUGFET or JFET) has no PN-junctions but instead has a narrow piece of high resistivity semiconductor material forming a "Channel" of either N-type or P-type silicon for the majority carriers to flow through with two ohmic electrical connections at either end commonly called the Drain and the Source respectively.

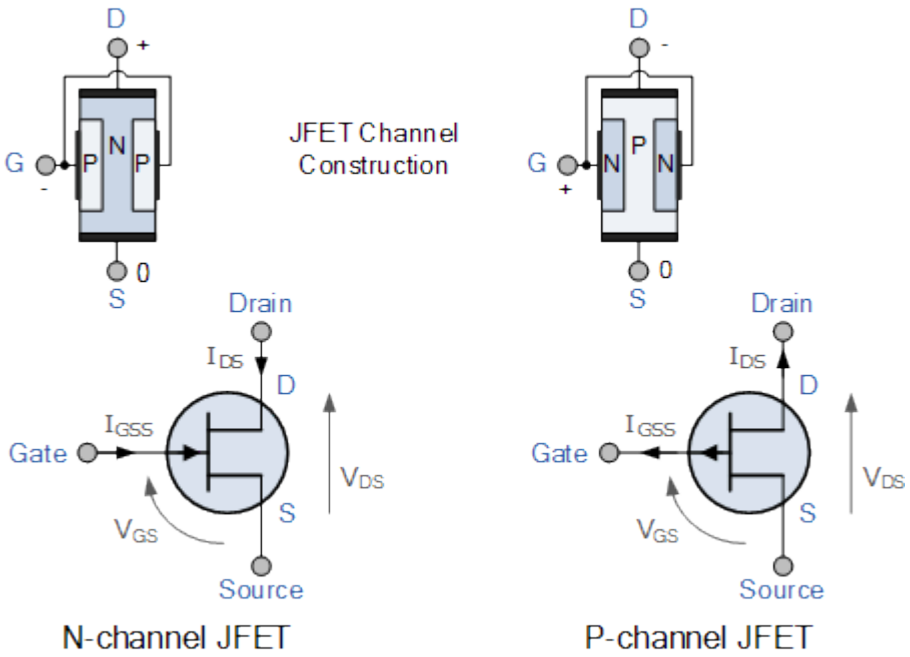
There are two basic configurations of junction field effect transistor, the N-channel JFET and the P-channel JFET. The N-channel JFET's channel is doped with donor impurities meaning that the flow of current through the channel is negative (hence the term N-channel) in the form of electrons.

Likewise, the P-channel JFET's channel is doped with acceptor impurities meaning that the flow of current through the channel is positive (hence the term P-channel) in the form of holes. N-channel JFET's have a greater channel conductivity (lower resistance) than their equivalent P-channel types, since electrons have a higher mobility through a conductor compared to holes. This makes the N-channel JFET's a more efficient conductor compared to their P-channel counterparts.

We have said previously that there are two ohmic electrical connections at either end of the channel called the Drain and the Source. But within this channel there is a third electrical connection which is called the Gate terminal and this can also be a P-type or N-type material forming a PN-junction with the main channel.

The relationship between the connections of a junction field effect transistor and a bipolar junction transistor are compared below.

The symbols and basic construction for both configurations of JFETs are shown below.



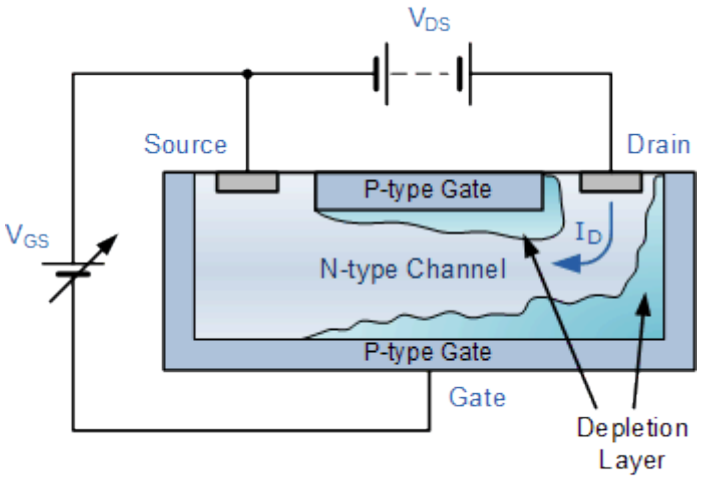
The semiconductor "channel" of the **Junction Field Effect Transistor** is a resistive path through which a voltage V_{DS} causes a current I_D to flow and as such the junction field effect transistor can conduct current equally well in either direction. As the channel is resistive in nature, a voltage gradient is thus formed down the length of the channel with this voltage becoming less positive as we go from the Drain terminal to the Source terminal.

The result is that the PN-junction therefore has a high reverse bias at the Drain terminal and a lower reverse bias at the Source terminal. This bias causes a "depletion layer" to be formed within the channel and whose width increases with the bias.

The magnitude of the current flowing through the channel between the Drain and the Source terminals is controlled by a voltage applied to the Gate terminal, which is a reverse-biased. In an N-channel JFET this Gate voltage is negative while for a P-channel JFET the Gate voltage is positive.

The main difference between the JFET and a BJT device is that when the JFET junction is reverse-biased the Gate current is practically zero, whereas the Base current of the BJT is always some value greater than zero.

Biasing of an N-channel JFET



The cross sectional diagram above shows an N-type semiconductor channel with a P-type region called the Gate diffused into the N-type channel forming a reverse biased PN-junction and it is this junction which forms the *depletion region* around the Gate area when no external voltages are applied. JFETs are therefore known as depletion mode devices.

This depletion region produces a potential gradient which is of varying thickness around the PN-junction and restrict the current flow through the channel by reducing its effective width and thus increasing the overall resistance of the channel itself.

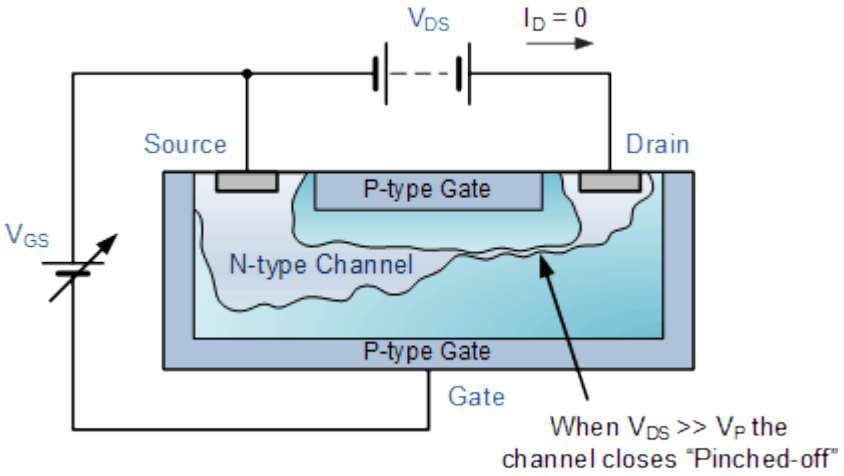
Then we can see that the most-depleted portion of the depletion region is in between the Gate and the Drain, while the least-depleted area is between the Gate and the Source. Then the JFET's channel conducts with zero bias voltage applied (ie, the depletion region has near zero width).

With no external Gate voltage ($V_G = 0$), and a small voltage (V_{DS}) applied between the Drain and the Source, maximum saturation current (I_{DSS}) will flow through the channel from the Drain to the Source restricted only by the small depletion region around the junctions.

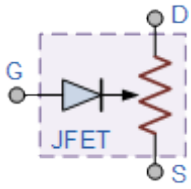
If a small negative voltage ($-V_{GS}$) is now applied to the Gate the size of the depletion region begins to increase reducing the overall effective area of the channel and thus reducing the current flowing through it, a sort of "squeezing" effect takes place. So by applying a reverse bias voltage increases the width of the depletion region which in turn reduces the conduction of the channel.

Since the PN-junction is reverse biased, little current will flow into the gate connection. As the Gate voltage ($-V_{GS}$) is made more negative, the width of the channel decreases until no more current flows between the Drain and the Source and the FET is said to be "pinched-off" (similar to the cut-off region for a BJT). The voltage at which the channel closes is called the "pinch-off voltage", (V_P).

JFET Channel Pinched-off



In this pinch-off region the Gate voltage, V_{GS} controls the channel current and V_{DS} has little or no effect.



JFET Model

The result is that the FET acts more like a voltage controlled resistor which has zero resistance when V_{GS} = 0 and maximum "ON" resistance (R_{DS}) when the Gate voltage is very negative. Under normal operating conditions, the JFET gate is always negatively biased relative to the source.

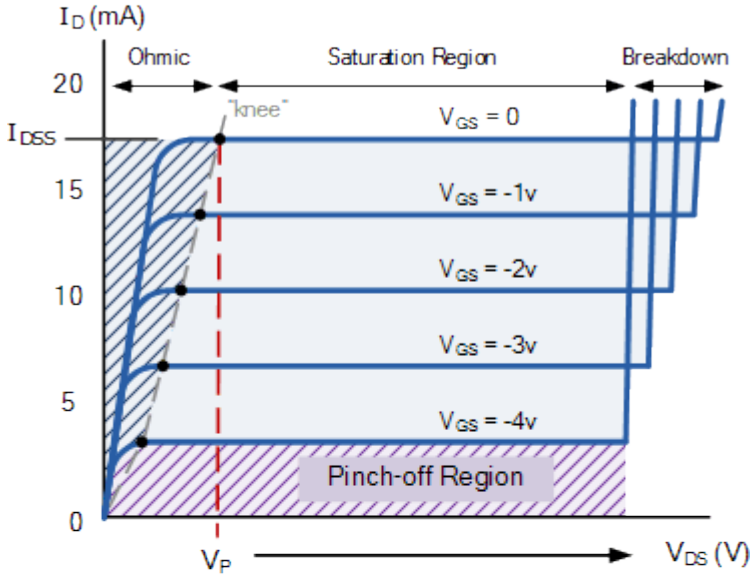
It is essential that the Gate voltage is never positive since if it is all the channel current will flow to the Gate and not to the Source, the result is damage to the JFET. Then to close the channel:

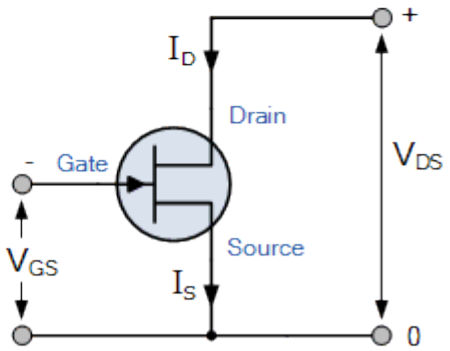
- No Gate Voltage (V_{GS}) and V_{DS} is increased from zero.
- No V_{DS} and Gate control is decreased negatively from zero.
- V_{DS} and V_{GS} varying.

The P-channel **Junction Field Effect Transistor** operates exactly the same as the N-channel above, with the following exceptions: 1). Channel current is positive due to holes, 2). The polarity of the biasing voltage needs to be reversed.

The output characteristics of an N-channel JFET with the gate short-circuited to the source is given as:

Output characteristic V-I curves of a typical junction FET





The voltage V_{GS} applied to the Gate controls the current flowing between the Drain and the Source terminals. V_{GS} refers to the voltage applied between the Gate and the Source while V_{DS} refers to the voltage applied between the Drain and the Source.

Because a **Junction Field Effect Transistor** is a voltage controlled device, "NO current flows into the gate!" then the Source current (I_S) flowing out of the device equals the Drain current flowing into it and therefore ($I_D = I_S$).

The characteristics curves example shown above, shows the four different regions of operation for a JFET and these are given as:

- Ohmic Region – When $V_{GS} = 0$ the depletion layer of the channel is very small and the JFET acts like a voltage controlled resistor.
- Cut-off Region – This is also known as the pinch-off region were the Gate voltage, V_{GS} is sufficient to cause the JFET to act as an open circuit as the channel resistance is at maximum.
- Saturation or Active Region – The JFET becomes a good conductor and is controlled by the Gate-Source voltage, (V_{GS}) while the Drain-Source voltage, (V_{DS}) has little or no effect.

- Breakdown Region – The voltage between the Drain and the Source, (V_{DS}) is high enough to causes the JFET's resistive channel to break down and pass uncontrolled maximum current.

The characteristics curves for a P-channel junction field effect transistor are the same as those above, except that the Drain current I_D decreases with an increasing positive Gate-Source voltage, V_{GS}.

The Drain current is zero when $V_{GS} = V_P$. For normal operation, V_{GS} is biased to be somewhere between V_P and 0. Then we can calculate the Drain current, I_D for any given bias point in the saturation or active region as follows:

Drain current in the active region.

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

Note that the value of the Drain current will be between zero (pinch-off) and I_{DSS} (maximum current). By knowing the Drain current I_D and the Drain-Source voltage V_{DS} the resistance of the channel (R_{DS}) is given as:

Drain-Source Channel Resistance.

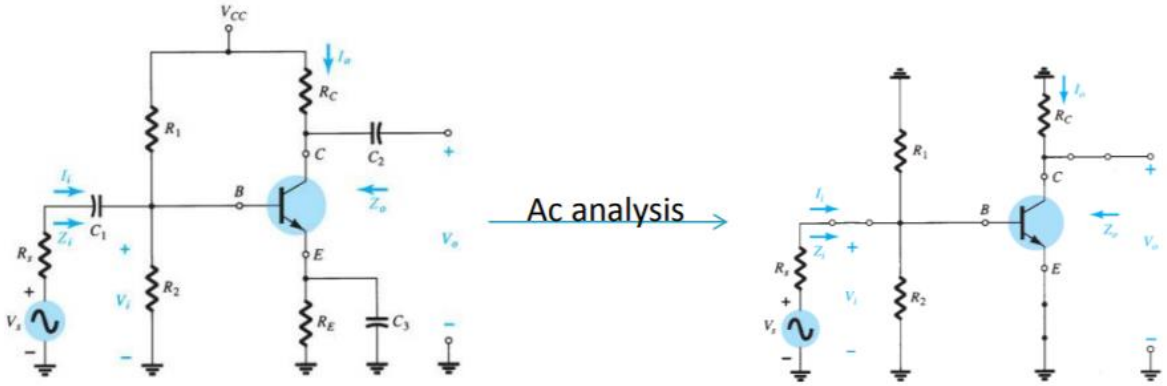
$$R_{DS} = \frac{\Delta V_{DS}}{\Delta I_D} = \frac{1}{g_m}$$

Where: g_m is the "transconductance gain" since the JFET is a voltage controlled device and which represents the rate of change of the Drain current with respect to the change in Gate-Source voltage.

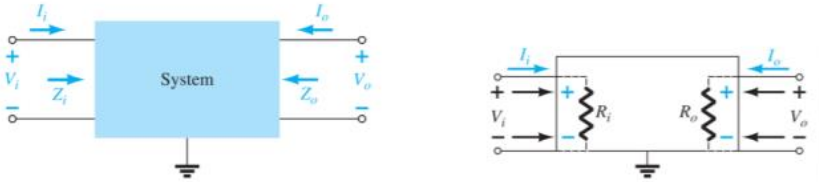
Small-signal model

Small-signal modeling is a common analysis technique in electronics engineering used to approximate the behavior of electronic circuits containing nonlinear devices with linear equations. It is applicable to electronic circuits in which the AC signals (i.e., the time-varying currents and voltages in the circuit) are small relative to the DC bias currents and voltages. A small-signal model is an AC equivalent circuit in which the nonlinear circuit elements are replaced by linear elements whose values are given by the first-order (linear) approximation of their characteristic curve near the bias point.

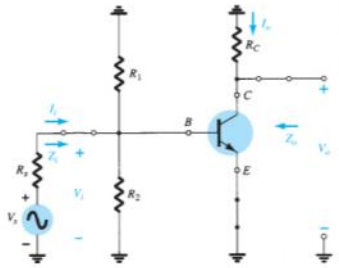
- A model is a combination of circuit elements, properly chosen, that best approximates the actual behavior of a semiconductor device under specific operating conditions.

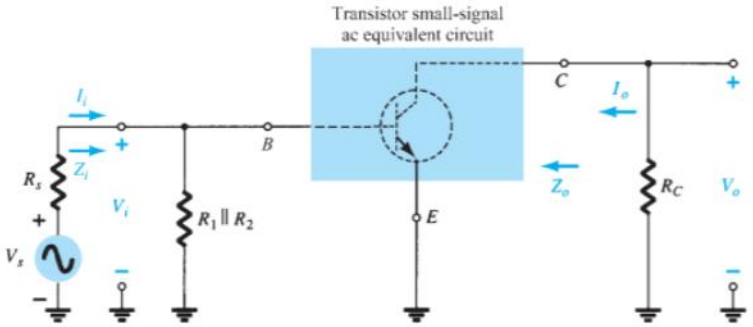


- Defining the important parameters of any system.



- the ac equivalent of a transistor network is obtained by:
  1. Setting all dc sources to zero and replacing them by a short-circuit equivalent
  2. Replacing all capacitors by a short-circuit equivalent
  3. Removing all elements bypassed by the short-circuit equivalents introduced by steps 1 and 2
  4. Redrawing the network in a more convenient and logical form





Hybrid Parameters

Usually an amplifier is analyzed with the help of β and other parameters. Though this method is simple, but very accurate results are not obtained. The reason is that for the analysis, the input and the output circuits of an amplifier are considered to be completely independent, but in practice it is not so.

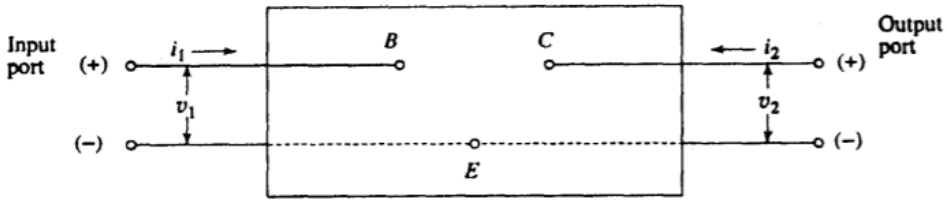
Therefore, for analyzing the behaviour of amplifiers, "hybrid method" is used which gives the most accurate results.

ADVANTAGES OF HYBRID PARAMETERS

- They give accurate results as the interactions of input and output circuits of the amplifier have been taken into account.
- These parameters can be measured easily.

TWO-PORT NETWORK

A transistor is a three terminal(Emitter E, Base B, Collector C) device. In all the three configurations one of the three terminals is common to input and output circuits, so there are **two-ports**(pair of terminals) in a transistor circuit. Therefore, it can be considered as a two port network for discussion (See figure).



Transistor as port

The voltages and currents of the above port can be related by the following equations

$$v_1 = h_{11}i_1 + h_{12}v_2 \quad \text{(i)}$$

$$i_2 = h_{21}i_1 + h_{22}v_2 \quad \text{(ii)}$$

Here h_{11},h_{21},h_{12} and h_{22} are constants and are known as "**hybrid parameters**".

UNITS FOR H-PARAMETERS

h_{11}	ohm
h_{12}	no units
h_{21}	no units
h_{22}	mho i.e. 1/ohm

DETERMINATION OF H-PARAMETERS

For the determination of h-parameters, proceed as follows:

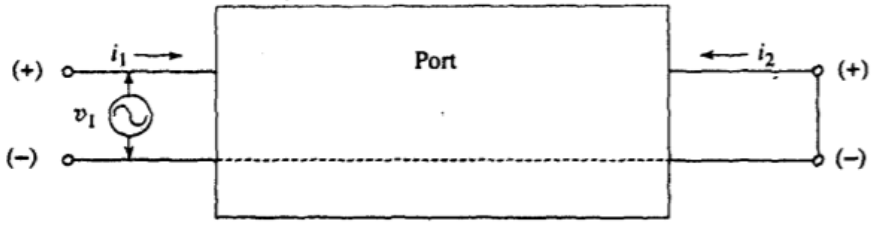
Short circuit the output terminals (See figure)

(a) Now the output voltage $v_2 = 0$, putting the value in Equation (I) above

$$v_1 = h_{11}i_1 + h_{12}0$$

$$h_{11} = v_1/i_1$$

h_{11} is called **input impedance**.



(b) Putting $v_2 = 0$ in equation(ii)

$$i_2 = h_{21}.i_1 + h_{22}.0$$

$$h_{21} = i_2/i_1$$

h_{21} is called "current gain" or "**forward current ratio**".

Open circuit the input terminals (See Figure)

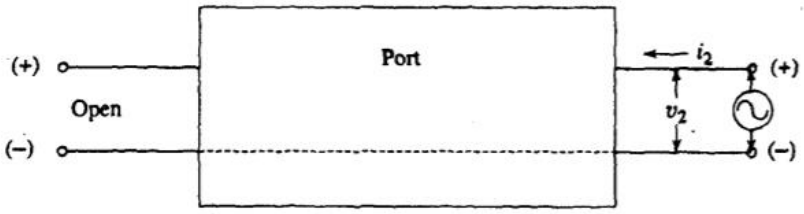
(a) This will reduce input current to $i_1 = 0$

Putting $i_1 = 0$ in Equation (I)

$$v_1 = h_{11}.0 + h_{12}.v_2$$

$$h_{12} = v_1/v_2$$

h_{12} is called "**reverse voltage ratio**" or "feedback voltage ratio".



(b) Putting $i_1 = 0$ in Eq. (ii)

$$i_2 = h_{21}.0 + h_{22}.v_2$$

$$h_{22} = i_1/v_2$$

The h_{22} is called "**output admittance**"(reverse of resistance).

Now the various h-parameters can be defined as :

$h_{11} = v_1/i_1$ ($v_2 = 0$) = input impedance (with output shorted = h_i (in ohms)

$h_{21} = i_2/i_1$ ($v_2 = 0$) = forward current ratio (with output shorted) = h_f (no units)

$h_{12} = v_1/v_2$ ($i_1 = 0$) = reverse voltage ratio (with input open) = h_r (no units)

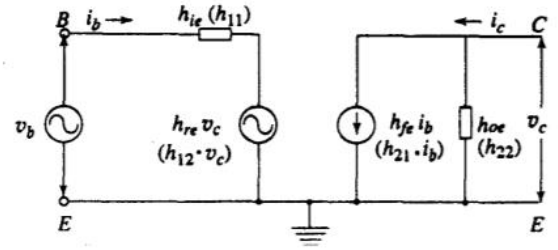
$h_{22} = i_1/v_2$ ($i_1 = 0$) = output admittance (with input open) = h_0 (in mho)

NOMENCLATURE OF H-PARAMETERS FOR COMMON EMITTER CONFIGURATION

h_{11}	h_{ib}
h_{12}	h_{rb}
h_{21}	h_{fb}
h_{22}	h_{ob}

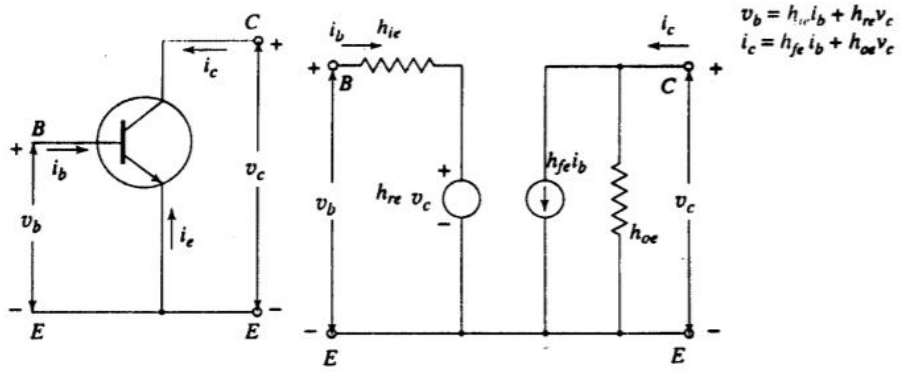
LOW FREQUENCY TRANSISTOR HYBRID MODEL

Following figure shows hybrid model of a transistor in CE configurations.



Hybrid model of transistor in CE configurations

Following figure shows circuit arrangement, hybrid model and V-I equations for CE configurations for an N-P-N transistor.



Circuit, hybrid model and V-I equations for N-P-N transistor (CE configuration)

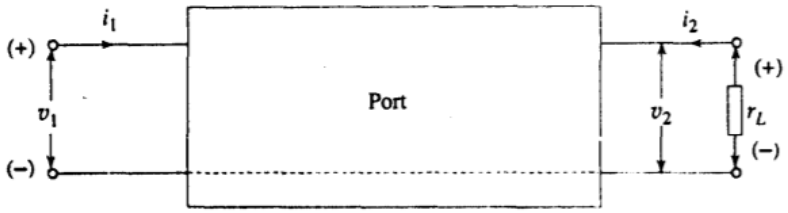
The circuit and equations shown in the figure are valid either for N-P-N or P-N-P transistors and independent of the type of load or method of biasing.

Performance of a Transistor in h-Parameters

We shall study the performance of a transistor in CE configuration in respect of its :

- Input impedance

- Current gain
- Voltage gain
- Power gain
- Output admittance



Input Impedance (Z_{in}). The input impedance is the ratio of input voltage to the input current.

In figure, input voltage is v_1 and input current is i_1. The input impedance

$$Z_{in} = v_1/i_1 \qquad \text{(i)}$$

We know, in terms of h-parameters

$$v_1 = h_{11}.i_1 + h_{12}.v_2$$

Hence putting the value of v_1 in Eq. (i)

We get

$$Z_{in} = \frac{h_{11}.i_1 + h_{12}.v_2}{i_1} = h_{11} + \frac{h_{12}.v_2}{i_1} = h_{11} + h_{12}.\frac{v_2}{i_1}$$

Further, in terms of h-parameters

$$i_2 = h_{21}.i_1 + h_{22}.v_2 \qquad \text{(ii)}$$

If A.C. load resistance is r_L, $i_2 = -v_2/r_L$ the minus sign is used to indicate that the direction of i_2 is opposite to the marked direction.

Putting value of i_2 in Eq. (ii) we get

$$-v_2/r_L = h_{21}.i_1 + h_{22}.v_2$$

or $$- h_{21}.i_1 = v_2(h_{22} + 1/r_L)$$

or $$\frac{v_2}{i_1} = \frac{-h_{21}}{h_{22} + 1/r_L} \qquad \text{(iii)}$$

Again, substituting this value in the expression for Z_{in}, we got above

$$Z_{in} = h_{ie} - \frac{h_{re}.h_{fe}}{h_{oe} + 1/r_L}$$

Current Gain (A_I). Current gain is the ratio of output current to input current.

See figure above.

$$A_i = i_2/i_1 \qquad \text{(iv)}$$

Now $i_2 = h_{21}.i_1 + h_{22}.v_2$ (in terms of h parameters)

$= h_{21}.i_1 + h_{22}(-i_2r_1)$ $\qquad (v_2 = -i_2r_L)$

or $i_2 = h_{21}.i_1 - h_{22}.r_L.i_2$

or $i_2(1+h_{22} \times r_L) = h_{21}.i_1$

or $$\frac{i_2}{i_1} = \frac{h_{21}}{1+h_{22}xr_L} \qquad \text{(v)}$$

or $$A_i = \frac{h_{21}}{1+h_{22}xr_L}$$

Substituting the values in h-parameters in CE configuration,

$$A_i = \frac{h_{fe}}{1+h_{oe}.r_L}$$

If $h_{oe}.r_L << 1$ then current gain = h_{fe}.

Voltage Gain (A_v). The voltage gain is the ratio of output voltage to input voltage.

Refer above figure again

$$A_v = v_2/v_1 \qquad \text{(vi)}$$

From input circuit

$$Z_{in} = v_2/i_1 \quad \text{or, } v_1 = i_1.Z_{in}$$

Thus $$A_v = v_2/i_1.Z_{in} = (v_2/i_1)(1/Z_{in}) \qquad \text{(vii)}$$

Now $$\frac{v_2}{i_1} = \frac{-h_{21}}{h_{22}+1/r_L} \qquad \text{(See Eq. iii)}$$

Putting this value in Eq. (vii)

$$A_v = \frac{-h_{21}}{\left(h_{22}+\frac{1}{r_L}\right).Z_{in}}$$

Substituting the values in h-parameters in CE configuration

$$A_v = \frac{-h_{fe}}{(h_{oe}+1/r_L).Z_{in}}$$

Power Gain (P_i). Power gain can be found by the product of current and voltage gains.

Power gain = current gain x voltage gain

Output admittance. The output impedance can be determined by using two assumptions $Z_L = \infty$ and $V_s = 0$.

Y_0 is defined as i_2/v_2 with $z_l = \infty$

But $$i_2 = h_f i_1 + h_0 v_2$$

Dividing by v_2

$$\frac{i_2}{v_2} = Y_0 = \frac{h_f i_1}{V_2} + h_0 \qquad (1)$$

From the equivalent circuit with $V_s = 0$,

$$r_s i_1 + h_i i_1 + h_f V_2 = 0$$

Here r_s = internal resistance of the source

V_s = open circuit signal voltage

Dividing by V_2 through out, we get

$$\frac{r_s i_1}{v_2} + \frac{h_i i_1}{V_2} + h_r = 0$$

or $$\frac{i_1}{V_2} = \frac{-h_r}{h_i + r_s} \qquad (2)$$

Substitute this value in the equation for Y_0 or equation (1)

$$Y_0 = h_f \left(\frac{-h_r}{h_i + r_s} \right) + h_0$$

$\therefore$ $$Y_0 = h_0 - \frac{h_f h_r}{h_i + r_s}$$

Limitations of h-parameters

- It is very difficult if not impossible to get accurate values of h-parameters for a transistor. The reason is that the h-parameters are subject to variations due to temperature, operating point and from unit to unit.
- A transistor behaves as a "two port" network for small signals only, hence h-parameters can be used to analyze only the small signal (i.e. single stage amplifiers).

Example

The h-parameters of a transistor in CE configurations are:

$h_{ie} = 1000\ \Omega$, $h_{re} = 3.5 \times 10^{-4}$, $h_{fe} = 55$, *and* $h_{oe} = 20\ \mu$ *mho*

If the load $r_L = 2$ *K, find current and voltage gains.*

Solution

(i) $$A_i = \frac{h_{fe}}{1 + h_{oe}.r_L} = \frac{55}{1 + (20x10^{-6}.2x10^3)} = 52.88$$

(ii) For finding voltage gain, first we find Z_{in}.

$$Z_{in} = h_{ie} - \frac{h_{re}xh_{fe}}{h_{oe} + 1/r_L} = 1000 - \frac{(3.5x10^{-4})x55}{(20x10^{-6}) + 1/(2x10^3)} = 962.98$$

Now, keeping the value of Z_{in} in the expression

$$A_v = \frac{-h_{fe}}{(h_{oe} + 1/r_L).Z_{in}} = \frac{-55}{[(20x10^{-6}) + 1/(2x10^3)]x962.8} = -112.2$$

The negative sign shows the 180^0 phase reversal between input and output.

Problem

Following figure shows the circuit of a single stage CE amplifier.

The values of h-parameters are $h_{ie} = 1.5\ k\Omega$, $h_{re} = 5 \times 10^{-3}$, $h_{fe} = 50$, $h_{oe} = 2 \times 10^{-5}\ \mu A/V$. *Determine the following*

(i) Current gain

(ii) Input resistance

Example

For the emitter follower (CC amplifier) with $R_s = 0.5\ k\Omega$ *and* $R_L = 5\ k\Omega$, *calculate* A_i, R_i, A_v. *Assume* $h_{fe} = 50$, $h_{ie} = 1\ k\Omega$, $h_{oe} = 25\ \mu A/volt$.

Solution

(i) Current gain

$$A_i = \frac{1 + h_{fe}}{1 + h_{oe}R_L} = \frac{1 + 50}{1 + 25x10^{-6}x5x10^3} = 45.33$$

(ii) Input resistance

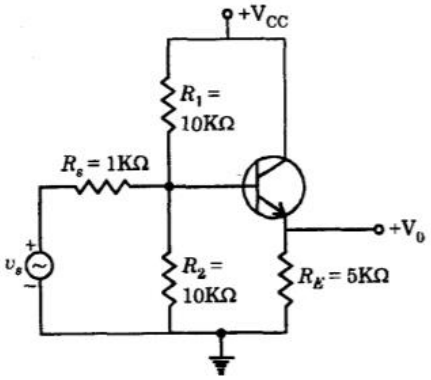
$$R_i = h_{ic} + h_{rc}A_iR_L$$

$$R_i = h_{ic} + 1.A_iR_L = h_{ie} + A_iR_L$$

$$R_i = 1x10^3 + 45.33x5x10^3 = 228.6\,k\Omega$$

(iii) $$A_v = \frac{v_o}{v_i} = \frac{A_i R_L}{R_i} = \frac{45.33x5}{227.6} = 0.9958$$

Following figure shows the circuit of common collector amplifier or emitter follower. The h parameters are h_{ic} = 2 kΩ, h_{fc} = -51, h_{rc} = 1 and h_{oc} = 25 x 10^{-6} mho. Determine the following (i) current gain (ii) input resistance (iii) voltage gain (iv) output resistance.



Answer: A_i = 45.3, R_i = 228 kΩ, Z_i = 4.9 kΩ, A_v = 1, R_0 = 58.8 Ω, Z_o = 581.1 Ω

Example

A BJT has h_{ie} = 2 kΩ, h_{fe} = 100, h_{re} = 2.5 x 10^{-4} and h_{oe} = 25 μA/V as parameters in CE configuration. It is used as an emitter follower (CC amp.) with R_s = 1 kΩ and R_L = 500 Ω. Determine for the amplifier, the voltage gain $A_{Vs} = V_o/V_s$, the current gain $A_{is} = I_o/I_s$, the input resistance R_i and output resistance R_o.

Solution

For the emitter follower (i.e. common-collector amplifier) transistor parameters are given as under:

$$h_{ic} = h_{i.e.} = 2\ k\Omega$$

$$h_{fc} = -(1 + h_{fe}) = -(1 + 100) = -101$$

$$h_{rc} = 1 - h_{re} = 1 - 2.5 \times 10^{-4} = 0.99975 = 1$$

$$h_{oc} = h_{oe} = 25 \times 10^{-6}$$

Current gain $$A_i = \frac{-h_{fc}}{1 + h_{oc} R_L} = \frac{-101}{1 + 25x10^{-6}(500)} = 99.75$$

Input resistance

$$R_{in} = h_{ic} - \frac{h_{rc} h_{fc}}{h_{oc} + \frac{1}{R_L}} = 2x10^3 - \frac{1x(-101)}{25x10^{-6} + \frac{1}{500}} = 51.876\,k\Omega$$

Voltage gain $A_v = \dfrac{-h_{fc}}{\left(h_{oc} + \dfrac{1}{R_L}\right)R_{in}} = \dfrac{-(-101)}{\left(25x10^{-6} + \dfrac{1}{500}\right)x51.876x10^{3}} = 0.9614$

Overall voltage gain

$$A_{vs} = A_v \frac{R_{in}}{R_{in} + R_s} = 0.9614.\frac{51.876}{51.876+1} = 0.9432$$

Overall current gain

$$A_{is} = A_i \frac{R_s}{R_{in} + R_s}$$

$$A_{vs} = 99.75.\frac{1}{51.876+1} = 1.886$$

Output conductances

$$G_o = h_{oc} - \frac{h_{fc}h_{rc}}{h_{ic} + R_s} = 25x10^{-6} - \frac{(-101x1)}{2x10^{3} + 1x10^{3}} = 33.69x10^{-3}$$

Output resistance

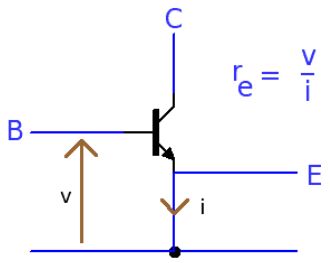
$$R_o = \frac{1}{G_o} = \frac{1}{33.69x10^{-3}} = 29.68\Omega$$

r_e Hybrid Model

The primary function of a "model" is to predict the behaviour of a device in a particular operating region. At DC the bipolar junction transistor (BJT) works in either the cut-off or saturation regions (as a switch).

In the AC domain (audio frequencies) operation is quite different and the transistor works in the linear operating region. The r_e model reflects the operation of the BJT at mid-frequencies and is sufficiently accurate. The r_e model is an equivalent circuit that can be used to predict performance.

Small r_e is the resistance looking into the emitter terminal of a transistor. As there is a voltage on the base of a transistor and a current flowing in the emitter, then from ohm's law $r_e = v/i$, see diagram below.



If the BJT is working in the linear region of its characteristic curves and base emitter junction is forward biased, then r_e can be defined as:

$$r_e = \frac{V_{BE}}{I_E}$$

The base emitter junction acts the same as a conducting diode and has an exponential relationship between the current and voltage in the forward region. The following equation can now be used to find an approximate value for r_e:

$$r_e = \frac{KT}{qI_E}$$

where:
K is Boltzman's constant 1.38 x 10^{-23} joule/K
T is absolute temperature in Kelvin (K = 273 + °C)
q is electronic charge 1.602 x 10^{-19} coulombs

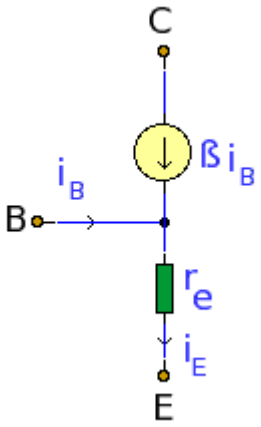
At room temperature r_e equates to 25 / I_E at 20 °C and 26 / I_E at 30 °C, see below:

$$r_e = \frac{25}{I_E} \quad @\ 20°\ C$$

$$r_e = \frac{26}{I_E} \quad @\ 25°\ C$$

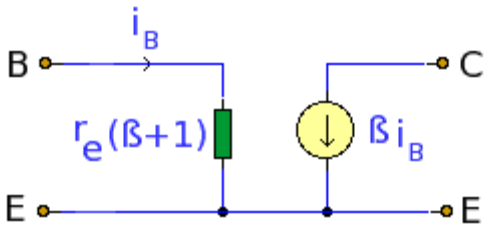
As I_E is approximately the same as I_C some text books quote r_e as 25 / I_C. It is important that I_E is measured in milliamps and to use the appropriate ambient temperature to calculate r_e.

In any BJT, the collector current i_c, is equal to the product of the base current, i_b multiplied by the small signal forward current gain, h_{fe} or β of the transistor. Thus βi_b can be thought of as a constant current generator. The equivalent circuit is shown below:



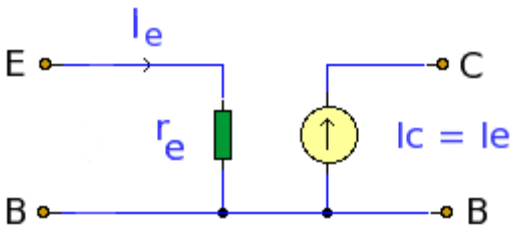
This model is quite accurate provided the DC conditions are evaluated to find the quiescent point of the circuit. Just one parameter is required which can be measured or taken from the manufacturers data sheet. Separating the above diagram and arranging in common emitter, the r_e model is drawn below:

Common Emitter r_e Model



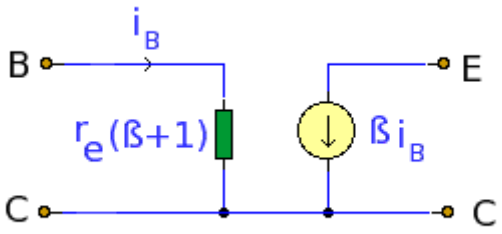
The output equivalent circuit between terminals C and E is now a constant current generator.
The input impedance is between terminals B and E and has a value of:

Common Base r_e Model



In common base the input signal is applied between B and E terminals and has the value:

Common Collector r_e Model



In common collector (emitter follower) the input impedance is:
The r_e model can be used to quickly estimate input impedance, gain and operating conditions of transistor circuits.
The r_e model is sufficiently accurate and only requires one parameter h_{fe}. Input impedance is derived from just one parameter, h_{fe}. However the r_e model does not have parameters for output admittance or reverse voltage ratio and contains no capacitance. As such it is only suitable at dc and mid-frequencies. For high frequency work the hybrid-pi model must be used.

POWER AMPLIFIERS

Class A power amplifier with resistive and transformer coupled load - calculation of efficiency - Class B - Push pull - complementary symmetry - efficiency calculation - Class C Power Amplifier - Class AB operation and Class D type of operation - distortion in power amplifiers - Thermal stability of power amplifier

LARGE SIGNAL AMPLIFIERS

Large signal amplifiers also known as power amplifiers are capable of providing large amount of power to the load**.** They are used as last stage in electronic systems. A power amplifier takes the d.c. power supply connected to the output circuit and converts it into a.c. signal power. Output power is controlled by input signal.

Important Features of Power Amplifiers:

- Some of the features of power amplifiers are
- Impedance matching with the load is necessary for delivering max power to the load.
- Power transistors are needed. (To withstand large voltages and currents)

- Power amplifiers are bulk.
- Due to the non–linear characteristics of transistors, Harmonic Distortions are available at the output.

Performance parameters:

The performance of power amplifiers are determined by the following points.

1. **Circuit efficiency:** Also known as conversion efficiency or overall efficiency.

$$\eta = \frac{\text{Max a.c. o/p power}}{\text{d.c. i/p power}}$$

   Its value may be anywhere from 25% to 90%

2. **Distortion:** The difference between the output & input of an amplifier is known as distortion. Even though the output is enlarged and faithful reproduction of input but in actual practice there may be differences in the waveforms or frequencies.

   (1) Harmonic or amplitude distortion – Due to nonlinearity in transistor.

   (2) Crossover distortion – occurs when transistors not operating in correct phase with each other.

3. **Power Dissipation capacity:** It's defined as the ability to dissipate the heat by the power transistor. Also known as power rating. During amplification process large current passes through power transistor hence Heat generated.By connecting a metal sheet (Heat sink) power dissipation capability can be increased.

Classification of power amplifiers:

Based on Transistor biasing and amplitude of input signal

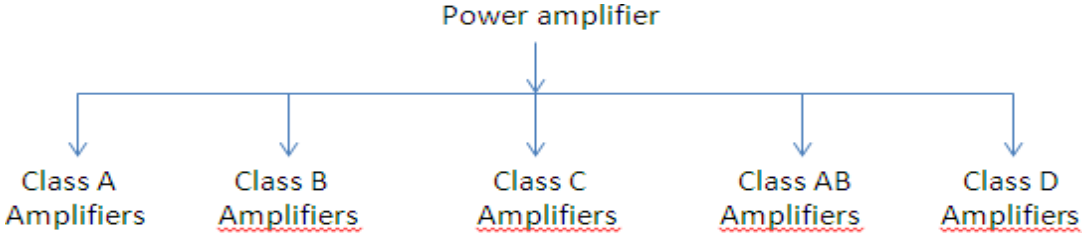


Fig (1) classification of power amplifiers

CLASS A POWER AMPLIFIER:

A power amplifier is called Class A amplifier if the transistor used in the circuit conducts for fullcycle of the input signal.

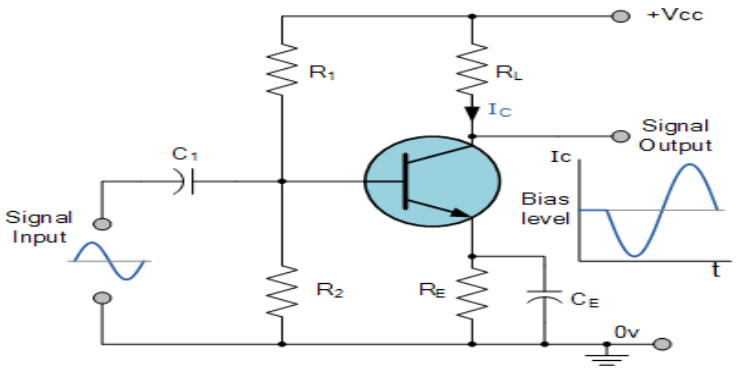


Fig (2) Class A Power amplifier

The operating point(Q) is selected approximately at the (Biased) centre, so that the output current faithfully follows the input signal. The transistor remains in the **active region** for the full input signal. Transistor is not operated in **Cut off** or **Saturation region**. Transistor conducts for full 360·as shown in Fig

the collector current also flows for full 360· Or full cycle. The base current changes sinusoidally, above and below to the quiescent base current. The collector output current also changes sinusoidally above and below the quiescent current value. They are in phase with each other. Due to this **Ic** change, **Vce** will also change sinusoidally as shown in Fig (3) but out of phase 180. Input is amplified faithfully without any distortions.Since transistor is operatedin active region continuously the collector current and voltage are high.This high collector output produces large power which is dissipated as heat.Hence the efficiency of Class A power amplifier is Low.

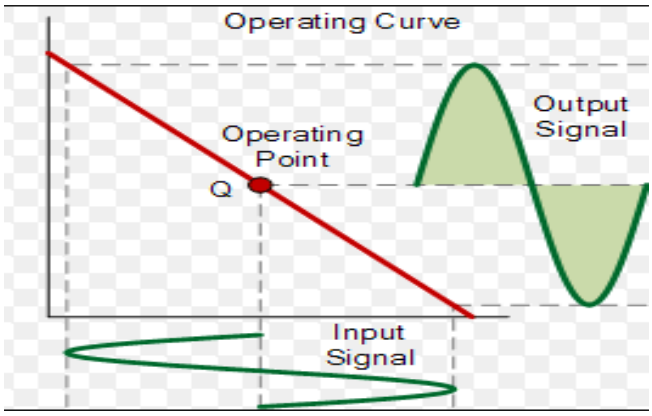


Fig (3): Load line analysis

Advantages: (1) simple construction

(2) Distortion less output voltage

Disadvantage: (1) very low efficiency (25%)

(2) Large power dissipation in the transistors.

(3) Output Impedance is very large.

Expressions: $I_{BQ} = (V_{CC} - 0.7)/R_B$

$I_{CQ} = \beta I_{BQ}$

$V_{EQ} = V_{CC} - I_{CQ} R_L$

Q point at

(V_{CEQ},

I_{CQ}) Pdc

= V_{CC}

I_{CQ}

$P_{ac} = ((V_{max} - V_{min})(I_{max} - I_{min}))/8$

Efficiency %η = (P_{ac}

/P_{dc})*100 Power dissipation

$P_d = P_{dc} - P_{ac}$

TRANSFORMER COUPLED CLASS A POWER AMPLIFIER:

Instead of connecting the load directly, the output is connected to the load through a transformer as shown in Fig (4). This set up is used for Impedance matching. This circuit can be useful for low impedance loads like Loudspeakers. By adjusting the turn's ratio (N1\N2) the output impedance is matched with the load impedance.

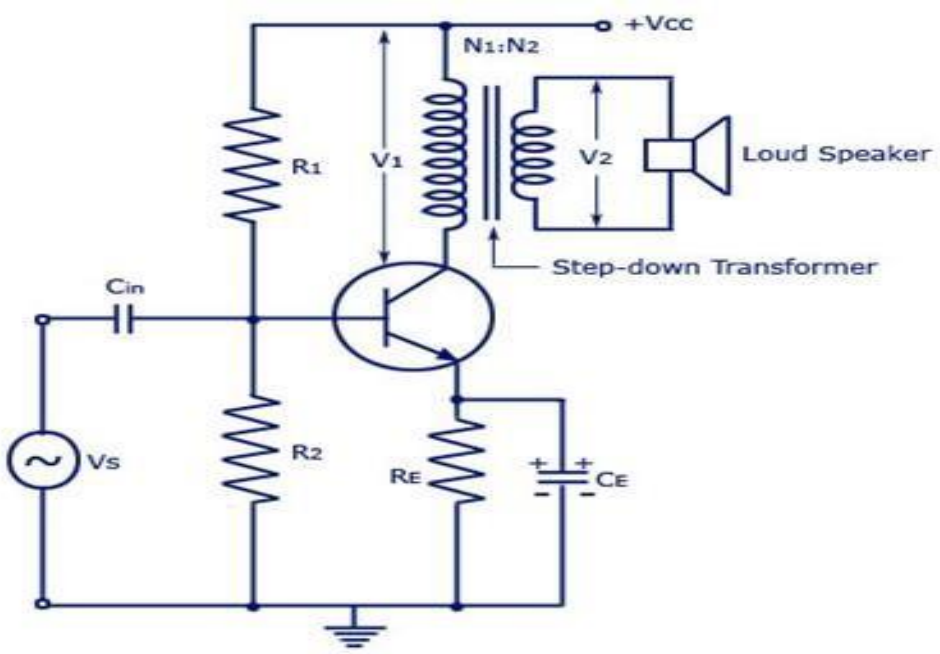


Fig (4): Transformer coupled power amplifier

This type is also known as Single ended Class A amplifier. The primary has negligible d .c. resistance hence no loss of d.c. power.This gives the necessary d.c. isolation to load.

Advantages:

- Max power transfer is done.
- Dc biasing current is doesn't flow through the load so power is saved.
- High efficiency when compared with direct coupled class A amplifier.

Disadvantage:

- Circuit design is complicated.
- Circuit is bulky and expensive.
- Due to saturation of transformer core ,secondary induced voltage is zero And primary current becomes very large.

Expressions: $R_L' = [N_1/N_2]^2 R_L$

Q point (V_{CC}, I_{CQ}),

$I_{CQ} = \beta I_{BQ}$ Pdc

$= V_{CC} I_{CQ}$

$P_{ac} = ((V_{max} - V_{min})(I_{max} - I_{min}))/8$

Efficiency $\%\eta = (P_{ac}/P_{dc})*100.$

$\%\eta$ max = 50%

Power dissipation $P_d = P_{dc}$

$= V_{CC} I_{CQ}$ Impedance

matching is possible Slope

of dc load line ideally ∞

Class B Power Amplifier:

The output power is obtained for one half cycle of input only. Refer Figure (4). The collector current flows for 180 degrees only. For this the Q point is adjusted so that it is in cut off region (refer figure 5& 6).

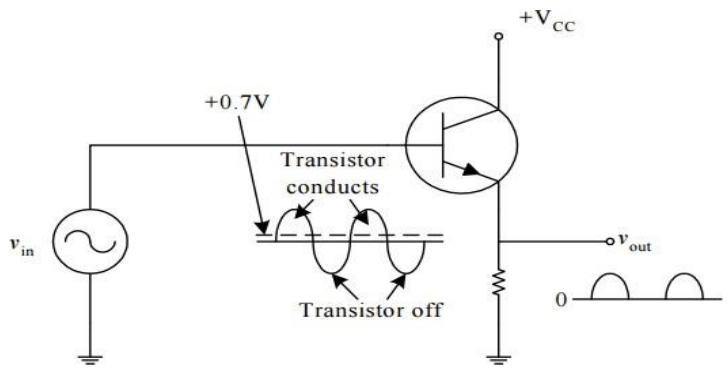


Fig (5) : Class B amplifier.

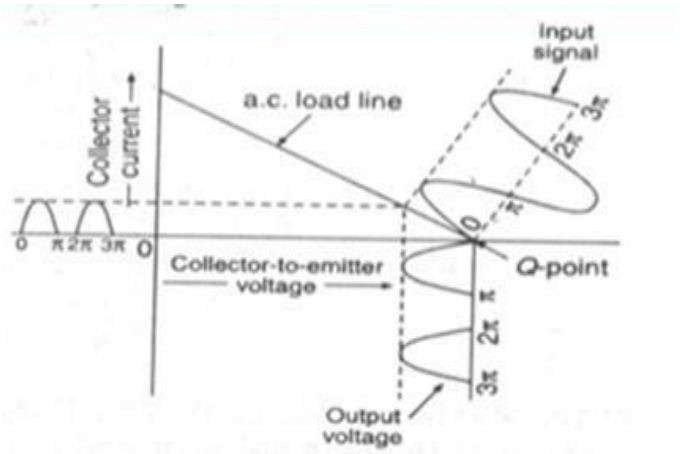


Fig (6) : Class B Operation

The transistor conducts one half cycle only for the positive half cycle of the input and in Negative cycle of input the transistor goes into Off state. Thus collector current flows only for one half cycle. Since the transistor conducts for one half cycle of the input the power dissipation of these class B amplifiers are very less. Hence efficiency gets increased.

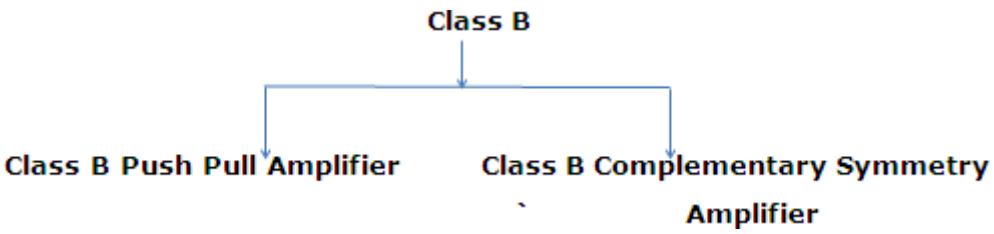
Advantages:

- Impedance with load is possible.
- Second harmonic get automatically cancelled.
- Zero power dissipation.
- High efficiency compared with class A amplifiers.

Disadvantage:

Crossover distortion is present in the output waveform. Since, the transistor is biased at cut off region the waveform is distorted near zero crossings.

Efficiency is not so high.



Push Pull Amplifier - If both the transistors are of same type (NPN or PNP)
Complementary Symmetry- If one of the transistors is NPN & the other one PNP or vice versa.

CLASS B PUSH PULL POWER AMPLIFIER:

In class B amplifier output collector current flows only for half cycle for full cycle of the input hence distortion. To get out for full input signal we use Push Pull circuit. Two transformers are used in Push pull amplifiers.one at the input and the other at the load side. Both are centre tapped transformers. As shown in Fig 7 it also contains two transistors Q1 & Q2 both NPN type. Since centre tapped is used Q1 & Q2 are 180 degrees out of phase.(the voltages are equal

but with opposite polarity). For positive half cycle Q1(Active region) gives output (shown in fig(7 & 8)) and Q2 is OFF(cut off region). In negative cycle Q2 is ON & Q1 is OFF. Thus at the output we get a full cycle for a full input signal.

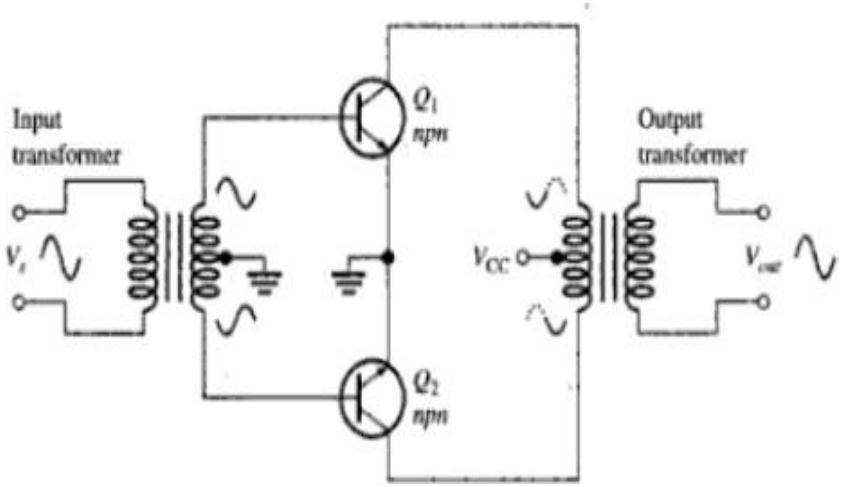


Fig (7) : Class B Push Pull Circuit

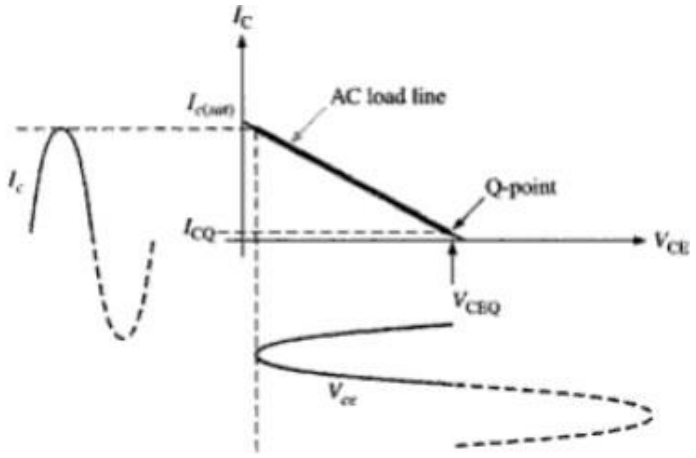


Fig (8) : Class B Push Pull Circuit operation for half cycle

Advantages:

- Efficiency is much higher than class A Amplifier
- Even harmonics get cancelled so harmonic distortion is less.
- Ripples in supply voltage are eliminated

Disadvantage:

- Two centre tapped transformers are necessary
- Hence circuit is bulky and costs more.

- Frequency response is poor.

CLASS B COMPLEMENTARY SYMMETRY AMPLIFIER:

The circuit diagram for complementary symmetry type is shown in Figure(8)**.** This circuit uses two transistors of different type. One is NPN and another PNP. It is a transformer less circuit. For better impedance matching the tow transistors Q1 & Q2 are connected as emitter follower configuration. Positive half cycle Q1 is in Active region so ON & Q2 in cut off So OFF. In negative half cycle Q2 is ON & Q1 is OFF. Thus for a complete input cycle output is developed as shown in figure 8.The difference between complementary symmetry and push pull models is in complementary model there is no output transformer.

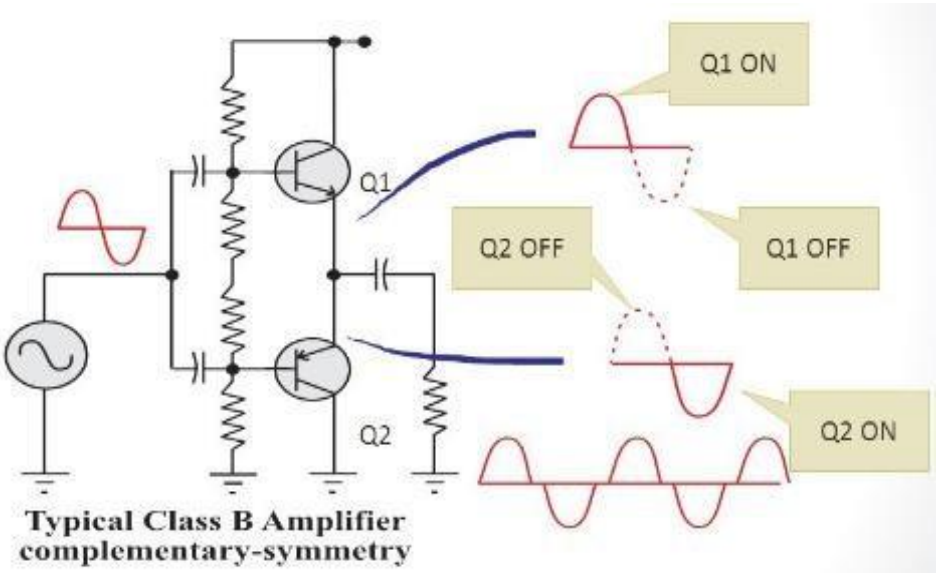


Fig (8): Class B Complementary symmetry Circuit operation

Analysis:

Note: All results for push pull amplifiers are applicable for complementary symmetry model. Only change is replace R_L' with real load R_L value. (Since, no output transformer is used).

Advantages:

- As transformer less circuit the weight and cost is less

- Due to common collector (emitter follower) impedance matching is possible.
- Frequency response is good.
- Value of efficiency is higher than push pull amplifier.

Disadvantage:

- Circuit needs two separate voltage supplies.
- Output is distorted due to crossover Distortion.
- It is necessary that both transistors Q1 & Q2 have matched characteristics.

Comparison of Push Pull & Complementary Symmetry circuits:

S No	Parameter	Push Pull	Complementary symmetry
1	Type of Transistor	Both should be of NPN or PNP type	One is PNP and other NPN
2	Use of transformers	Used at both i/p & o/p side	Not needed
3	Impedance matching	Possible due to use of two transformers	Possible due to operation of transistors in CC configuration
4	Transistor Configuration	Both transistors Operates in CE mode	Both transistors Operates in CC mode
5	Conduction Angle	180º	180º
6	Power dissipation when no input is present	Zero	Zero
7	Efficiency	Low	Higher than Push Pull type.

CLASS C AMPLIFIERS:

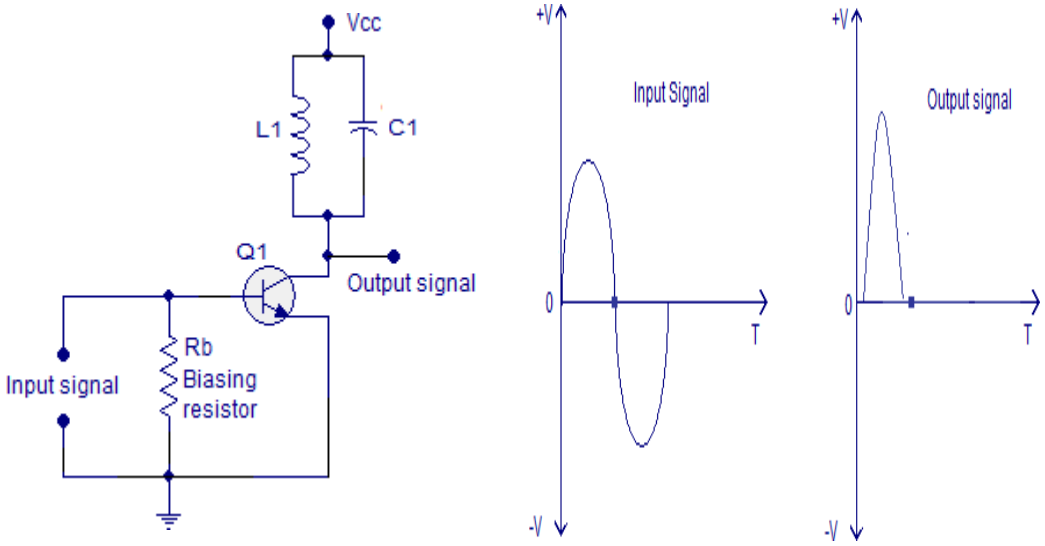


Fig (9) Class Circuit & operations

In class C the transistor conducts for less than one half cycle period of the input i.e around 80º to 120º angle. This reduced conduction angle increases the efficiency (Theoretically around 90 %). But this kind of operation causes large distortions. Hence, it is not used in Audio applications. Tuned circuit is used as load as shown in Figure(9).

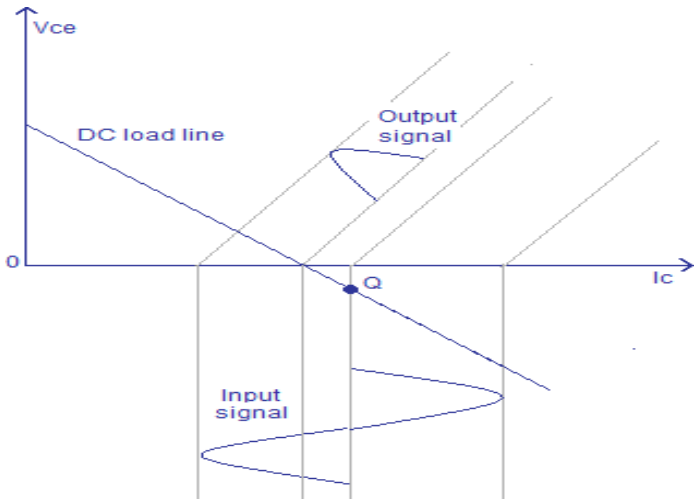


Fig (10): Class Circuit & operations

When the input signal is applied the tuned circuit starts resonating at the frequency of the input signal. Transistor produces a series of current pulses based on the input. By selecting Proper L1, C1 resonance can be achieved. This resonance frequency is extracted by the tuned load at the output. Harmonics can be eliminated by adding filters to the circuit shown in figure (9). The biasing resistance pulls the q point below Cut off region. Hence the transistor conducts only after the input amplitude is greater than the base emitter voltage. (Refer figure 9 & 10)

Advantages:

- Less Physical size.
- Used in RF applications.
- High Efficiency (higher than 95%)
- Low power loss in power transistors

Disadvantage:

- Creates lot of RF Interference.
- Selection of ideal Inductors is problem.
- Not suitable in Audio applications.

Applications: Tuned amplifiers**,** RF amplifiers, oscillators, Booster amplifiers, and High Frequency repeaters.

CLASS D AMPLIFIERS:

Class D type is designed to work with pulse or digital input signals. The Input V_{in} is compared with saw tooth wave (known as chopping wave) and accordingly a pulse waveform is generated (refer figure 11) which is fed to the amplifier.

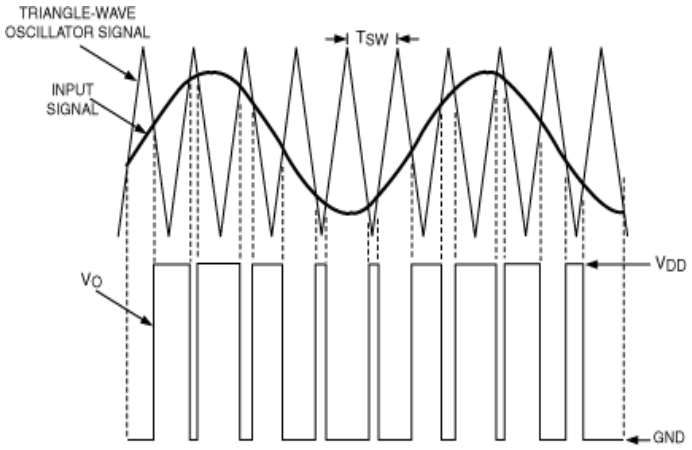


Fig (11): Class D operation

The circuit diagram of class D amplifier is shown in Figure 12.Input is applied to the non-inverting terminal of the comparator and the saw tooth wave is applied to the inverting terminal. Based on this the comparator produces an output pulse width modulated waveform and this PWM wave is amplified by the amplifier as shown in figure 11. Transistor in the amplifier circuit just acts as a switch and hence the power loss is very less. Low pass filter converts the pulse wave back into sinusoidal signal.At the output thus we have sinusoidal signal.

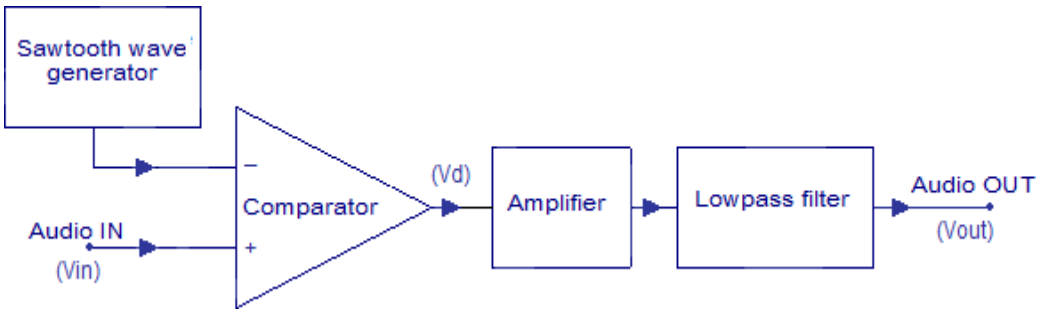


Fig (12): Class D circuit diagram

Efficiency: Transistor operates in saturation region when turned on .So V_{ce} is small. This is the reason for class D amplifiers have very high efficiency (Around 90%).

Advantages:

- High efficiency

- Possible to amplify the digital signals and analog signals as well.

CLASS AB AMPLIFIERS:

To eliminate cross over distortion in Class B Push Pull Amplifiers the Biasing of transistors can be done. This arrangement moves the transistor Q point slightly above the cut off region. Usually voltage divider bias is used as shown in Figure13 (a).Due to temperature changes V_{BE} also changes, hence no stable biasing. To avoid this we go for diode biasing as shown in figure 13.b.if D1, D2 matches with the transistor characteristics then we get a stable biasing. The d.c. voltage at the diode is connected to the transistors. (d.c. biasing).This value is equal to cut in voltage, hence conducts for full half cycle of the input. All analysis for class B holds good for class AB power amplifier.

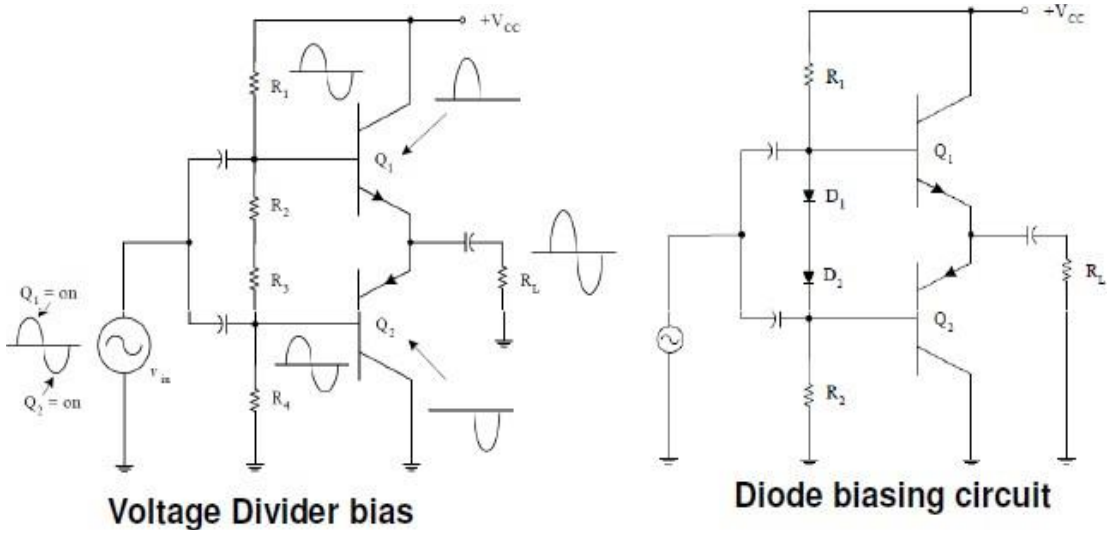


Fig (13 a): Class AB circuit diagram with Fig (13 b): Class AB circuit diagram with Voltage divider biasdiagram with Diode biasing

Distortions in amplifiers:

If the output of an amplifier is not a complete sine wave, then it is distortion. It can be analysed by using Fourier analysis.in this method any distorted periodic waveform can be broken down into different frequencycomponents. These components are harmonics of the fundamentalfrequency.Harmonics are integer multiples of a fundamental frequency (F). For example, 1st harmonic is 1 x F kHz.

TYPES OF DISTORTION

Amplitude or Non Linear distortion:

Due to the non-linearity of transistor (nonlinear dynamic characteristics of transistor) the output is different from the input. This kind of distortion is known as amplitude distortion or harmonic or non-linear distortion.

Harmonic distortion %D = (A_n/A_1)*100

Frequency Distortion:

When different frequency components of the input signal are amplified differently frequency amplification takes place.This is mainly due to the internal capacitance effect of the transistors.

Delay or Phase shift distortion:

If the phase shift introduced by amplifier is not proportional to the frequency then phase distortion takes place.

Note: For more information please refer the class notes.

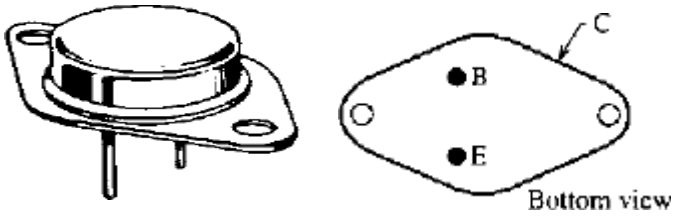
THERMAL STABILITY:

Average power of a transistor depends on the collector base junction. It is around 150 to 200º. If the temperature exceeds this limit then transistor get physically damaged.Performance of transistor depends on the ability of transistor to dissipate the heat generated in base collector junction. This can be achieved by

- ✓ Operating the transistor in safe region (proper biasing).
- ✓ By effectively removing the heat to the surrounding air quickly.

To remove the heat we use **Heat sinks**. The concept of **Heat Sink** is to keep the junction of the power device (transistor) to below a maximum operating temperature.

Heat sinks: All power devices come in complete package where there is a metal contact which connects the external heat sink to the metal surface of the device. (Usually to the collector terminal)



Fig(14) :Heat Sink(a) Top view (b) Bottom view

In figure 14(b) B – Base , E – Emitter & C – Collector terminal. From the above figure 14(b) we can notice that the Collector is connected to the metal top (chasis or heat sink) which has more area than Base & Emitter. So the heat generated at the output junction(collector junction) is dissipated fast. If more number of devices are connected to the same sink the INSULATORS are needed to shield individually. Usually Nylon material is used to ensure.

Note: For Problems and more details on quantitative analysis refer class notes.

Reference Books:

1. Donald. L, Schilling and C.Belove, “Electronic Circuits - Discrete and Integrated”, 3rd Edition, McGraw Hill, 1989.
2. David A. Bell, “Electronic Devices and Circuits”, PHI, 1998.
3. Gupta. J.B, “Electronic Devices and Circuits”, Katson Publishers, 2009.

2 Marks Questions

1. What is Class AB operation?
2. Define the conversion efficiency of a power amplifier. What is its value for a class C power amplifier?
3. What is cross over distortion? How it can be eliminated?
4. Define thermal resistance.
5. What is meant harmonic distortion?
6. What is the drawback of class B amplifier
7. What is the difference between Class B and Class AB amplifier
8. State the types of distortions in amplifier.
9. What is the advantage of using transformer for a class A amplifier?
10. What is the difference between a voltage amplifier and a power amplifier?
11. State important features of power amplifiers.

12 Marks Questions

1. For the transformer coupled class A power amplifier circuit derive the expression for its efficiency.
2. Prove that the maximum efficiency of class A transformer coupled amplifier is 50% and that of class B type is 78.5%.
3. Draw the circuit of push pull class B amplifier coupled using transformers and explain the operation. Prove that all the even harmonics get eliminated. What is the assumption made for this?
4. Write notes on distortions in amplifiers and give the solutions to avoid the same.
5. Explain the operation of class D amplifier with suitable diagram.
6. Explain the operation of class C amplifier with neat circuit arrangement.

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SCHOOL OF SCIENCE AND HUMANITIES

DEPARTMENT OF PHYSICS

UNIT – III - Digital and Analog Electronics – SPH1216

UNIT 3 - Feedback & Oscillator Circuits and Operational Amplifiers

Effect of positive and negative feedbacks, basic feedback topologies & their properties, Analysis of feedbacks, Sinusodial Oscillators (RC, LC and Crystal), Multivibrators, The 555 timer, Op-Amp Basics, practical Op-Amp circuits, differential and Common mode operation, Inverting & Non Inverting Amplifier, differential and cascade amplifier, Op-Amp applications.

OSCILLATORS

Principle of Oscillators

An **oscillator** is a circuit which produces a continuous, repeated, alternating waveform without any input. **Oscillators** basically convert unidirectional current flow from a DC source into an alternating waveform which is of the desired frequency, as decided by its circuit components.

Classification of Oscillators

1. Based on operating principle

   a) Negative resistance effect oscillators

   b) Feedback oscillators

2. Based on type of output waveform

   a) Sinusoidal oscillators (Harmonic oscillators)

   b) Non-sinusoidal oscillators (Relaxation oscillators)

3. Based on frequency generation

   a) Audio Frequency (AF) oscillators (20 Hz to 20 kHz)

   b) Radio Frequency (RF) oscillators (20 kHz to 30 MHz)

   c) Very High Frequency (VHF) oscillators (30 MHz to 300 MHz)

   d) Ultra High Frequency (UHF) oscillators (300 MHz to 3 GHz)

   e) Microwave oscillators (300 MHz to 300 GHz)

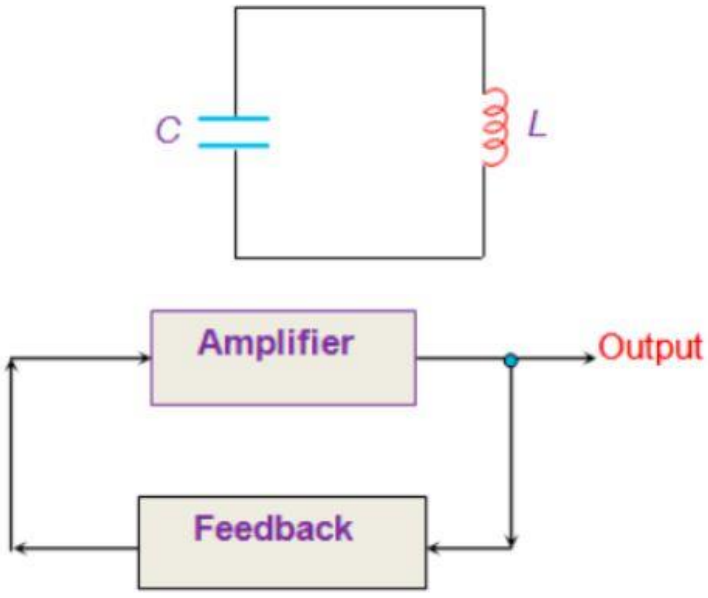
4. Based on the circuit employed

   a) RC oscillators b) LC oscillators

The different types of oscillators are mentioned below and some of them are explained.

- ✓ Armstrong Oscillator
- ✓ Crystal Oscillator
- ✓ Hartley oscillator
- ✓ RC Phase Shift Oscillator
- ✓ Colpitts Oscillators
- ✓ Cross-Coupled Oscillator
- ✓ Dynatron Oscillator
- ✓ Meissner Oscillator
- ✓ Optoelectronic Oscillator
- ✓ Phase Shift Oscillator
- ✓ Wine Bridge Oscillator
- ✓ Robinson Oscillator
- ✓ Tri-Tet Oscillator

The basic principle behind the working of oscillators can be understood by analyzing the behavior of an LC tank circuit shown in Figure, which employs an inductor L and a completely pre-charged capacitor C as its components.

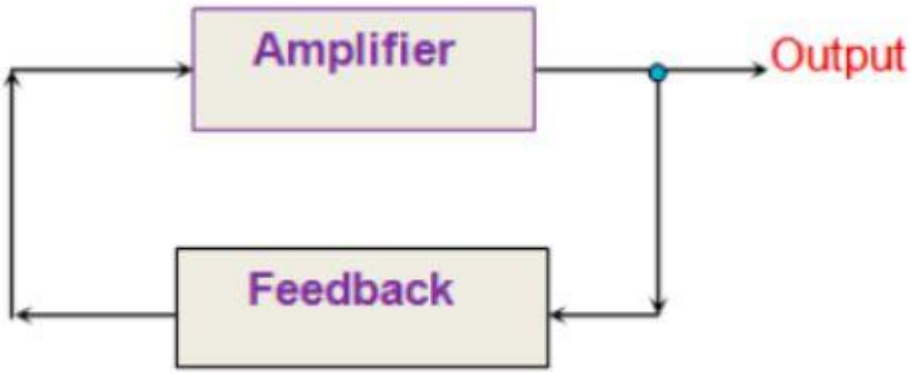


Practically, the **oscillators** are nothing but the amplifier circuits which are provided with a positive or regenerative feedback wherein a part of the output signal is fed back to the input. Here the amplifier consists of an amplifying active element which can be a transistor or an Op-Amp and the back-fed in-phase signal is held responsible to keep-up (sustain) the oscillations by making-up for the losses in the circuit.

The expression for the closed-loop gain of the oscillator

$$G = \frac{A}{1 + A\beta}$$

- ✓ Where A is the voltage gain of the amplifier and β is the gain of the feedback network.
- ✓ Here, if $A\beta > 1$, then the oscillations will increase in amplitude, while if $A\beta < 1$, then the oscillations will be damped.
- ✓ On the other hand, $A\beta = 1$ leads to the oscillations which are of constant amplitude.
- ✓ In other words, this indicates that if the feedback loop gain is small, then the oscillation dies-out, while if the gain of the feedback loop is large, then the output will be distorted; and only if the gain of feedback is unity, then the oscillations will be of constant amplitude leading to self-sustained oscillatory circuit.



$$V_i = V_s + V_f$$

$$V_i = V_s + \beta V_o$$

$$V_f = \beta V_o$$

$$V_o = A V_i$$

$$V_o = A(V_s + \beta V_o)$$

$$V_o = AV_s + \beta V_o A$$

$$V_o - A\beta V_o = AV_s$$

$$V_o[1 - A\beta] = AV_s$$

$$\frac{V_o}{V_s} = \frac{A}{1 - A\beta}$$

gain with positive feedback ← $A_f = \frac{V_o}{V_s} = \frac{A}{1 - A\beta}$

→ Amplifier becomes an oscillator

$$\frac{A}{1 - A\beta} = \infty$$

$$1 - A\beta = 0$$

$$A\beta = 1$$ → condition for oscillator

→ Barkhausen criteria

① product of open loop gain (A) + feedback (β) is equal to 1

$$|A\beta| = 1$$

② Net phase shift around the loop must be equal, 0° or 360°

$$\angle A\beta = 0^\circ \text{ or } 360^\circ$$

RC PHASE-SHIFT OSCILLATORS

RC phase-shift oscillators use resistor-capacitor (RC) network (Figure 1) to provide the phase-shift required by the feedback signal. They have excellent frequency stability and can yield a pure sine wave for a wide range of loads.

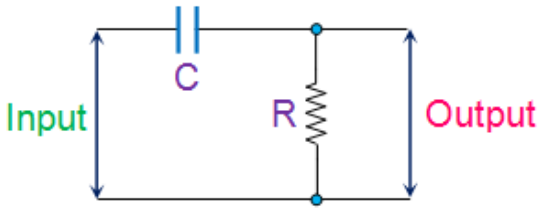


Figure 1 RC Phase-Shift Network

- Where, $X_C = 1/(2\pi f_C)$ is the reactance of the capacitor C and R is the resistor.
- In oscillators, these kind of RC phase-shift networks, each offering a definite phase-shift can be cascaded so as to satisfy the phase-shift condition led by the Barkhausen Criterion.
- In the case of **RC phase-shift oscillator** is formed by cascading three RC phase-shift networks, each offering a phase-shift of 60°, as shown by Figure 2

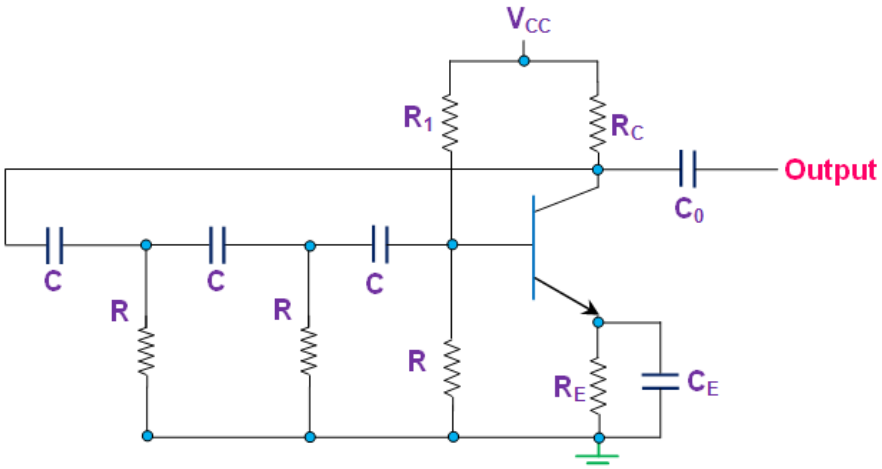


Figure 2 RC Phase-Shift Oscillator Using BJT

- the collector resistor RC limits the collector current of the transistor, resistors R_1 and R (nearest to the transistor) form the voltage divider network while the emitter resistor R_E improves the stability.
- Next, the capacitors C_E and C_o are the emitter by-pass capacitor and the output DC decoupling capacitor, respectively. Further, the circuit also shows three RC networks employed in the feedback path.
- The arrangement causes the output waveform to shift by 180° during its course of travel from output terminal to the base of the transistor.
- Next, this signal will be shifted again by 180° by the transistor in the circuit due to the fact that the phase-difference between the input and the output will be 180° in the case of common emitter configuration.

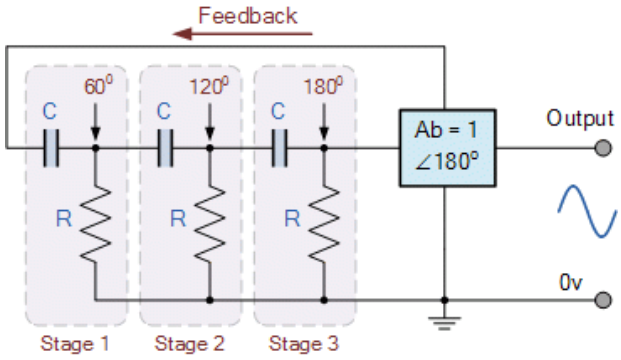
- This makes the net phase-difference to be 360°, satisfying the phase-difference condition.
- One more way of satisfying the phase-difference condition is to use four RC networks, each offering a phase-shift of 45°.
- Hence it can be concluded that the **RC phase-shift oscillators** can be designed in many ways as the number of RC networks in them is not fixed.

  However it is to be noted that, although an increase in the number of stages increases the frequency stability of the circuit, it also adversely affects the output frequency of the oscillator due to the loading effect.

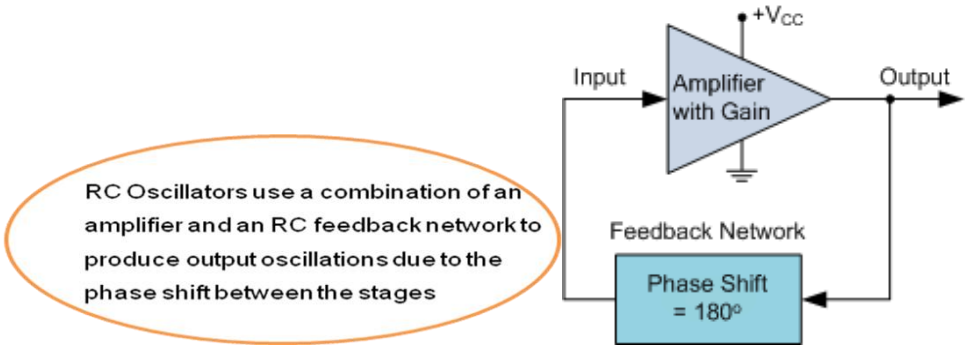
  The generalized expression for the frequency of oscillations produced by a **RC phase-shift oscillator** is given by

$$f = \frac{1}{2\pi RC\sqrt{2N}}$$

Where, N is the number of RC stages formed by the resistors R and the capacitors C.



- ✓ we can configure transistor stages to operate as oscillators by placing resistor-capacitor (RC) networks around the transistor to provide the required regenerative feedback without the need for a tank circuit.
- ✓ Frequency selective RC coupled amplifier circuits are easy to build and can be made to oscillate at any desired frequency by selecting the appropriate values of resistance and capacitance.



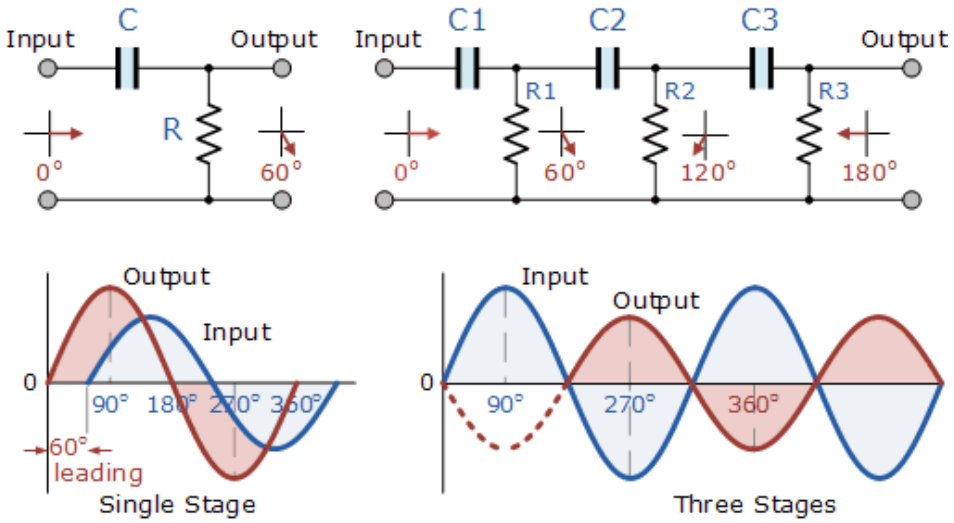
For an RC oscillator to sustain its oscillations indefinitely, sufficient feedback of the correct phase, that is positive (in-phase) Feedback must be provided along with the voltage gain of the single transistor amplifier being used to inject adequate loop gain

into the closed-loop circuit in order to maintain oscillations allowing it to oscillates continuously at the selected frequency.

In an **RC Oscillator** circuit the input is shifted 180º through the feedback circuit returning the signal out-of-phase and 180º again through an inverting amplifier stage to produces the required positive feedback.

- ✓ This then gives us "180º + 180º = 360º" of phase shift which is effectively the same as 0º, thereby giving us the required positive feedback.
- ✓ In other words, the total phase shift of the feedback loop should be "0" or any multiple of 360º to obtain the same effect.

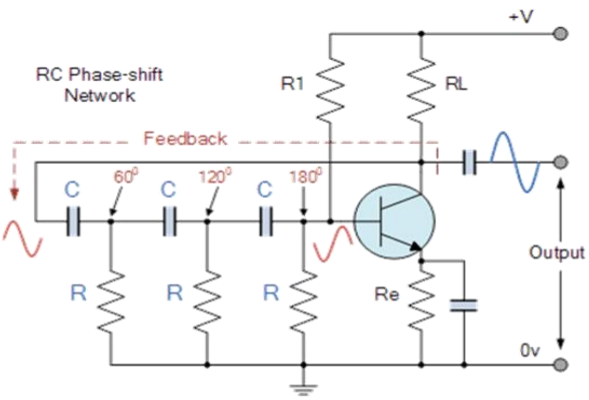
In a **Resistance-Capacitance Oscillator** or simply known as an **RC Oscillator**, we can make use of the fact that a phase shift occurs between the input to a RC network and the output from the same network by using interconnected RC elements in the feedback branch



RC Phase-Shift Network

- ✓ The circuit on the left shows a single resistor-capacitor network whose output voltage "leads" the input voltage by some angle less than 90º.
- ✓ In a pure or ideal single-pole RC network. it would produce a maximum phase shift of exactly 90º, and because 180º of phase shift is required for oscillation, at least two single-poles networks must be used within an *RC oscillator* design.
- ✓ However in reality it is difficult to obtain exactly 90º of phase shift for each RC stage so we must therefore use more RC stages cascaded together to obtain the required value at the oscillation frequency.
- ✓ The amount of actual phase shift in the circuit depends upon the values of the resistor (R) and the capacitor (C), at the chosen frequency of oscillations with the phase angle (φ) being given as:

- The basic **RC Oscillator** which is also known as a **Phase-shift Oscillator**, produces a sine wave output signal using regenerative feedback obtained from the resistor-capacitor (RC) ladder network.
- This regenerative feedback from the RC network is due to the ability of the capacitor to store an electric charge, (similar to the LC tank circuit).



This resistor-capacitor feedback network can be connected as shown above to produce a leading phase shift (phase advance network) or interchanged to produce a lagging phase shift (phase retard network) the outcome is still the same as the sine wave oscillations only occur at the frequency at which the overall phase-shift is 360°.

By varying one or more of the resistors or capacitors in the phase-shift network, the frequency can be varied and generally this is done by keeping the resistors the same and using a 3-ganged variable capacitor because capacitive reactance (X_C) changes with a change in frequency as capacitors are frequency-sensitive components. However, it may be required to re-adjust the voltage gain of the amplifier for the new frequency.

If the three resistors, R are equal in value, that is $R_1 = R_2 = R_3$, and the capacitors, C in the phase shift network are also equal in value, $C_1 = C_2 = C_3$, then the frequency of oscillations produced by the RC oscillator is simply given as:

$$f_r = \frac{1}{2\pi RC\sqrt{2N}}$$

Where:
f_r is the oscillators output frequency in Hertz
R is the feedback resistance in Ohms
C is the feddback capacitance in Farads
N is the number of RC feedback stages.

- ✓ Since the resistor-capacitor combination in the **RC Oscillator** ladder network also acts as an attenuator, that is the signal reduces by some amount as it passes through each passive stage.
- ✓ It could be assumed that the three phase shift sections are independent of each other Thus the voltage gain of the amplifier must be sufficiently high enough to overcome these passive RC losses.

Advantages RC Oscillator Circuit

- ✓ It is constructed with cheap and simple components

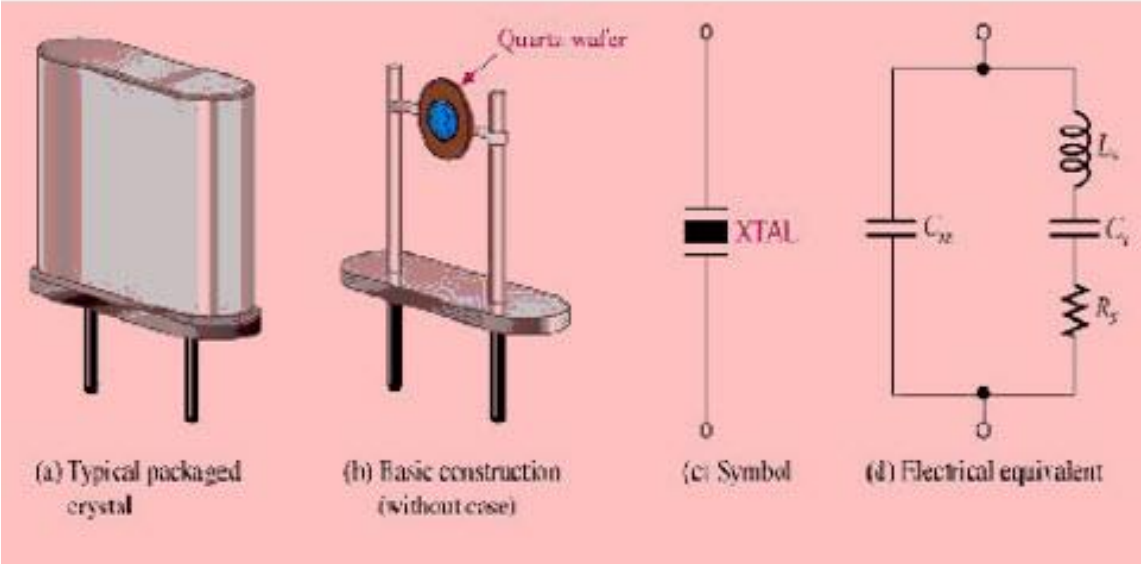
- ✓ It can be made to operate at very low frequencies as compared with Hartley's and Colpit's oscillator
- ✓ The frequency of oscillation depends on R and C
- ✓ Therefore a wide range of frequencies may be obtained using this oscillator

CRYSTAL OSCILLATORS

A crystal oscillator is an electronic oscillator circuit that uses the mechanical resonance of a vibrating crystal of piezoelectric material to create an electrical signal with a constant frequency. This frequency is often used to keep track of time, as in quartz wristwatches, to provide a stable clock signal for digital integrated circuits, and to stabilize frequencies for radio transmitters and receivers. A crystal oscillator relies on the slight change in shape of a quartz crystal under an electric field, a property known as electrostriction or inverse piezoelectricity.

A voltage applied to an electrode on the crystal causes it to change shape; when the voltage is removed, the crystal generates a small voltage as it elastically returns to its original shape.

Crystal Oscillator Circuit and Working



Piezoelectric Effect is the ability of certain materials to generate an electric charge in response to applied mechanical stress.

Crystal oscillators operate on the principle of inverse piezoelectric effect in which an alternating voltage applied across the crystal surfaces causes it to vibrate at its natural frequency. It is these vibrations which eventually get converted into oscillations.

These oscillators are usually made of Quartz crystal, eventhough other substances like Rochelle salt and Tourmaline exhibit the piezoelectric effect because, quartz is inexpensive, naturally-available and mechanically-strong when compared to others

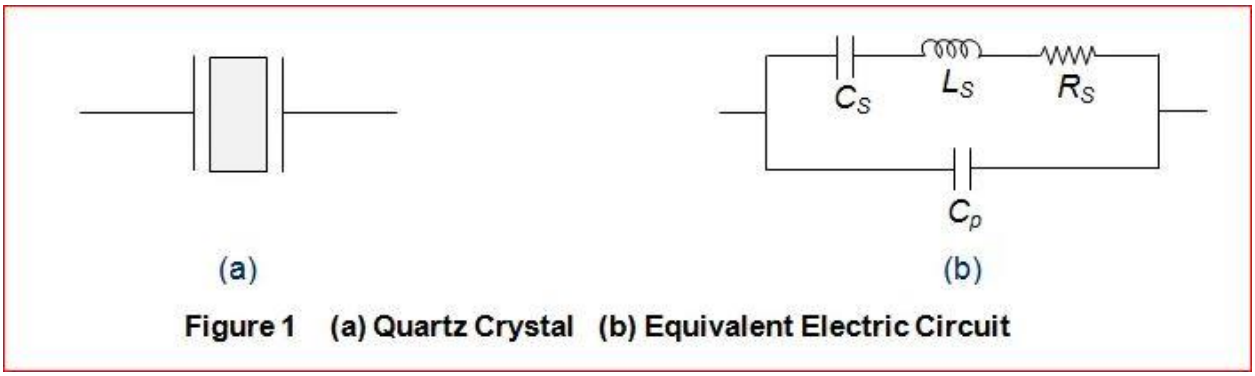
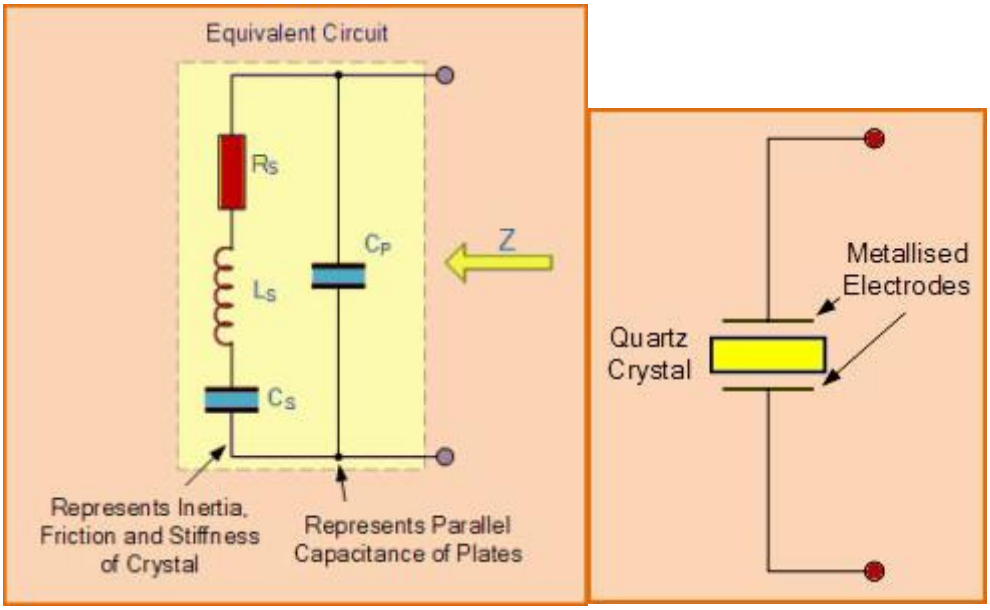


Figure 1 (a) Quartz Crystal (b) Equivalent Electric Circuit

The quartz crystal oscillator circuit diagram can be represented as follows:



atoms, molecules, ions are packed in an order in three spatial dimensions with repeating pattern to form a solid that can be called as a crystal.

The crystal can be made by almost any object that is made of elastic material by using appropriate electrical transducers. As every object consists of natural resonant frequency of vibration, steel consists of high speed of sound and is also very elastic.

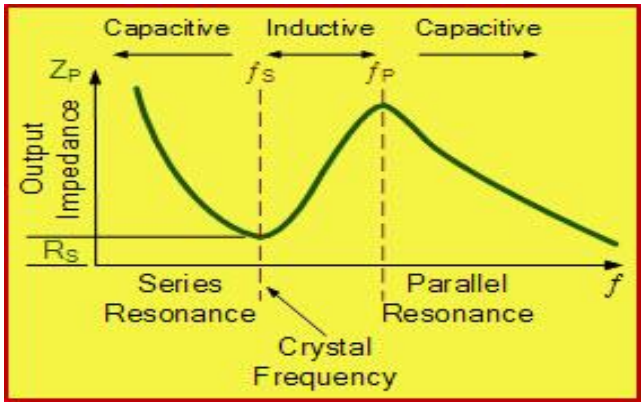
a mechanical deformation is produced by applying an electric field across certain materials. Thus, it utilizes the vibrating crystal's mechanical resonance which is made of a piezoelectric material for generating an electrical signal of a specific frequency.

These quartz crystal oscillators are highly stable, consists of good quality factor, they are small in size, and are very economical. Hence, quartz crystal oscillator circuits are superior compared to other resonators such as LC circuits, turning forks, and so on. Generally, 8MHz crystal oscillator is used in microprocessors and microcontrollers.

$$f_S = \frac{1}{2\pi\sqrt{L_S C_S}}$$

$$f_p = \frac{1}{2\pi\sqrt{L_S\left(\frac{C_p C_S}{C_p + C_S}\right)}}$$

The quartz crystal oscillator circuit diagram consists of series resonance and parallel resonance, i.e., two resonant frequencies. If the reactance produced by capacitance C1 is equal and opposite to the reactance produced by inductance L1, then the series resonance occurs. The series and parallel resonant frequencies are represented by fs and fp respectively, and the values of fs and fp can be determined



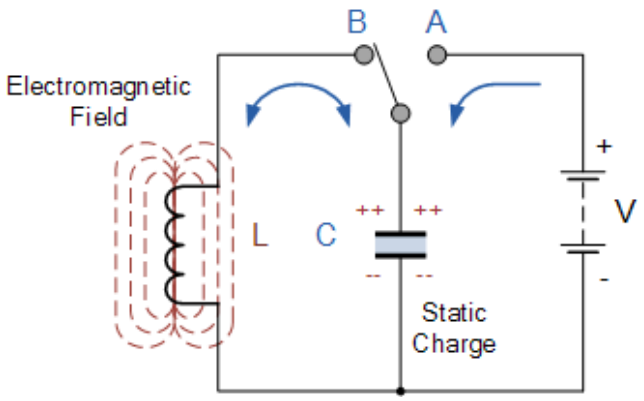
The above figure shows the graph between impedance and frequency of the quartz crystal oscillator circuit. Typically, crystal oscillators are having a frequency range from 32KHz to 200MHz.

Applications

- ✓ Crystal Oscillator in Military and Aerospace - efficient communication system
- ✓ in Research and Measurement - space tracking purpose, in the measuring instruments and medical devices
- ✓ in computers, digital systems, instrumentation, phase locked loop systems, marine, modems, sensors, telecommunications, disk drives
- ✓ engine controlling, stereo, clock and to trip computer, and in GPS system.
- ✓ cable television systems, personal computers, video cameras, toys and video games, radio systems, cellular phones, and so on.

LC OSCILLATOR

LC Oscillator tank circuit



- ✓ The circuit consists of an inductive coil, L and a capacitor, C.

- ✓ The capacitor stores energy in the form of an electrostatic field and which produces a potential (*static voltage*) across its plates, while the inductive coil stores its energy in the form of an electromagnetic field.
- ✓ The capacitor is charged up to the DC supply voltage, V by putting the switch in position A. When the capacitor is fully charged the switch changes to position B.
- ✓ The rising current sets up an electromagnetic field around the coil which resists this flow of current. When the capacitor, C is completely discharged the energy that was originally stored in the capacitor, C as an electrostatic field is now stored in the inductive coil, L as an electromagnetic field around the coils windings.
- ✓ As there is now no external voltage in the circuit to maintain the current within the coil, it starts to fall as the electromagnetic field begins to collapse.
- ✓ A back emf is induced in the coil ($e = -Ldi/dt$) keeping the current flowing in the original direction.
- ✓ This current charges up capacitor, C with the opposite polarity to its original charge. C continues to charge up until the current reduces to zero and the electromagnetic field of the coil has collapsed completely.
- ✓ This process then forms the basis of an LC oscillators tank circuit and theoretically this cycling back and forth will continue indefinitely. However, things are not perfect and every time energy is transferred from the capacitor, C to inductor, L and back from L to C some energy losses occur which decay the oscillations to zero over time.
- ✓ The energy originally introduced into the circuit through the switch, has been returned to the capacitor which again has an electrostatic voltage potential across it, although it is now of the opposite polarity.
- ✓ The capacitor now starts to discharge again back through the coil and the whole process is repeated.
- ✓ The polarity of the voltage changes as the energy is passed back and forth between the capacitor and inductor producing an AC type sinusoidal voltage and current waveform.
- ✓ This oscillatory action of passing energy back and forth between the capacitor, C to the inductor, L would continue indefinitely if it was not for energy losses within the circuit.
- ✓ Electrical energy is lost in the DC or real resistance of the inductors coil, in the dielectric of the capacitor, and in radiation from the circuit so the oscillation steadily decreases until they die away completely and the process stops.

- ✓ The frequency of the oscillatory voltage depends upon the value of the inductance and capacitance in the LC tank circuit.
- ✓ Resonance to occur in the tank circuit, there must be a frequency point were the value of X_C, the capacitive reactance is the same as the value of X_L, the inductive reactance ($X_L = X_C$) and which will therefore cancel out each other out leaving only the DC resistance in the circuit to oppose the flow of current.

✓

$$X_L = 2\pi f L \quad \text{and} \quad X_C = \frac{1}{2\pi f C}$$

at resonance: $X_L = X_C$

$$\therefore \; 2\pi f L = \frac{1}{2\pi f C}$$

$$2\pi f^2 L = \frac{1}{2\pi C}$$

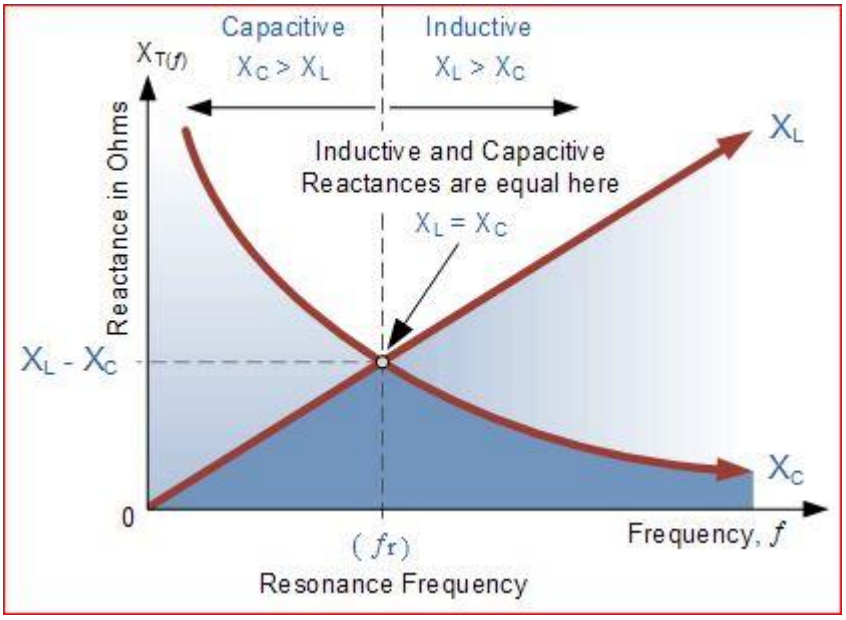
$$\therefore \; f^2 = \frac{1}{(2\pi)^2 LC}$$

$$f = \frac{\sqrt{1}}{\sqrt{(2\pi)^2 LC}}$$

✓

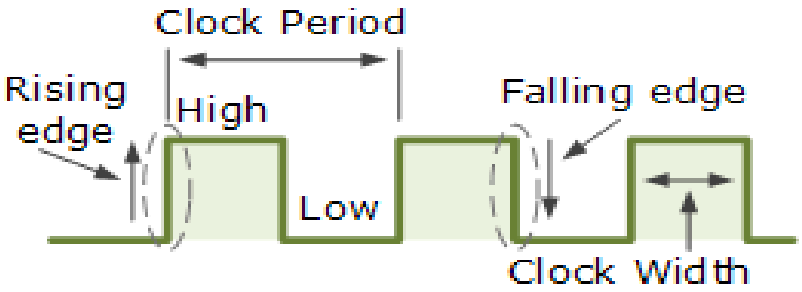
$$f_r = \frac{1}{2\pi\sqrt{LC}}$$

✓



Multivibrators

- Multivibrators are sequential logic circuits that operate continuously between two distinct states of HIGH and LOW
- Clock pulses are generally continuous square or rectangular shaped waveform which are produced by a single pulse generator circuit such as a **Multivibrator**.
- A *multivibrator* circuit oscillates between a "HIGH" state and a "LOW" state producing a continuous output. Astable multivibrators generally have an even 50% duty cycle, that is that 50% of the cycle time the output is "HIGH" and the remaining 50% of the cycle time the output is "OFF". In other words, the duty cycle for an astable timing pulse is 1:1.
- Sequential logic circuits which use a clock signal for synchronization are dependent upon the frequency and therefore the clock pulse width to activate their switching action.
- Sequential circuits can also change their switching state using either the rising edge, falling edge, or both edges of the clock signal as we have seen previously with the basic flip-flop circuits.
- The following list are terms commonly associated with a timing pulse or waveform.



Active HIGH – if the state change occurs from a "LOW" to a "HIGH" on the clock's pulse rising edge or during the clock width.

Active LOW – if the state change occurs from a "HIGH" to a "LOW" on the clock's pulses falling edge.

Clock Width – this is the time during which the value of the clock signal is equal to a logic "1", or HIGH.

Clock Period – this is the time between successive transitions in the same direction, ie, between two rising or two falling edges.

Duty Cycle – this is the ratio of the clock width to the clock period.

Clock Frequency – the clock frequency is the reciprocal of the clock period, frequency = 1/clock period. ($f = 1/T$)

- ✓ Clock pulse generation circuits can be a combination of analogue and digital circuits that produce a continuous series of pulses (these are called Astable multivibrators) or a pulse of a specific duration (these are called Monostable multivibrators).

- ✓ Combining two or more multivibrator circuit provides generation of a desired pattern of pulses (including pulse width, time between pulses and frequency of pulses).

There are basically three types of clock pulse generation circuits:

Astable – A *free-running multivibrator* that has **NO** stable states but switches continuously between two states this action produces a train of square wave pulses at a fixed known frequency.

Monostable – A *one-shot multivibrator* that has only **ONE** stable state as once externally triggered it returns back to its first stable state.

Bistable – A *flip-flop* that has **TWO** stable states producing a single pulse either HIGH or LOW in value.

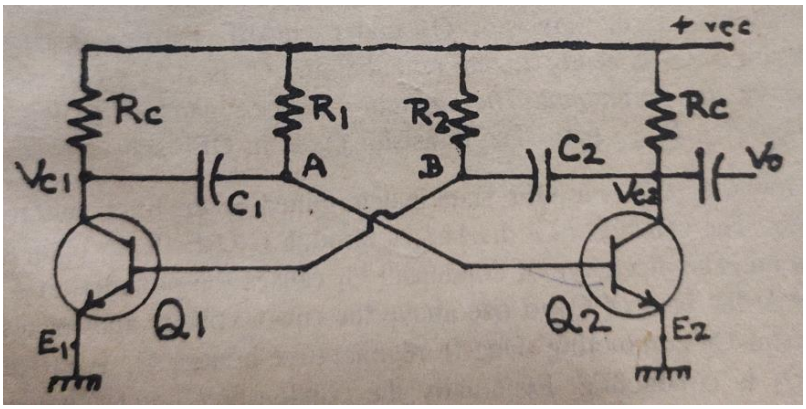
Astable Multivibrator

- ✓ Astable Multivibrator has two quasi stable state

- ✓ It switches from one state to the other in an interval of time, depending upon the discharge of CR – circuit
- ✓ It is an oscillatory circuit – requires no external triggering

CONSTRUCTION

- ✓ The circuit diagram has a two stage RC-coupled amplifier
- ✓ Output of each stage is coupled to the input through the capacitor C1 or C2
- ✓ The cross-coupling arrangement produces a phase change of 180° resultng in a positive feedback – needed for oscillation
- ✓ The amount of feedback is large enough to drive the transistors between cut-off and saturation



The resistance R1/Rc is kept less than current gain of the transistor used.

The O/P is available at the collector – in form of pulses

Working

- ✓ When the circuit is switched ON, collector current flows through both transistors
- ✓ As the circuit is symmetrical equal current flows through the transistor
- ✓ Used transistor is not identical, more current will pass through one of the transistor
- ✓ The current through Q1 will be slightly greater than Q2
- ✓ The collector voltage of Q1 is slightly less than that of Q2
- ✓ This decreases the base current of Q2, since the collector of Q1 is coupled with the base of Q2 through C1
- ✓ As a result the collector current of Q2 is decreased and it's collector voltage increases.

- ✓ Increase the base current of Q1 because of the coupling capacitor C2
- ✓ Inturn increases the collector current of Q1 and the collector voltage of Q1 decreased.
- ✓ The falling collector voltage in Q_1 further decease the base current of Q_2 causing a decrease in collector current.
- ✓ Now Q_1 is in saturation and transistor Q_2 under cut-off
- ✓ The collector Q_1 is nearly at zero potential and Q_2 is at Vcc.
- ✓ The capacitor C_2 gets charged to Vcc volts through Rc_2, The transistor Q2 is in OFF state

The duration in OFF state is determined by the time constant C_1 and R_1

C_1 discharges through C_1Q_1E1 R_1C_1 path, since Q_1 is on.

- ✓ Discharge of condenser C_1 causes the potential at A and the base of Q_2 to raise above the cut-in voltage, makes the transistor Q_2 conducting
- ✓ Now Q_1 is at cut-off and Q_2 is conducting
- ✓ The condenser C1 gets charged to +Vcc through $Rc_1C_1AQ_2E_2Rc_1$
- ✓ As Q2 is conducting, the condenser C2 discharges through C2Q2E2Rc2C2 path, causing the potential at B and hence the base potential of Q1 to raise above the cut-in-voltage.
- ✓ Due to regenerative action, Q1 starts conducting and Q2 is driven to cut off.
- ✓ The condenser C2 is recharged through Rc2BQ1 path again
- ✓ The whole process is repeated.
- ✓ The transistor Q1 and Q2 are alternately switched on and off
- ✓ The O/P taken from any one collector will be a square wave and it will be

complementary in time to the output from the other collector

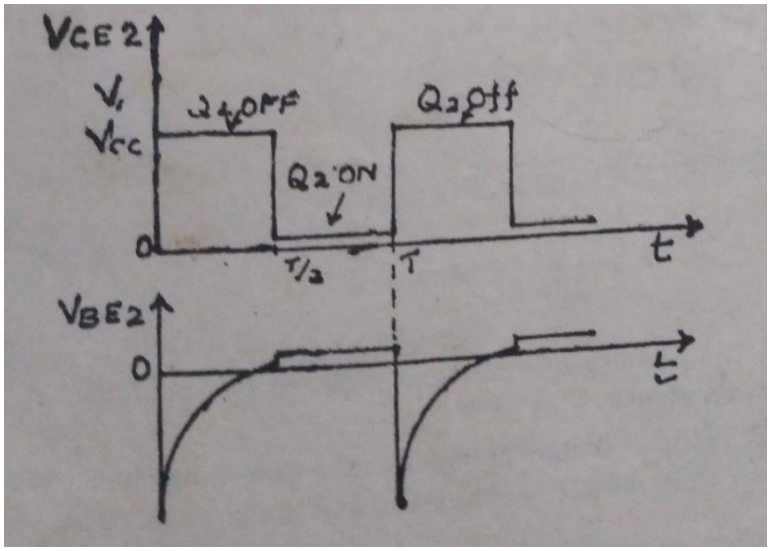
The period of the output wave is given by

$T = 0.69 (R_1C_1 + R_2C_2)$

The frequency of the wave is given by f = 1/t (hertz)

$$f = \frac{1}{0.69(R_1C_1 + R_2C_2)}$$

The output wave form is a square wave as shown



Expression for frequency of the O/P wave

The time period for which the O/P from collector to transistor Q2 is at VCC (giving Vc2 high) is the same as the time for which Q2 is OFF.

This equals the time duration of discharge of the condenser C1 through R1 to make the base potential of Q2 just above the cut-in-voltage of the transistor

The time period is

$$t_1 = 0.69 R_1 C$$

At the end of this interval, Q2 starts conducting and Q1 is in cut-off.

The time for which Q1 is OFF giving Vc2 low is given by

$$t_2 = 0.69 R_2 C_2$$

The total period of one wave in the output is

$$T = t_1 + t_2$$
$$= 0.69(R_1 C_1 + R_2 C_2)\,\text{sec}\,ond$$

The frequency of the wave produced is

$$f = \frac{1}{T}$$

$$f = \frac{1}{0.69(R_1 C_1 + R_2 C_2)}$$

When R1 = R2 = R
and C1=C2=C

$$f = \frac{1}{0.69(RC)} hertz$$

For oscillations to takes place, the transistors must switch from cut-off and in saturation stage and vice versa

To ensure saturation the transistors must have high gain, depending on the value of R1 and Rc

It is necessary that the transistor Q2 is in saturation

Then the collector – emitter voltage = base –emiter voltage in Q2

By approximation

Voltage drop across R1 = Voltage drop across R2

IB2 ∗ R1 = IC2 ∗ Rc2

$$\therefore \left(\frac{Ic_2}{IB_2} \right) = \frac{R_1}{Rc_2}$$

Duty Cycle:

It is defined as the ratio of te duration of the high state to the duration of te period of the output.

For astable multivibrator duty cycle = $\frac{t_1}{t_1 + t_2} or \frac{t_2}{t_1 + t_2}$

If it is equal then,

or 50 % $\frac{t}{2t} or \frac{1}{2}$

Applications

- To produce continuous train of square waves or rectangular waves
  - O/P is square waves it generates harmonic waves
  - Hence called as harmonic generator – got name as multivibrator
  - -Used along with logic gates – Digital Voltameter
  - - d.c to a.c or low voltage d.c to high voltage d.c
  - Switching mode power supply (SMPS) in T.V sets
  - Operates as an oscillator
  - Operates over a wide range of audio and radio frequency

- Multivibrators uses transistors, resistors and capacitors without using coils

OP-AMP - Operational Amplifier

Construction of Operational Amplifier

An op-amp consists of differential amplifier(s), a level translator and an output stage. A differential amplifier is present at the input stage of an op-amp and hence an op-amp consists of **two input terminals**. One of those terminals is called as the **inverting terminal** and the other one is called as the **non-inverting terminal**. The terminals are named based on the phase relationship between their respective inputs and outputs.

Characteristics of Operational Amplifier

The important characteristics or parameters of an operational amplifier are as follows −

- Open loop voltage gain
- Output offset voltage
- Common Mode Rejection Ratio
- Slew Rate

This section discusses these characteristics in detail as given below −

Open loop voltage gain

The open loop voltage gain of an op-amp is its differential gain without any feedback path.

Mathematically, the open loop voltage gain of an op-amp is represented as −

Av=v0v1−v2Av=v0v1−v2

Output offset voltage

The voltage present at the output of an op-amp when its differential input voltage is zero is called as **output offset voltage.**

Common Mode Rejection Ratio

Common Mode Rejection Ratio (**CMRR**) of an op-amp is defined as the ratio of the closed loop differential gain, AdAd and the common mode gain, AcAc.

Mathematically, CMRR can be represented as −

CMRR=AdAcCMRR=AdAc

Note that the common mode gain, AcAc of an op-amp is the ratio of the common mode output voltage and the common mode input voltage.

Slew Rate

Slew rate of an op-amp is defined as the maximum rate of change of the output voltage due to a step input voltage.

Mathematically, slew rate (SR) can be represented as −

SR=MaximumofdV0dtSR=MaximumofdV0dt

Where, V0V0 is the output voltage. In general, slew rate is measured in either V/μSecV/μSec or V/mSecV/mSec.

Types of Operational Amplifiers

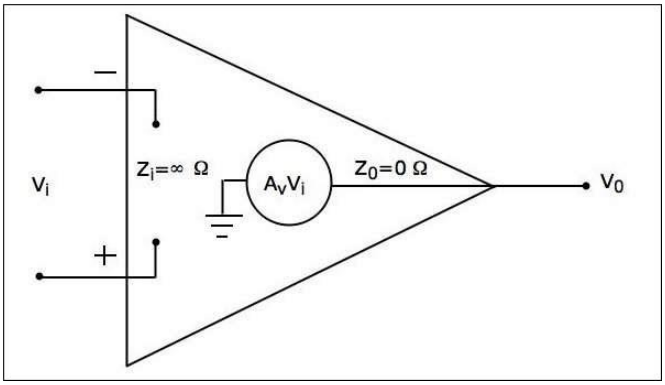
An op-amp is represented with a triangle symbol having two inputs and one output.

Op-amps are of two types: **Ideal Op-Amp** and **Practical Op-Amp**.

They are discussed in detail as given below −

Ideal Op-Amp

An ideal op-amp exists only in theory, and does not exist practically. The **equivalent circuit** of an ideal op-amp is shown in the figure given below −

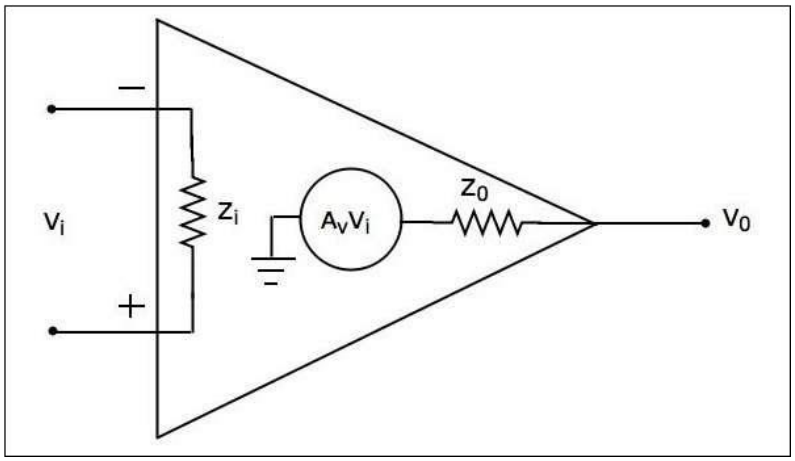


An **ideal op-amp** exhibits the following characteristics −

- Input impedance Zi=∞ΩZi=∞Ω
- Output impedance Z0=0ΩZ0=0Ω
- Open loop voltage gaine Av=∞Av=∞
- If (the differential) input voltage Vi=0VVi=0V, then the output voltage will be V0=0VV0=0V
- Bandwidth is **infinity**. It means, an ideal op-amp will amplify the signals of any frequency without any attenuation.
- Common Mode Rejection Ratio **(CMRR)** is **infinity**.
- Slew Rate **(SR)** is **infinity**. It means, the ideal op-amp will produce a change in the output instantly in response to an input step voltage.

Practical Op-Amp

Practically, op-amps are not ideal and deviate from their ideal characteristics because of some imperfections during manufacturing. The **equivalent circuit** of a practical op-amp is shown in the following figure −



A **practical op-amp** exhibits the following characteristics −

- Input impedance, ZiZi in the order of **Mega ohms**.
- Output impedance, Z0Z0 in the order of **few ohms.**.
- Open loop voltage gain, AvAv will be **high**.

When you choose a practical op-amp, you should check whether it satisfies the following conditions −

- Input impedance, ZiZi should be as high as possible.
- Output impedance, Z0Z0 should be as low as possible.
- Open loop voltage gain, AvAv should be as high as possible.
- Output offset voltage should be as low as possible.
- The operating Bandwidth should be as high as possible.
- CMRR should be as high as possible.
- Slew rate should be as high as possible.

Note − IC 741 op-amp is the most popular and practical op-amp.

-AMP-APPLICATIONS

A circuit is said to be **linear**, if there exists a linear relationship between its input and the output. Similarly, a circuit is said to be **non-linear**, if there exists a non-linear relationship between its input and output.

Op-amps can be used in both linear and non-linear applications. The following are the basic applications of op-amp −

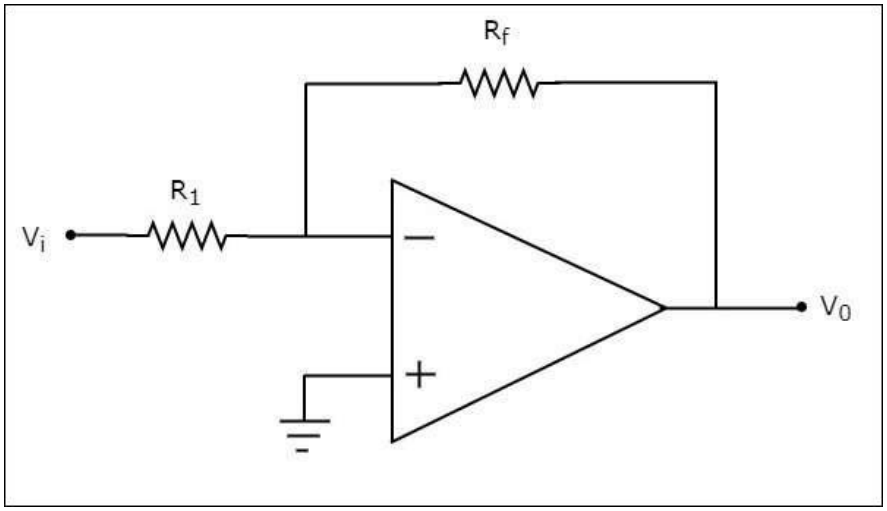
- Inverting Amplifier
- Non-inverting Amplifier
- Voltage follower

This chapter discusses these basic applications in detail.

INVERTING AMPLIFIER

An inverting amplifier takes the input through its inverting terminal through a resistor R1R1, and produces its amplified version as the output. This amplifier not only amplifies the input but also inverts it (changes its sign).

The **circuit diagram** of an inverting amplifier is shown in the following figure −



Note that for an op-amp, the voltage at the inverting input terminal is equal to the voltage at its non-inverting input terminal. Physically, there is no short between those two terminals but **virtually**, they are in **short** with each other.

In the circuit shown above, the non-inverting input terminal is connected to ground. That means zero volts is applied at the non-inverting input terminal of the op-amp.

According to the **virtual short concept**, the voltage at the inverting input terminal of an op-amp will be zero volts.

The **nodal equation** at this terminal's node is as shown below −

$$0-ViR1+0-V0Rf=00-ViR1+0-V0Rf=0$$

$$=>-ViR1=V0Rf=>-ViR1=V0Rf$$

$$=>V0=(-RfR1)Vt=>V0=(-RfR1)Vt$$

$$=>V0Vi=-RfR1=>V0Vi=-RfR1$$

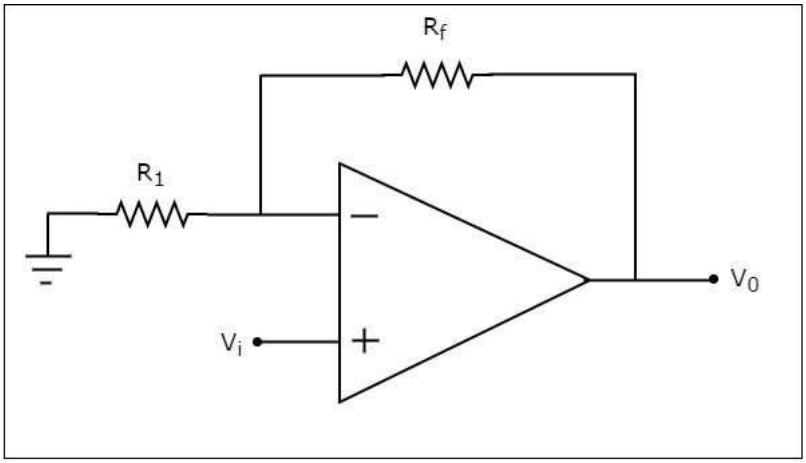
The ratio of the output voltage V0V0 and the input voltage ViVi is the voltage-gain or gain of the amplifier. Therefore, the **gain of inverting amplifier** is equal to −RfR1−RfR1.

Note that the gain of the inverting amplifier is having a **negative sign**. It indicates that there exists a 180^0 phase difference between the input and the output.

NON-INVERTING AMPLIFIER

A non-inverting amplifier takes the input through its non-inverting terminal, and produces its amplified version as the output. As the name suggests, this amplifier just amplifies the input, without inverting or changing the sign of the output.

The **circuit diagram** of a non-inverting amplifier is shown in the following figure −



In the above circuit, the input voltage ViVi is directly applied to the non-inverting input terminal of op-amp. So, the voltage at the non-inverting input terminal of the op-amp will be ViVi.

By using **voltage division principle**, we can calculate the voltage at the inverting input terminal of the op-amp as shown below −

=>V1=V0(R1R1+Rf)=>V1=V0(R1R1+Rf)

According to the **virtual short concept**, the voltage at the inverting input terminal of an op-amp is same as that of the voltage at its non-inverting input terminal.

=>V1=Vi=>V1=Vi

=>V0(R1R1+Rf)=Vi=>V0(R1R1+Rf)=Vi

=>V0Vi=R1+RfR1=>V0Vi=R1+RfR1

=>V0Vi=1+RfR1=>V0Vi=1+RfR1

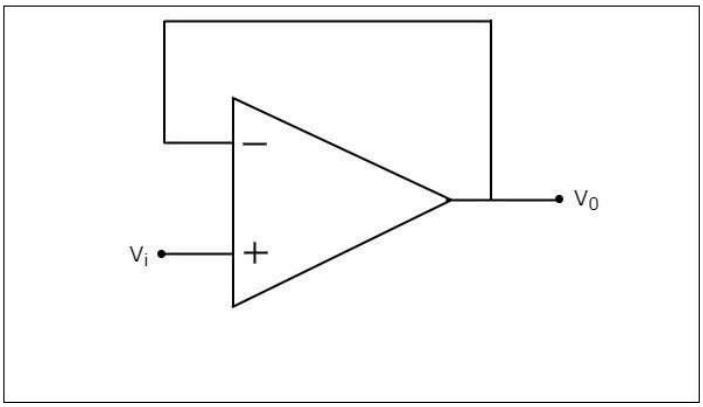
Now, the ratio of output voltage V0V0 and input voltage ViVi or the voltage-gain or **gain of the non-inverting amplifier** is equal to 1+RfR11+RfR1.

Note that the gain of the non-inverting amplifier is having a **positive sign**. It indicates that there is no phase difference between the input and the output.

VOLTAGE FOLLOWER

A **voltage follower** is an electronic circuit, which produces an output that follows the input voltage. It is a special case of non-inverting amplifier.

If we consider the value of feedback resistor, RfRf as zero ohms and (or) the value of resistor, 1 as infinity ohms, then a non-inverting amplifier becomes a voltage follower. The **circuit diagram** of a voltage follower is shown in the following figure −



In the above circuit, the input voltage ViVi is directly applied to the non-inverting input terminal of the op-amp. So, the voltage at the non-inverting input terminal of op-amp is equal to ViVi. Here, the output is directly connected to the inverting input terminal of opamp. Hence, the voltage at the inverting input terminal of op-amp is equal to V0V0.

According to the **virtual short concept**, the voltage at the inverting input terminal of the op-amp is same as that of the voltage at its non-inverting input terminal.

=>V0=Vi=>V0=Vi

So, the output voltage V0V0 of a voltage follower is equal to its input voltage ViVi. Thus, the **gain of a voltage follower** is equal to one since, both output voltage V0V0 and input voltage ViVi of voltage follower are same.

Arithmetic Circuits

In the previous chapter, we discussed about the basic applications of op-amp. Note that they come under the linear operations of an op-amp. In this chapter, let us discuss about arithmetic circuits, which are also linear applications of op-amp.

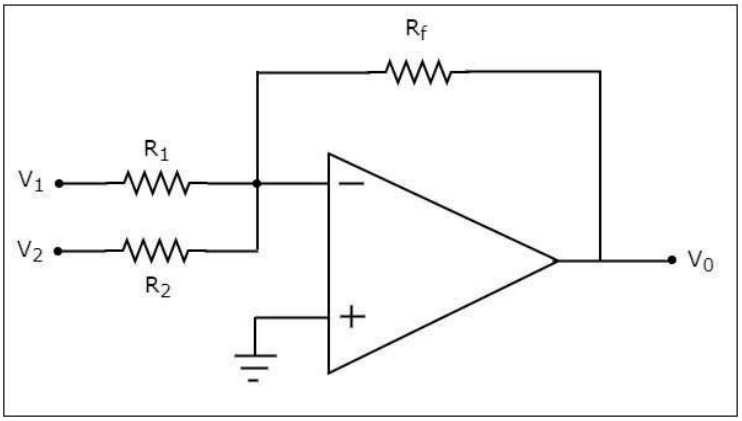
The electronic circuits, which perform arithmetic operations are called as **arithmetic circuits**. Using op-amps, you can build basic arithmetic circuits such as an **adder** and a **subtractor**. In this chapter, you will learn about each of them in detail.

ADDER

An adder is an electronic circuit that produces an output, which is equal to the sum of the applied inputs. This section discusses about the op-amp based adder circuit.

An op-amp based adder produces an output equal to the sum of the input voltages applied at its inverting terminal. It is also called as a **summing amplifier**, since the output is an amplified one.

The **circuit diagram** of an op-amp based adder is shown in the following figure −



In the above circuit, the non-inverting input terminal of the op-amp is connected to ground. That means zero volts is applied at its non-inverting input terminal.

According to the **virtual short concept**, the voltage at the inverting input terminal of an op-amp is same as that of the voltage at its non-inverting input terminal. So, the voltage at the inverting input terminal of the op-amp will be zero volts.

The **nodal equation** at the inverting input terminal's node is

$$0-V1R1+0-V2R2+0-V0Rf=00-V1R1+0-V2R2+0-V0Rf=0$$

$$=>V1R1-V2R2=V0Rf=>V1R1-V2R2=V0Rf$$

$$=>V0=Rf(V1R1+V2R2)=>V0=Rf(V1R1+V2R2)$$

If Rf=R1=R2=RRf=R1=R2=R, then the output voltage V0V0 will be −
$V0=-R(V1R+V2R)V0=-R(V1R+V2R)$

$$=>V0=-(V1+V2)=>V0=-(V1+V2)$$

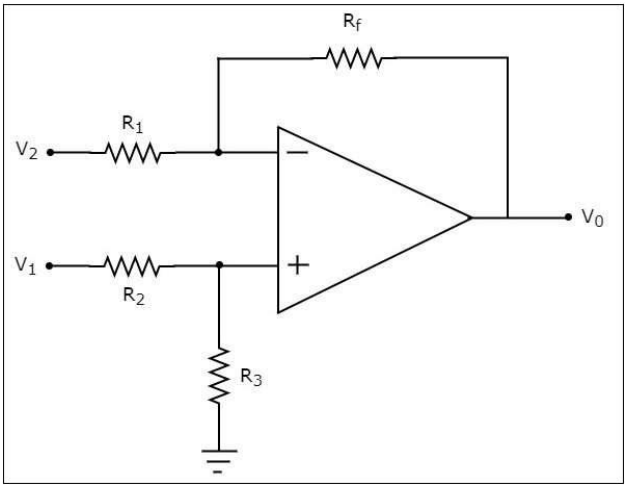
Therefore, the op-amp based adder circuit discussed above will produce the sum of the two input voltages v1v1 and v1v1, as the output, when all the resistors present in the circuit are of same value. Note that the output voltage V0V0 of an adder circuit is having a **negative sign**, which indicates that there exists a 180^0 phase difference between the input and the output.

SUBTRACTOR

A subtractor is an electronic circuit that produces an output, which is equal to the difference of the applied inputs. This section discusses about the op-amp based subtractor circuit.

An op-amp based subtractor produces an output equal to the difference of the input voltages applied at its inverting and non-inverting terminals. It is also called as a **difference amplifier**, since the output is an amplified one.

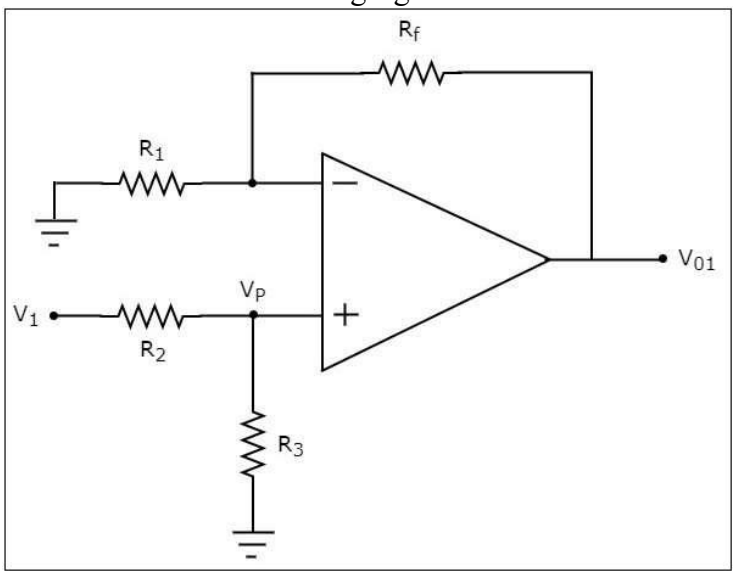
The **circuit diagram** of an op-amp based subtractor is shown in the following figure −



Now, let us find the expression for output voltage V0V0 of the above circuit using **superposition theorem** using the following steps −

Step 1

Firstly, let us calculate the output voltage V01V01 by considering only V1V1.
For this, eliminate V2V2 by making it short circuit. Then we obtain the **modified circuit diagram** as shown in the following figure −



Now, using the **voltage division principle**, calculate the voltage at the non-inverting input terminal of the op-amp.

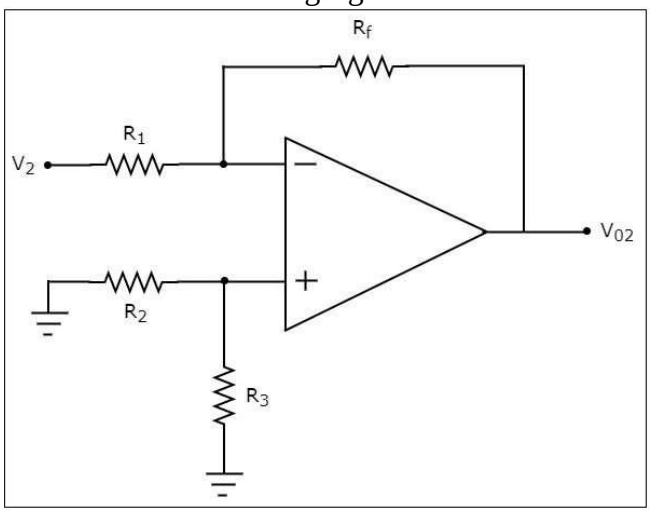
=>Vp=V1(R3R2+R3)=>Vp=V1(R3R2+R3)

Now, the above circuit looks like a non-inverting amplifier having input voltage VpVp. Therefore, the output voltage V01V01 of above circuit will be
V01=Vp(1+RfR1)V01=Vp(1+RfR1)

Substitute, the value of VpVp in above equation, we obtain the output voltage V01V01 by considering only V1V1, as −
V01=V1(R3R2+R3)(1+RfR1)V01=V1(R3R2+R3)(1+RfR1)

Step 2

In this step, let us find the output voltage, V02V02 by considering only V2V2. Similar to that in the above step, eliminate V1V1 by making it short circuit. The **modified circuit diagram** is shown in the following figure.



You can observe that the voltage at the non-inverting input terminal of the op-amp will be zero volts. It means, the above circuit is simply an **inverting op-amp**. Therefore, the output voltage V02V02 of above circuit will be −

V02=(−RfR1)V2V02=(−RfR1)V2

Step 3

In this step, we will obtain the output voltage V0V0 of the subtractor circuit by **adding the output voltages** obtained in Step1 and Step2. Mathematically, it can be written as

V0=V01+V02V0=V01+V02

Substituting the values of V01V01 and V02V02 in the above equation, we get −

V0=V1(R3R2+R3)(1+RfR1)+(−RfR1)V2V0=V1(R3R2+R3)(1+RfR1)+(−RfR1)V2

=>V0=V1(R3R2+R3)(1+RfR1)−(RfR1)V2=>V0=V1(R3R2+R3)(1+RfR1)−(RfR1)V2

If Rf=R1=R2=R3=RRf=R1=R2=R3=R, then the output voltage V0V0 will be

V0=V1(RR+R)(1+RR)−(RR)V2V0=V1(RR+R)(1+RR)−(RR)V2

=>V0=V1(R2R)(2)−(1)V2=>V0=V1(R2R)(2)−(1)V2

V0=V1−V2V0=V1−V2

Thus, the op-amp based subtractor circuit discussed above will produce an output, which is the difference of two input voltages V1V1 and V2V2, when all the resistors present in the circuit are of same value.

Differentiator And Integrator

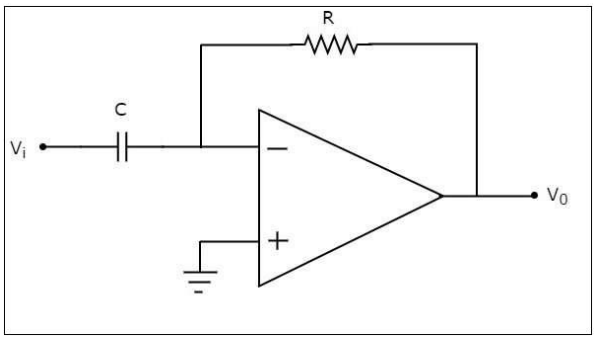
The electronic circuits which perform the mathematical operations such as differentiation and integration are called as differentiator and integrator, respectively.

This chapter discusses in detail about op-amp based **differentiator** and integrator. Please note that these also come under linear applications of op-amp.

DIFFERENTIATOR

A **differentiator** is an electronic circuit that produces an output equal to the first derivative of its input. This section discusses about the op-amp based differentiator in detail.

An op-amp based differentiator produces an output, which is equal to the differential of input voltage that is applied to its inverting terminal. The **circuit diagram** of an op-amp based differentiator is shown in the following figure −



In the above circuit, the non-inverting input terminal of the op-amp is connected to ground. That means zero volts is applied to its non-inverting input terminal.

According to the **virtual short concept**, the voltage at the inverting input terminal of opamp will be equal to the voltage present at its non-inverting input terminal. So, the voltage at the inverting input terminal of op-amp will be zero volts.

The nodal equation at the inverting input terminal's node is −

Cd(0−Vi)dt+0−V0R=0Cd(0−Vi)dt+0−V0R=0

=>−CdVidt=V0R=>−CdVidt=V0R

=>V0=−RCdVidt=>V0=−RCdVidt

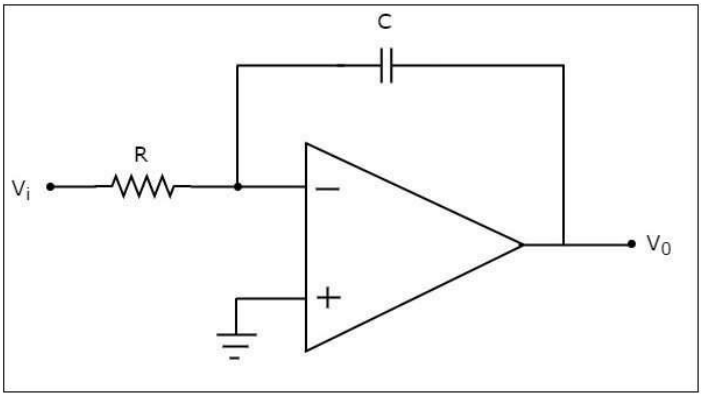
If RC=1secRC=1sec, then the output voltage V0V0 will be −
V0=−dVidtV0=−dVidt

Thus, the op-amp based differentiator circuit shown above will produce an output, which is the differential of input voltage ViVi, when the magnitudes of impedances of resistor and capacitor are reciprocal to each other.
Note that the output voltage V0V0 is having a **negative sign**, which indicates that there exists a 180^0 phase difference between the input and the output.

INTEGRATOR

An **integrator** is an electronic circuit that produces an output that is the integration of the applied input. This section discusses about the op-amp based integrator.

An op-amp based integrator produces an output, which is an integral of the input voltage applied to its inverting terminal. The **circuit diagram** of an op-amp based integrator is shown in the following figure −



In the circuit shown above, the non-inverting input terminal of the op-amp is connected to ground. That means zero volts is applied to its non-inverting input terminal.

According to **virtual short concept**, the voltage at the inverting input terminal of op-amp will be equal to the voltage present at its non-inverting input terminal. So, the voltage at the inverting input terminal of op-amp will be zero volts.

The **nodal equation** at the inverting input terminal is −

$$0-ViR+Cd(0-V0)dt=00-ViR+Cd(0-V0)dt=0$$

$$=>-ViR=CdV0dt=>-ViR=CdV0dt$$

$$=>dV0dt=-ViRC=>dV0dt=-ViRC$$

$$=>dV0=(-ViRC)dt=>dV0=(-ViRC)dt$$

Integrating both sides of the equation shown above, we get −

$$\int dV0=\int(-ViRC)dt\int dV0=\int(-ViRC)dt$$

$$=>V0=-1RC\int Vtdt=>V0=-1RC\int Vtdt$$

If RC=1secRC=1sec, then the output voltage, V0V0 will be −

$$V0=-\int VidtV0=-\int Vidt$$

So, the op-amp based integrator circuit discussed above will produce an output, which is the integral of input voltage ViVi, when the magnitude of impedances of resistor and capacitor are reciprocal to each other.

Note − The output voltage, V0V0 is having a **negative sign**, which indicates that there exists 180^0 phase difference between the input and the output.

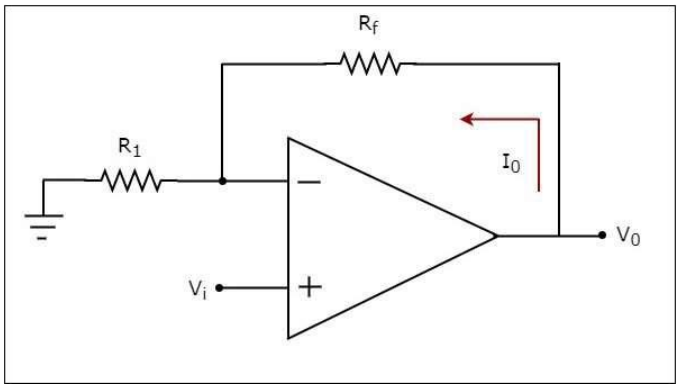
Converters Of Electrical Quantities

Voltage and current are the basic electrical quantities. They can be converted into one another depending on the requirement. **Voltage to Current Converter** and Current to **Voltage Converter** are the two circuits that help in such conversion. These are also linear applications of op-amps. This chapter discusses them in detail.

VOLTAGE TO CURRENT CONVERTER

A **voltage to current converter** or **V to I converter**, is an electronic circuit that takes current as the input and produces voltage as the output. This section discusses about the op-amp based voltage to current converter.

An op-amp based voltage to current converter produces an output current when a voltage is applied to its non-inverting terminal. The **circuit diagram** of an op-amp based voltage to current converter is shown in the following figure.



In the circuit shown above, an input voltage ViVi is applied at the non-inverting input terminal of the op-amp. According to the **virtual short concept**, the voltage at the inverting input terminal of an op-amp will be equal to the voltage at its non-inverting input terminal . So, the voltage at the inverting input terminal of the op-amp will be ViVi.

The **nodal equation** at the inverting input terminal's node is −

ViR1−I0=0ViR1−I0=0

=>I0=VtR1=>I0=VtR1

Thus, the **output current** I0I0 of a voltage to current converter is the ratio of its input voltage ViVi and resistance R1R1.

We can re-write the above equation as −

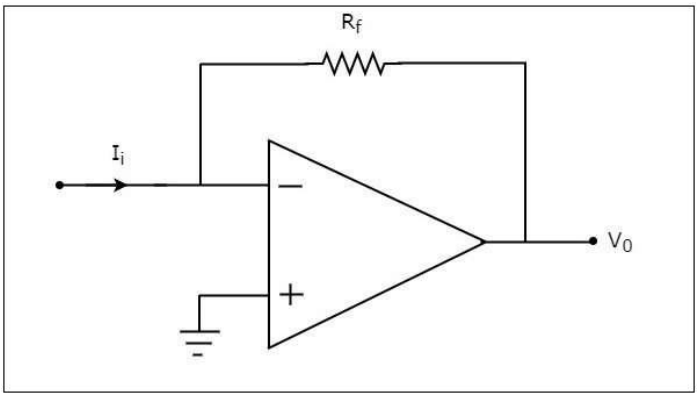
I0Vi=1R1I0Vi=1R1

The above equation represents the ratio of the output current I0I0 and the input voltage ViVi & it is equal to the reciprocal of resistance R1R1 The ratio of the output current I0I0 and the input voltage ViVi is called as **Transconductance**.
We know that the ratio of the output and the input of a circuit is called as gain. So, the gain of an voltage to current converter is the Transconductance and it is equal to the reciprocal of resistance R1R1.

CURRENT TO VOLTAGE CONVERTER

A **current to voltage converter** or **I to V converter** is an electronic circuit that takes current as the input and produces voltage as the output. This section discusses about the op-amp based current to voltage converter.

An op-amp based current to voltage converter produces an output voltage when current is applied to its inverting terminal. The **circuit diagram** of an op-amp based current to voltage converter is shown in the following figure.



In the circuit shown above, the non-inverting input terminal of the op-amp is connected to ground. That means zero volts is applied at its non-inverting input terminal.

According to the **virtual short concept**, the voltage at the inverting input terminal of an op-amp will be equal to the voltage at its non-inverting input terminal. So, the voltage at the inverting input terminal of the op-amp will be zero volts.

The **nodal equation** at the inverting terminal's node is −

−Ii+0−V0Rf=0−Ii+0−V0Rf=0

−Ii=V0Rf−Ii=V0Rf

V0=−RtIiV0=−RtIi

Thus, the **output voltage,** V0V0 of current to voltage converter is the (negative) product of the feedback resistance, RfRf and the input current, ItIt. Observe that the output voltage, V0V0 is having a **negative sign**, which indicates that there exists a 180^0 phase difference between the input current and output voltage.

We can re-write the above equation as −

V0Ii=−RfV0Ii=−Rf

The above equation represents the ratio of the output voltage V0V0 and the input current IiIi, and it is equal to the negative of feedback resistance, RfRf. The ratio of output voltage V0V0 and input current IiIi is called as **Transresistance**.
We know that the ratio of output and input of a circuit is called as **gain**. So, the gain of a current to voltage converter is its trans resistance and it is equal to the (negative) feedback resistance Rf.

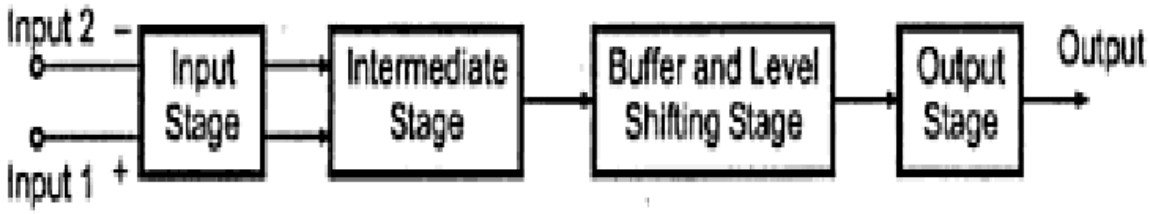
Ideal op-amp

SLEW RATE	∞
CMRR	∞
A_C	0

A_D	∞
BIAS CURRENT	$I_1=I_2=I$
V_1-V_2	0
$\|I_1-I_2\|$	0
V_O	0

Block diagram of op-amp

The block diagram of IC op-amp is as shown in figure



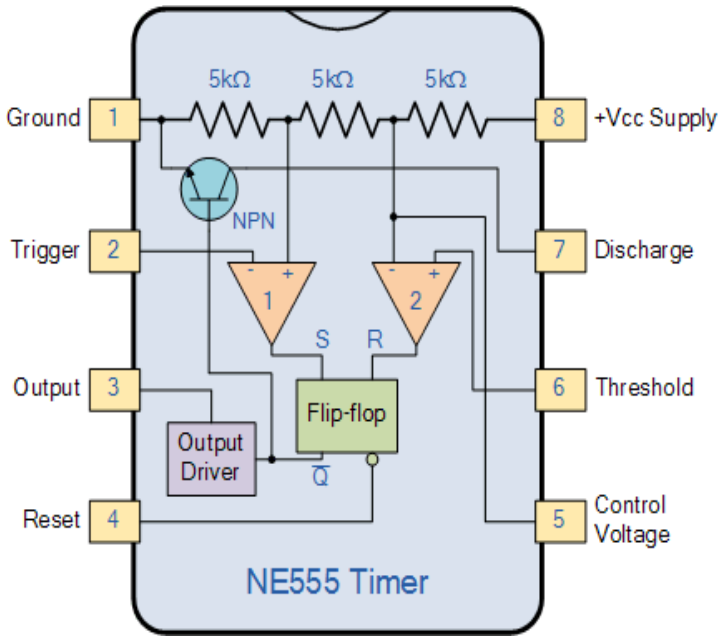
555 TIMER

- The 555 Timer is a commonly used IC designed to produce a variety of output waveforms with the addition of an external RC network
- he basic **555 timer** gets its name from the fact that there are three internally connected 5kΩ resistors which it uses to generate the two comparators reference voltages.
- The 555 timer IC is a very cheap, popular and useful precision timing device which can act as either a simple timer to generate single pulses or long time delays, or as a relaxation oscillator producing a string of stabilised waveforms of varying duty cycles from 50 to 100%.
- The 555 timer chip is extremely robust and stable 8-pin device
- The single 555 Timer chip in its basic form is a Bipolar 8-pin mini Dual-in-line Package (DIP) device consisting of some 25 transistors, 2 diodes and about 16

resistors arranged to form two comparators, a flip-flop and a high current output stage as shown below.

- As well as the 555 Timer there is also available the NE556 Timer Oscillator which combines TWO individual 555's within a single 14-pin DIP package and low power CMOS versions of the single 555 timer such as the 7555 and LMC555 which use MOSFET transistors instead.

- A simplified "block diagram" representing the internal circuitry of the **555 timer** is given below with a brief explanation of each of its connecting pins to help provide a clearer understanding of how it works.



Pin 1. – **Ground**, The ground pin connects the 555 timer to the negative (0v) supply rail.

Pin 2. – **Trigger**, The negative input to comparator No 1. A negative pulse on this pin "sets" the internal Flip-flop when the voltage drops below 1/3Vcc causing the output to switch from a "LOW" to a "HIGH" state.

Pin 3. – **Output**, The output pin can drive any TTL circuit and is capable of sourcing or sinking up to 200mA of current at an output voltage equal to approximately Vcc – 1.5V so small speakers, LEDs or motors can be connected directly to the output.

Pin 4. – **Reset**, This pin is used to "reset" the internal Flip-flop controlling the state of the output, pin 3. This is an active-low input and is generally connected to a logic "1" level when not used to prevent any unwanted resetting of the output.

Pin 5. – **Control Voltage**, This pin controls the timing of the 555 by overriding the 2/3Vcc level of the voltage divider network. By applying a voltage to this pin the width of the output signal can be varied independently of the RC timing network. When not used it is connected to ground via a 10nF capacitor to eliminate any noise.

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The **555 Timers** name comes from the fact that there are three 5kΩ resistors connected together internally producing a voltage divider network between the supply voltage at pin 8 and ground at pin 1.

The voltage across this series resistive network holds the negative inverting input of comparator two at 2/3Vcc and the positive non-inverting input to comparator one at 1/3Vcc.

The most common use of the 555 timer oscillator is as a simple astable oscillator by connecting two resistors and a capacitor across its terminals to generate a fixed pulse train with a time period determined by the time constant of the RC network. But the 555 timer oscillator chip can also be connected in a variety of different ways to produce Monostable or Bistable multivibrators as well as the more common Astable Multivibrator.

Working Principle of 555 Timer

- ✓ The working principle of the 555 timer is by considering the block diagram of the 555 timer IC. The first comparator has threshold input to pin 6 and control inputs for pin 5.
- ✓ The control input is used in some of the applications, but most of the applications the control input is not used hence the control voltage is equal to +2/3 Vcc.
- ✓ The output of the first comparator is given to the flip flop of set pin input. Whenever the threshold voltage overcomes the control voltage then the first comparator is set to flip flop and the output is very high.
- ✓ The high output gives the flip flop saturation which discharges the transistor and capacitor these are connected to pin 7. To the pin 3 the complementary signal is connected and the output of this pin is low.
- ✓ These conditions are applied unless the comparator 2 triggers the flip flop. If any cases occur threshold input is less than the 2/3 Vcc, then the first comparator can't charge the charge flip flop. Hence, the first comparator has the chances of high flip flops output high.
- ✓ If the voltage at the trigger input is less than the 1/3 Vcc then the output of the flip-flop changes to minimum or low. If the second comparator triggers output is minimized to the flip flops.

- ✓ This situation is kept on continuing to the voltage of the trigger input. The output is low for the second comparator with the help of flip flops.

Functions of 555 timer IC

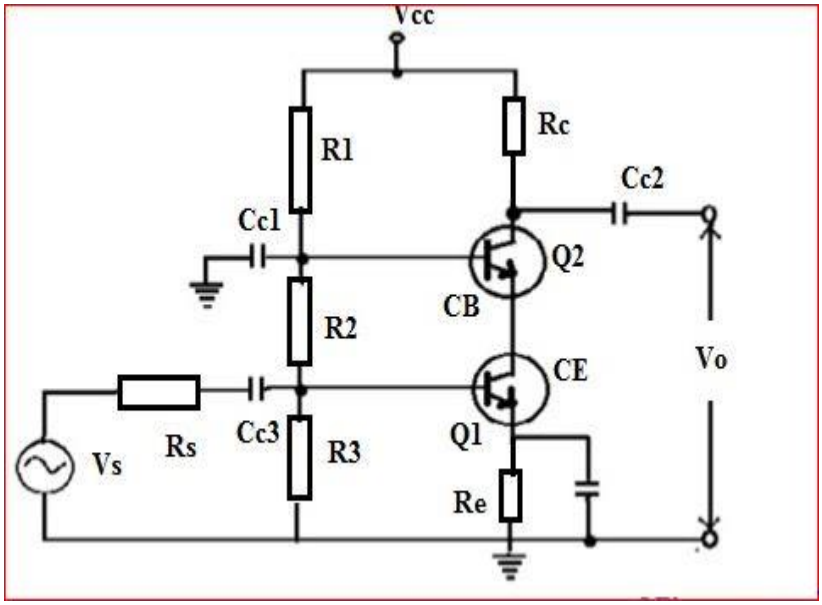
- ➢ The 555 timer power supply has high range from +5volts to +18 volts.
- ➢ The load current for the 555 timer is sourcing 200 mA.
- ➢ The 555 timer has high output current and the output is driven for the TTL.
- ➢ To change in temperature in the 555 timer it has a temperature stability of 50 ppm/ degree.
- ➢ The duty cycle of the 555 timer has the maximum power dissipation.

Cascade amplifier

A cascade amplifier is a two-port network designed with amplifiers which are connected in series when every amplifier transmits its o/p to the second amplifiers input in a daisy chain. The problem in measuring the gain of the cascaded stage is the non-perfect coupling among two stages because of loading. The two stages of cascaded CE (common-emitter) are shown in the following circuit. Here the voltage divider can be formed by using the input and output resistances of the first and next stage. The complete gain cannot be the result of the individual stages.

This amplifier is used to enhance the strength of a signal in a TV receiver. In this amplifier, the primary stage of the amplifier can be connected to the secondary stage of the amplifier. To build a practical electronic system, a single-stage amplifier is not enough.

Even though the amplifier's gain mainly depends on parameters of the device as well as components of the circuit, there exists a higher limit of gain which can be attained from a single-stage amplifier. Therefore, the gain of this amplifier cannot be sufficient in practical application.



The circuit diagram of cascade amplifier is shown below. The circuit can be designed with two configurations of a transistor namely CE (common-emitter) and CB (common base).

The CB (common base) configuration provides a good high-frequency operation.

The current gain, as well as the i/p resistance of the cascade arrangement, is equivalent to the related value of a common emitter single-stage amplifier.

The o/p resistance can be equivalent to the common base configuration. The miller's capacitor shunting the common emitter input stage is extremely small.

Applications

The applications of the cascade amplifier include the following.

- This amplifier is used in tuned RF amplifiers within television circuits.
- This amplifier can also be used as a wideband amplifier.
- The isolation offered among input & output with these amplifiers is extremely high.

Other applications of op-amp

1. Op Amp applications as Inverting Amplifiers
2. Op Amp Applications as Non Inverting Amplifiers
3. Op Amp application as a Phase Shifter
4. Op Amp Applications as Adder or Summing Amplifier
5. Op Amp application as a Differentiator
6. Op Amp Applications as Integrator
7. Op Amp Applications as Voltage to Current Converter

8. Op Amp Applications as Current to Voltage Converter
9. Op Amp Applications as Logarithmic Amplifier
10. Op Amp Applications as Half Wave Rectifier
11. Op Amp Applications as Peak Detector
12. Op Amp Applications as Voltage Comparator

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SCHOOL OF SCIENCE AND HUMANITIES

DEPARTMENT OF PHYSICS

UNIT – IV - Digital and Analog Electronics – SPH1216

UNIT 4 - Number Systems and Boolean Algebra

Decimal, binary, octal, hexadecimal number system and conversion, binary weighted codes, signed numbers, 1s and 2s complement codes, Binary arithmetic, Binary logic functions, Boolean laws, truth tables, associative and distributive properties, De-Morgans theorems, realization of switching functions using logic gates.

Decimal Number System

Decimal number system is a **base 10** number system having 10 digits from 0 to 9. This means that any numerical quantity can be represented using these 10 digits. Decimal number system is also a **positional value system**. This means that the value of digits will depend on its position. Let us take an example to understand this.

Say we have three numbers – 734, 971 and 207. The value of 7 in all three numbers is different−

- In 734, value of 7 is 7 hundreds or 700 or 7×100 or 7×10^2
- In 971, value of 7 is 7 tens or 70 or 7×10 or 7×10^1
- In 207, value 0f 7 is 7 units or 7 or 7×1 or 7×10^0

The weightage of each position can be represented as follows –

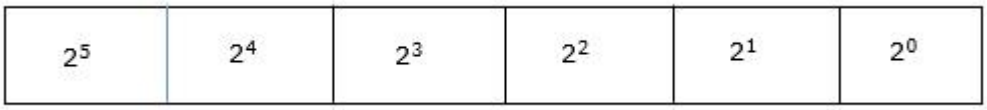
10^5	10^4	10^3	10^2	10^1	10^0

In digital systems, instructions are given through electric signals; variation is done by varying the voltage of the signal. Having 10 different voltages to implement decimal number system in digital equipment is difficult. So, many number systems that are easier to implement digitally have been developed. Let's look at them in detail.

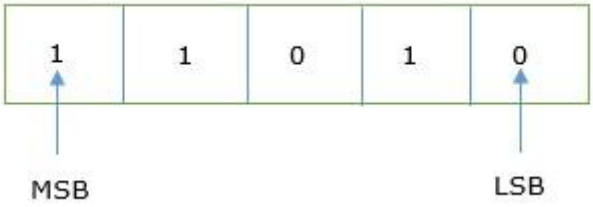
Binary Number System

The easiest way to vary instructions through electric signals is two-state system – on and off. On is represented as 1 and off as 0, though 0 is not actually no signal but signal at a lower voltage. The number system having just these two digits – 0 and 1 – is called **binary number system**.

Each binary digit is also called a **bit**. Binary number system is also positional value system, where each digit has a value expressed in powers of 2, as displayed here.



In any binary number, the rightmost digit is called **least significant bit (LSB)** and leftmost digit is called **most significant bit (MSB)**.



And decimal equivalent of this number is sum of product of each digit with its positional value.

$11010_2 = 1\times2^4 + 1\times2^3 + 0\times2^2 + 1\times2^1 + 0\times2^0$

$= 16 + 8 + 0 + 2 + 0$

$= 26_{10}$

Computer memory is measured in terms of how many bits it can store. Here is a chart for memory capacity conversion.

- 1 byte (B) = 8 bits
- 1 Kilobytes (KB) = 1024 bytes
- 1 Megabyte (MB) = 1024 KB
- 1 Gigabyte (GB) = 1024 MB
- 1 Terabyte (TB) = 1024 GB
- 1 Exabyte (EB) = 1024 PB
- 1 Zettabyte = 1024 EB
- 1 Yottabyte (YB) = 1024 ZB

Octal Number System

Octal number system has eight digits – 0, 1, 2, 3, 4, 5, 6 and 7. Octal number system is also a positional value system with where each digit has its value expressed in powers of 8, as shown here −

Decimal equivalent of any octal number is sum of product of each digit with its positional value.

$726_8 = 7\times8^2 + 2\times8^1 + 6\times8^0$

$= 448 + 16 + 6$

$= 470_{10}$

Hexadecimal Number System

Octal number system has 16 symbols – 0 to 9 and A to F where A is equal to 10, B is equal to 11 and so on till F. Hexadecimal number system is also a positional value system with where each digit has its value expressed in powers of 16, as shown here −

16^5	16^4	16^3	16^2	16^1	16^0

Decimal equivalent of any hexadecimal number is sum of product of each digit with its positional value.

$27FB_{16} = 2\times16^3 + 7\times16^2 + 15\times16^1 + 10\times16^0$

$= 8192 + 1792 + 240 + 10$

$= 10234_{10}$

HEXADECIMAL	DECIMAL	OCTAL	BINARY
0	0	0	0000
1	1	1	0001
2	2	2	0010
3	3	3	0011
4	4	4	0100
5	5	5	0101
6	6	6	0110
7	7	7	0111
8	8	10	1000
9	9	11	1001
A	10	12	1010
B	11	13	1011
C	12	14	1100
D	13	15	1101
E	14	16	1110
F	15	17	1111

Advantages of Hexadecimal System over Octal System:

The advantages are:

i. For a long computer word length the binary representation of hexadecimal number is shorter.
ii. For the word length which is divisible by 4 and not by 3, the hexadecimal system is a convenient one. The octal number system needs the extension of zero bits ahead of the most significant bit in this case.

Advantages of Octal Number System over the Decimal System:
The advantages are:
i. Conversion of octal number to decimal number is easier as the octal number contains only digits. During the process of conversion, the letters used in hexadecimal numbers are to be converted into equivalent decimal numbers.
ii. In hexadecimal number system letters are used to represent decimal numbers 10 to 15. The numbers using letters resemble with words and consequently the use of letters in hexadecimal numbers make confusion. In octal system no such confusion arises as the octal number system uses digits 1 to 7 only.

Decimal to Binary Conversion

It is obtained by using the technique of successive multiplication by 2. In this technique the integer part is noted down after each multiplication and the new fraction obtained is used for further multiplication.

Example:

Convert 50.7 (decimal) to its binary equivalent.

For this decimal real number its binary equivalent is obtained separately for the integer and the fraction.

We first convert the decimal number 50 to binary number in the following way:

	Binary number	*Remainder*	
2	50		
2	25	0	(LSB)
2	12	1	
2	6	0	
2	3	0	
2	1	1	
	0	1	(MSB)

∴ 50 (decimal) = 110010 (binary).
Next we convert 0.7 (decimal) to its binary fraction in the following way :

Fraction	Fraction × 2	Remainder fraction	Integer	
0.7	1.4	0.4	1	(MSB)
0.4	0.8	0.8	0	
0.8	1.6	0.6	1	
0.6	1.2	0.2	1	
0.2	0.4	0.4	0	
0.4	0.8	0.8	0	
0.8	1.6	0.6	1	(LSB)
–	–	–	–	
–	–	–	–	
–	–	–	–	

We find that the fraction has not become zero and the process will continue. So, we have taken an approximation in this case. We have taken here 7 binary bits after the binary point.

The result is-

0.7 (decimal) = 0.1011001 (binary), combining the above two steps, we have-

50.7 (decimal) = 110010.1011001 (binary).

Decimal to Octal Conversion

Example 1

Convert 120 (decimal) to its equivalent octal number.

Octal number		*Remainder*
8	120	
8	15	0
8	1	7
	0	1

∴ the octal equivalent of 120 is 170.

Example 2

Convert 460 (decimal) to its equivalent octal number.

Octal number		*Remainder*
8	460	
8	57	4
8	7	1
	0	7

∴ the octal number = 714.

Decimal to Hexadecimal Conversion:

Decimal to HD conversion is done in the same as the double-dabble method. Here the technique is called Hexa-dabble method. This method is more suitable for fractional number because we need not to know negative powers of 16 to perform the conversion. This

conversion performs in 2 ways. They are conversion of whole number and conversion of fractional number.

Ex: Convert $(379.54)_{10}$ to HD system.

Step-1: Conversion of whole number (379):

1. Divide the whole part of the decimal number repeatedly by 16.
2. Each time, if there is no remainder, write down 0. If there is a remainder, write down a remainder.
3. Write the HD equivalent of each reminder.
4. Write remainders in reverse order to form octal number (bottom to top).

Division	Quotient	Reminder
175÷16	10	15 = F (LSD)
10÷16	0	10 = A (MSD)
So $(175)_{10} = (AF)_{16}$		

Step-2: Conversion of fractional number (0.23):

1. Multiply the fractional part of the decimal number repeatedly by 16
2. Record each time a carry in the integer position.
3. Continue the process till the fractional part is zero or enough digits have been obtained.
4. Write carry's in direct order to form octal number (top to bottom).

Multiply	Value	Fract value	Carry
0.23x16	3.68	0.68	3 (MSD)
0.68x16	10.88	0.88	10 = A
0.88x16	14.08	0.08	14 = E
0.8x16	1.28	0.28	1
0.28x16	4.48	0.48	4
0.48x16	7.68	0.68	7
0.68x16	10.88	0.88	10 = A (LSD)
So $(0.23)_{10} = (0.3AE147AE147A)_{16}$			

So $(175.23)_{10} = (AF.\ 3AE147AE147A)_{16}$

Binary to Decimal Conversion:

Step: 1. Write the binary number.

2. Write the position weights under each bit.

3. Strike off weights corresponding to 0 in the binary number.

4. Add the remaining weight values.

Ex: Convert $(110.10)_2$ to decimal system.

1	1	0	.	1	0
2^2	2^1	2^0	.	2^{-1}	2^{-2}
4	2	—	.	0.5	—

$= (1x4) + (1x2) + (1x0.5) = 4+2+0.5 = (6.5)_{10}$

So $(110.10)_2 = (6.5)_{10}$

Octal to Decimal Conversion:

Convert the octal number 645 to equivalent decimal number.

$$645 = 6 \times 8^2 + 4 \times 8^1 + 5 \times 8^0$$
$$= 6 \times 64 + 4 \times 8 + 5 \times 1$$
$$= 384 + 32 + 5 = 421$$

$\therefore$ the decimal number = 421.

Convert the octal number 715 to equivalent decimal number.

$$715 = 7 \times 8^2 + 1 \times 8^1 + 5 \times 8^0$$
$$= 7 \times 64 + 1 \times 8 + 5 \times 1$$
$$= 448 + 8 + 5 = 461$$

$\therefore$ the decimal number = 461.

Hexadecimal to Decimal Conversion:

Step: 1. Write the Hexadecimal number.

2. Write the position weights under each digit.

3. Strike off weights corresponding to 0 in the HD number.

4. Add the remaining weight values

Ex: Convert $(470)_{16}$ to decimal system.

4	7	0	.	6	5
16^2	16^1	16^0	.	16^{-1}	16^{-2}
256	16	—	.	0.0625	0.00390625

$= (4x256) + (7x16) + (6x0.0625) + (5x0.00390625)$

$= 1024 + 112 + 0.375 + 0.01953125 = (1136.394531)_{10}$

So $(470)_{16} = (1136.394531)_{10}$

Binary to Octal Conversion:

We know that the base of an octal number is 8. As $8 = 2^3$, so for a conversion of binary number to octal number groups of 3 bits are formed in the binary number from right. After forming the groups each 3-bit binary group is replaced by its octal equivalent.

Convert the binary number 1101110 to the octal number.

$(1101110)_2$ = (1) (101) (110)
= (001) (101) (110)
= (1) (5) (6)
= $(156)_8$
= 156 (octal).

Convert the binary number 101111100 to its octal equivalent.

$(101111100)_2$ = (101) (111) (100)
= (5) (7) (4)
= $(574)_8$
= 574 (octal).

Octal to Binary Conversion:

For the conversion each digit of the given octal number is converted to its 3-bit binary equivalent.

Convert octal number 527 to its binary equivalent.

527 (octal) = (101) (010) (111)
5 2 7
= 101010111 (binary).

Convert the octal number 436 to binary.

$(436)_8$ = (100) (011) (110)
4 3 6
= 100011110 (binary).

Octal to Hexadecimal and vice versa Conversion:

Convert the octal number 27 to its hexadecimal equivalent.

27 (octal) = (010) (111)
2 7
= 010111 (binary)

010111 (binary) = (01) (0111)
= (0001) (0111)
1 7
= 17 (hexadecimal).

Convert 456 (octal) to hexadecimal.

456 (octal) = (100) (101) (110)
4 5 6
= 100101110 (binary)

100101110 (binary) = (1) (0010) (1110)
= (0001) (0010) (1110)
1 2 *E*
= 12*E* (hexadecimal).

Convert 5*A* hexadecimal to octal number.

5*A* (hex) = (0101) (1010)
5 *A*
= 01011010 (binary).

The equivalent binary number is now divided into groups of 3 bits from the right to obtain its octal equivalent.

01011010 (binary) = (01) (011) (010)
= (001) (011) (010)
1 3 2
= 132 (octal).

Example 4

Convert 4*DF* hexadecimal to octal number.

4*DF* (hex) = (0100) (1101) (1111)
4 *D* *F*
= 010011011111 (binary).

The equivalent binary number is now divided into groups of 3 bits from the right to get its octal equivalent.

010011011111 (binary) = (010) (011) (011) (111)
2 3 3 7
= 2337 (octal).

UNSIGNED & SIGNED BINARY NUMBERS:

If all data is either positive or negative, then we can forget about positive and negative signs and concentrate on the magnitude (absolute value) of numbers. A separate bit is not allocated for representing the sign of the number. Such binary numbers which do not carry a sign bit with them are called **unsigned binary numbers**. Binary numbers that carry identifications as to their sign are called **signed binary numbers**.

They are classified into 3 major signed binary notations. They are,

1. Sign-Magnitude notation
2. 1's Complement notation
3. 2's Complement notation

Sign-Magnitude notation:

To include the positive or negative sign in the binary, we have to prefix the sign to binary number. The positive and negative signs have to be represented bit 0 and1. The most significant position of a binary number is called **sign-bit** and indicates whether the number represented by the remaining bit is positive or negative. Numbers containing a sign-magnitude notation is easy to read but not easy to use when adding and subtracting binary numbers. They are used in analog-digital conversions.

Conversion: Decimal to Sign-Magnitude Binary:

Step 1: Write the magnitude of the decimal number (without sign).
Step 2: Write the binary equivalent of each decimal digit.
Step 3: Write the binary number.
Step 4: Write the sign bit in the left end of the binary number.

Example: Convert $(- 23. 4)_{10}$ to sign-magnitude system.

		2	3 .	4
		0010	0011	. 0100
Binary No	:	(0010	0011	. 0100)$_2$
Sign bit	:	1		
Sign-Mag. Binary No	:	(1 0010	0011	. 0100)$_2$

1's Complement notation:

The 1's Complement of a binary number is the number that results when we complement each bit. It is calculated by subtracting each bit from 1. It is found that, 1's Complement of a binary number is formed by simply changing every 0 to 1 and every 1 to 0. It means that, we need not carry out subtraction operations. Changing a bit to its opposite is called Complementing the bit.

Conversion: Binary to 1's Complement Binary:

Step 1: Write the binary number.
Step 2: Subtract each binary bit from 1.

Example : Convert $(1010)_2$ to 1's Complement of a binary number
Binary No : 1 0 1 0
1's Comp : 0 1 0 1
So $(1010)_2$ = $(0\ 1\ 0\ 1)_2$ ▶ 1's Complement

Binary Addition:
Rules for Binary Addition:

0 + 0 = 0
0 + 1 = 1
1 + 0 = 1
1 + 1 = 10

Example: Add X = $(1011.01)_2$ and Y = $(1101.11)_2$

Carry :	**1 1 1 1 1**	**1**
X :	1 0 1 1 . 0 1	+
Y :	1 1 0 1 . 1 1	
Answer :	1 1 0 0 1 . 0 0	

Binary Subtraction:
Rules for Binary Subtraction:

0 - 0 = 0
1 + 0 = 1
1 + 1 = 0
10- 1 = 1

Example: Subtract Y = $(1101.11)_2$ from X = $(11011.01)_2$

Borrow	:	0 0 - 0 0 . - -
X :	1 1 0 1 1 . 0 1	(-)

Y : 1 1 0 1 . 1 1
Answer : 0 1 1 0 1 . 1 0

Binary Subtraction with addition using 1's Complement:

The advantage of 1's complement number is that subtraction is never required.

Step 1: Write the binary number of the decimal number (first number).
Step 2: Write the 1's complement of the number to be subtracted.
Step 3: Add it to the number from which the subtraction is to be made.
Step 4: When there is a carry in the last position (MSB) of the result in step (3), remove this
carry and add it to the remaining number.
Step 5: If carry is not obtained in the last position (MSB) of the result in step (3), then the result is a negative number and it is in its 1's complement form. So to express the final answer, 1's complement of the result with a minus sign is to be written.
Step 6 : Write the decimal equivalent of the result.

Example : 14 - 7 = 14 + (-7)
1's Comp of Substract
Binary of 7 = 0 1 1 1
1's Comp of 7 = 1 0 0 0

Binary of 14 = 1 1 1 0 +
1's Comp.of 7 = 1 0 0 0
1 0 1 1 0 (+) (Perform binary addition)
Add carry : 1 (Carry is generated; Add with LSB)
Answer : 0 1 1 1 (Neglect Carry answer; Answer is Positive)

Example: 7 - 14 = 7 + (- 14)
Carry : 1 1 1
Binary No. Of 7 = 0 1 1 1 (+)
1's Comp of 14 = 0 0 0 1
1 0 0 0 (+)
No carry. So answer is negative.
1's Comp of $(1000)_2$ = $(0111)_2$
Decimal No of $(0111)_2$ = 7. So 7-14 = (-7)

2's Complement notation:

The 2's Complement of a binary number is the number that results when we add 1 to the 1's complement binary number. It is a little more difficult to form but it simplifies addition and subtraction. 2's Complement operation is faster than 1's Complement operation since 1'sComplement operation requires the addition of end-around carry.

2's Complement = 1's Complement + 1

Conversion: Decimal to 2's Complement Binary:

Step 1: Write the decimal number
Step 2: Write the binary equivalent of each decimal digit.
Step 3: Write the 1's Complement of a binary number.
Step 4: Add 1 to the 1's complement binary number.

Example:
Convert $(18)_{10}$ to 2's Complement of a binary No.
Binary of 18 = 0001 0011
1's Comp of 18 = 1110 1100 (+)
Add 1 = 1
2's Comp of 18 = 1110 1101

Binary Subtraction with addition using 2's Complement:

Step 1: Write the binary number of the decimal number (first number).
Step 2: Write the 2's complement of the number to be subtracted.
Step 3: .Add it to the number from which the subtraction is to be made.
Step 4: When there is a carry in the last position (MSB) of the result in step (3), remove this
carry and the result is positive.
Step 5: If carry is not obtained in the last position (MSB) of the result in step (3), then the result
is a negative number and it is in its 2's complement form. So to express the final answer, 2's complement of the result with a minus sign is to be written.
Step 6: Write the decimal equivalent of the result.

Example : 14 -7 = 14 + (-7)
Carry 1
Binary of 14 = 1 1 1 0
2's Comp.of 7 = 1 0 0 1 (Perform binary addition)
1 0 1 1 1
So remove this carry and the result is positive.
Decimal of $(0111)_2$ = 7. So 1 -7 = 7

Example : 7-14 = 7 + (-14)
Carry : 1 1
Binary of $(7)_2$ = 0 1 1 1 (+)
2's Comp of 14 = 0 0 1 0
1 0 0 1
No carry. So answer is negative.
2's Comp of $(1001)_2$ = $(0111)_2$
Decimal of $(0111)_2$ = 7. So 7-14 = (-7)

BINARY CODED DECIMAL (BCD) or 8421 CODE OR WEIGHTED CODE:

The BCD code expresses each digit in a decimal number by its nibble equivalent. Some early computers processed BCD numbers. This means that, the decimal numbers were changed into BCD numbers, which the computer then added, subtracted etc. the final result was converted from BCD back to decimal numbers. It is also called **8421 Code or Weighted Code**, since the weights of the digit positions from left to right are 8, 4, 2 and 1 (23, 22, 21, 20). The main advantage of the 8421 code is that, we have to remember the binary numbers from 0 to 9 only.

Decimal	BCD	Decimal	BCD
0	0000	8	1000
1	0001	9	1001
2	0010	10	0001 0000
3	0011	11	0001 0001
4	0100	12	0001 0010
5	0101	13	0001 0011
6	0110	14	0001 0100
7	0111	15	0001 0110

BCD Arithmetic:

A disadvantage of the 8421 code is that, the rules of binary addition and subtraction do not apply to the entire 8421 number but only to the individual 4 bit groups. The BCD addition is, therefore, performed by individually adding the corresponding digits of the decimal numbers expressed in 4 bit binary groups starting from the LSD. If there is a carry out of one group to the next group, or if the result is an illegal code then 6_{10} (0110) is added to the sum term of that group and the resulting carry is added to the next group (This is done to skip the six illegal states). The BCD subtraction is performed by subtracting the digits of each 4-bit group of the subtrahend from the corresponding 4-bit group of the minuend in binary starting from the LSD. If there is a barrow from the next group, then 6_{10} (0110) is subtracted from the difference term of this group (This is done to skip the six illegal states).

Example 1 Perform the following decimal addition in the 8421 code

(a) 25 + 13 (b) 679.6 + 536.8

Solution:

(a)

25		0010	0101	(25 in BCD)
+ 13	⟹	+ 0001	0011	(13 in BCD)
38		0011	1000	(No carry, no illegal code. So, this is the correct sum)

(b)

679.6		0110	0111	1001	. 0110	(679.6 in BCD)
+ 536.8	⟹	+ 0101	0011	0110	. 1000	(536.8 in BCD)
1216.4		1011	1010	1111	. 1110	(All are illegal codes)
		+ 0110	+ 0110	+ 0110	+. 0110	(Add 0110 to each)
		1 0001	1 0000	1 0101	1 . 0100	(Propagate carry)

	+1	+1	+1	+1	
00 01	0010	0001	0110	. 0100	(Corrected sum)
1	2	1	6	. 4	

Example 2 : Perform the following decimal addition in the 8421 code

(a) 38 - 15 (b) 206.7 - 147.8

Solution:

(a)

38	0011	1000	(38 in BCD)
- 15 ⟹	- 0001	0101	(15 in BCD)
23	0010	0011	(No borrow. So this is the correct difference.)

(b)

206.7	0010	0000	0110	.0111	(206.7 in BCD)
- 147.8 ⟹	- 0001	0100	0110	.1000	(147.8 in BCD)
58.9	0000	1011	1110	.1111	(Borrows are present, subtract 0110)
		- 0110	- 0110	-.0110	
		0101	1000	.1001	(Corrected difference)

XS-3 Arithmetic:

The XS-3 code has some very interesting when used in addition and subtraction. To add in XS-3, add the XS-3 number by adding the 4-bit groups in each column starting from LSD. If there is no carry out from the addition of any of the 4-bit groups, subtract 0011 from the sum term of those groups (because when two decimal digits are added in XS-3 and there is no carry, the result is in XS-6). If there is a carry out, add 0011 to the sum term of those groups (because when there is a carry, the invalid states are skipped and the result is in normal binary) To subtract in XS-3, subtract the XS-3 number by subtracting each 4-bit group of the subtrahend from the corresponding 4-bit group of the minuend starting from the LSD. If there is no borrow from the next 4-bit group, add 0011 to the difference term of such groups (Because when the decimal digits are subtracted in XS-3 and there is no borrow, the result in normal binary). If there is a borrow, subtract 0011 from the difference term (because taking a barrow is equivalent to adding six invalid states, so the result is in XS-6).

Example 1 Perform the following decimal addition in XS-3 code

(a) 5 + 3 (b) 37 + 28 (c)247.6 + 359.4

Solution

(a)

5	⇨	1000	(5 in XS-3)
+ 3		+ 0110	(5 in XS-3)
8		1110	(No carry)
		- 0011	(Subtract 0011)
		1011	(Corrected sum in XS-3)

(b)

37	⇨	0110	1010	(37 in XS-3)
+ 28		+ 0101	1011	(28 in XS-3
65		1011 ❶	0101	(Carry generated)
		+1 ⌟		(Propagate carry)
		1100	0101	(Add 0011 to correct 0101)
		- 0011	+ 0011	(Subtract 0011 to correct 1100)
		1001	1000	(Corrected sum in XS-3)

c

247.6	⇨	0101	0111	1010	.1001	(247.6 in XS-3)
+ 359.4		+ 0110	1000	1100	.0111	(359.4 in XS-3)
607.0		1011	1111 ❶	0110 ❶	.0000	(Carry generated)
			+1 ⌟	+1 ⌟		(Propagate carry)
		1011 ❶	0000	0111	.0000	
		+1 ⌟				
		1100	0000	0111	.0000	(Add 0011 to 0000, 0111 and .0000)
		- 0011	+ 0011	+ 0011	+ .0011	(Subtract 0011 from 1100)
		1001	0011	1010	.0011	(Corrected sum in XS-3)

Example 2 Perform the following decimal addition in XS-3 code

(a) 267 - 175 (b) 57.6 - 27.8

Solution

(a)

267	⇨	0101	1001	1010	(267 in XS-3)
- 175		- 0100	1010	1000	(175 in XS-3)
092		0000	1111	0010	(Correct 0010 and 0000 by adding 0011)
		+ 0011	- 0011	+ 0011	(Correct 1111 by subtracting 0011)
		0011	1100	0101	(Corrected difference in XS-3)

(b)

57.6	⇨	1000	1010	.1001	(57.6 in XS-3)
- 27.8		- 0101	1010	.1011	(27.8 in XS-3)
29.8		0010	1111	.1110	(Correct 0010 by adding 0011 and correct .1110 and 1111 by subtracting 0011)
		+ 0011	- 0011	- .0011	
		0101	1110	.1011	(Corrected difference in XS-3)

GRAY CODE OR CYCLIC CODE OR UNWEIGHTED CODE

The gray code is an unweighted code, not suitable for arithmetic operation, but useful for input-output devices, analog to digital converters etc. Each gray code number differs from any adjacent number by a single bit.

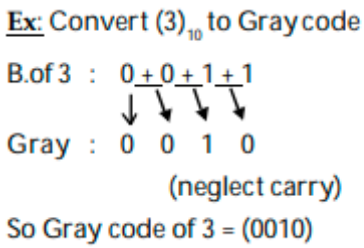
Conversion: Binary to Gray Code

Step: 1. Write the binary number.

2. The MSD in the gray code is same as the MSB in the binary number.

3. Add each pair of adjacent bits from MSB in the binary number and enter the result in the next gray digit.

4. Neglect the carry value in all the places



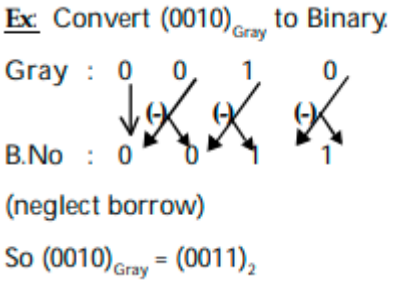
Conversion: Gray to Binary

Step: 1. Write the Gray number.

2. The MSD in the binary number is same as the MSB in the gray code.

3. Subtract the resulted binary bit from the next gray digit and enter the final value in the next binary bit.

4. Neglect the borrow value in all the places.



ASCII CODE OR 7-BIT CODE

ASCII means American Standard code for Information Interchange. To get information into and out of a computer, we need to use some kind of alphanumeric code like numbers, letters, punctuation, mathematical symbols etc. At one time, manufacturers used their own alphanumeric codes, which led to all kinds of confusion. Later, they formed a new input-output code known as ASCII (ask'-ee). This code allows manufacturers to standardize computer hardware such as keyboards, printers and video displays. The ASCII code is a 7-bit code, which includes numerals from 0 to 9, uppercase and lowercase letters of the alphabet and some of the most commonly used symbols. The ASCII code format is X6 X5 X4 X3 X2 X1 X0

Where X = 0 or 1

LIST = 100 1100 100 1001 101 0011 101 0100

list = 110 1100 110 1001 111 0011 111 0100

$X_6 X_5 X_4$ / $X_3 X_2 X_1 X_0$	010	011	100	101	110	111
0000	space	0	@	P		p
0001	!	1	A	Q	a	q
0010	"	2	B	R	b	r
0011	#	3	C	S	c	s
0100	$	4	D	T	d	t
0101	%	5	E	U	e	u
0110	&	6	F	V	f	v
0111	'	7	G	W	g	w
1000	(	8	H	X	h	x
1001	)	9	I	Y	i	y
1010	*	:	J	Z	j	z
1011	+	;	K		k	
1100	,	<	L		l	
1101	-	=	M		m	
1110	.	>	N		n	
1111	/	?	O		o	

Parity Bit:

The ASCII code is used for digital data over telephone lines. 1-bit errors may occur in transmitted data. To catch these errors, a parity bit is usually transmitted along with the original bits. Then a parity checker at the receiving end can test for even or odd parity (0 or 1) whichever parity has been prearranged between the sender and the receiver. Since ASCII code uses 7-bits, the addition of a parity bit to the transmitted data produces an 8-bit number. X7 X6 X5 X4 X3 X2 X1 X0 , where X7 is parity bit. This is an ideal length because most digital equipment is set up to handle bytes of data.

Ex: A computer sends a message to another computer using odd parity bit. Here is the message in ASCII code, plus the parity bit.

1100 1000

0100 0101

0100 1100

0100 1100

0100 1111

What do these numbers mean?

Ans: It is clear that, first 8-bit number has odd parity and no 1-bit errors occurred during transmission. Using the ASCII character table, the message is HELLO.

Basic Logic Gates

A logic gate is a basic building block of a digital circuit that has two inputs and one output. The relationship between the i/p and the o/p is based on a certain logic. These gates are implemented using electronic switches like transistors, diodes. But, in practice, basic logic gates are built using CMOS technology, FETS, and MOSFET(Metal Oxide Semiconductor FET)s. Logic gates are used in microprocessors, microcontrollers, embedded system applications, and in electronic and electrical project circuits. The basic logic gates are categorized into seven: AND, OR, XOR, NAND, NOR, XNOR, and NOT. These logic gates with their logic gate symbols and truth tables are explained below.

Basic Logic Gates Operation

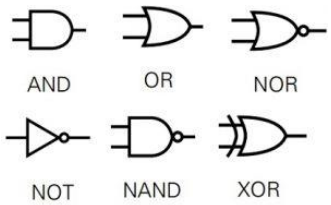
Use of Basic Logic Gates

The basic logic gates are used to perform fundamental logical functions. These are the basic building blocks in the digital ICs (integrated circuits). Most of the logic gates use two binary inputs and generates a single output like 1 or 0. In some electronic circuits, few logic gates are used whereas in some other circuits, microprocessors include millions of logic gates.

The implementation of Logic gates can be done through diodes, transistors, relays, molecules, and optics otherwise different mechanical elements. Because of this reason, basic logic gates are used like electronic circuits.

Types of Logic Gates

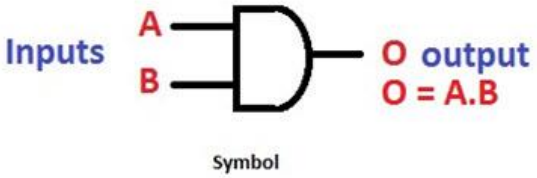
The different types of logic gates and symbols with truth tables are discussed below.



Basic Logic Gates

AND Gate

The AND gate is a digital logic gate with ‘n’ i/ps one o/p, which performs logical conjunction based on the combinations of its inputs. The output of this gate is true only when all the inputs are true. When one or more inputs of the AND gate’s i/ps are false, then only the output of the AND gate is false. The symbol and truth table of an AND gate with two inputs is shown below.



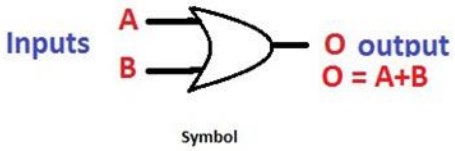
Inputs		Output
A	B	O
0	0	0
0	1	0
1	0	0
1	1	1

Truth table

AND Gate and its Truth Table

OR Gate

The OR gate is a digital logic gate with 'n' i/ps and one o/p, that performs logical conjunction based on the combinations of its inputs. The output of the OR gate is true only when one or more inputs are true. If all the i/ps of the gate are false, then only the output of the OR gate is false. The symbol and truth table of an OR gate with two inputs is shown below.



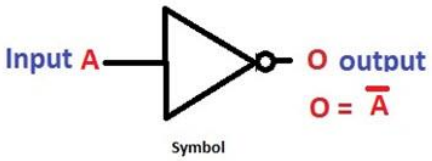
Inputs		Output
A	B	O
0	0	0
0	1	1
1	0	1
1	1	1

Truth table

OR Gate and its Truth Table

NOT Gate

The NOT gate is a digital logic gate with one input and one output that operates an inverter operation of the input. The output of the NOT gate is the reverse of the input. When the input of the NOT gate is true then the output will be false and vice versa. The symbol and truth table of a NOT gate with one input is shown below. By using this gate, we can implement NOR and NAND gates



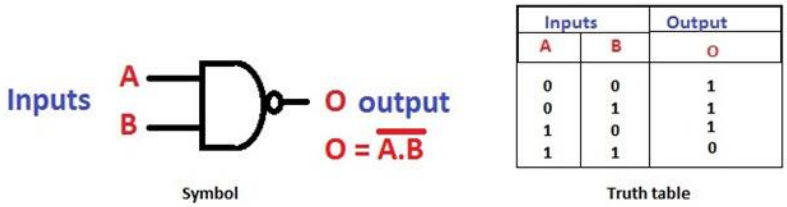
Inputs	Output
A	O
0	1
1	0

Truth table

NOT Gate and Its Truth Table

NAND Gate

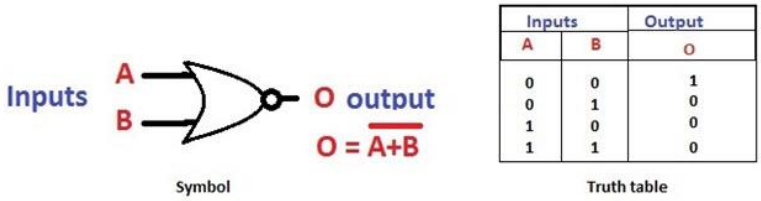
The NAND gate is a digital logic gate with 'n' i/ps and one o/p, that performs the operation of the AND gate followed by the operation of the NOT gate.NAND gate is designed by combining the AND and NOT gates. If the input of the NAND gate high, then the output of the gate will be low.The symbol and truth table of the NAND gate with two inputs is shown below.



NAND Gate and its Truth Table

NOR Gate

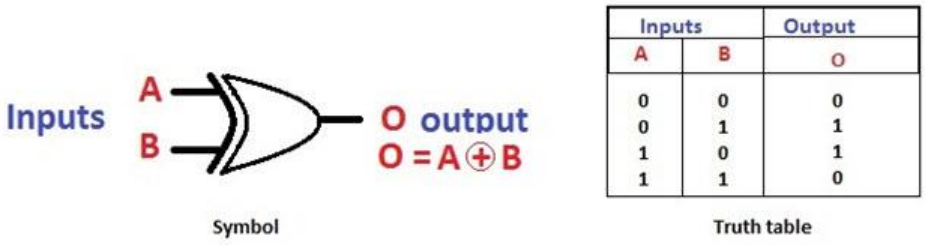
The NOR gate is a digital logic gate with n inputs and one output, that performs the operation of the OR gate followed by the NOT gate. NOR gate is designed by combining the OR and NOT gate. When any one of the i/ps of the NOR gate is true, then the output of the NOR gate will be false. The symbol and truth table of the NOR gate with the truth table is shown below.



NOR Gate and Its Truth Table

Exclusive-OR Gate

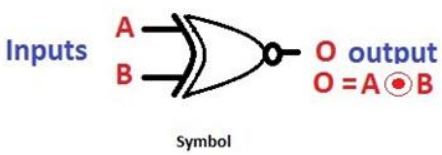
The Exclusive-OR gate is a digital logic gate with two inputs and one output. The short form of this gate is Ex-OR. It performs based on the operation of the OR gate. . If any one of the inputs of this gate is high, then the output of the EX-OR gate will be high. The symbol and truth table of the EX-OR are shown below.



EX-OR gate and Its Truth Table

Exclusive-NOR Gate

The Exclusive-NOR gate is a digital logic gate with two inputs and one output. The short form of this gate is Ex-NOR. It performs based on the operation of the NOR gate. When both the inputs of this gate are high, then the output of the EX-NOR gate will be high. But, if any one of the inputs is high (but not both), then the output will be low. The symbol and truth table of the EX-NOR are shown below.



Inputs		Output
A	B	O
0	0	1
0	1	0
1	0	0
1	1	1

Truth table

EX-NOR Gate and Its Truth Table

The applications of logic gates are mainly determined based upon their truth table, i.e., their mode of operations. The basic logic gates are used in many circuits like a push-button lock, light-activated burglar alarm, safety thermostat, an automatic watering system, etc.

Laws of Boolean Algebra

Boolean Algebra is used to analyze and simplify the digital (logic) circuits. It uses only the binary numbers i.e. 0 and 1. It is also called as **Binary Algebra** or **logical Algebra**. Boolean algebra was invented by **George Boole** in 1854.

Rule in Boolean Algebra

Following are the important rules used in Boolean algebra.

- Variable used can have only two values. Binary 1 for HIGH and Binary 0 for LOW.
- Complement of a variable is represented by an overbar (-). Thus, complement of variable B is represented as $\overline{B}$. Thus if B = 0 then $\overline{B}$ = 1 and B = 1 then $\overline{B}$ = 0.
- ORing of the variables is represented by a plus (+) sign between them. For example ORing of A, B, C is represented as A + B + C.
- Logical ANDing of the two or more variable is represented by writing a dot between them such as A.B.C. Sometime the dot may be omitted like ABC.

Boolean Laws

There are six types of Boolean Laws.

Commutative law

Any binary operation which satisfies the following expression is referred to as commutative operation.

$$\text{(i) } A.B = B.A \qquad \text{(ii) } A + B = B + A$$

Commutative law states that changing the sequence of the variables does not have any effect on the output of a logic circuit.

Associative law

This law states that the order in which the logic operations are performed is irrelevant as their effect is the same.

$$(i)\ (A.B).C = A.(B.C) \qquad (ii)\ (A + B) + C = A + (B + C)$$

Distributive law

Distributive law states the following condition.

$$A.(B + C) = A.B + A.C$$

AND law

These laws use the AND operation. Therefore they are called as **AND** laws.

$$(i)\ A.0 = 0 \qquad (ii)\ A.1 = A$$
$$(iii)\ A.A = A \qquad (iv)\ A.\overline{A} = 0$$

OR law

These laws use the OR operation. Therefore they are called as **OR** laws.

$$(i)\ A + 0 = A \qquad (ii)\ A + 1 = 1$$
$$(iii)\ A + A = A \qquad (iv)\ A + \overline{A} = 1$$

INVERSION law

This law uses the NOT operation. The inversion law states that double inversion of a variable results in the original variable itself.

$$\overline{\overline{A}} = A$$

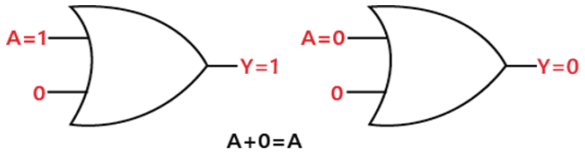
Rules of Boolean algebra

There are the following rules of Boolean algebra, which are mostly used in manipulating and simplifying Boolean expressions. These rules plays an important role in simplifying boolean expressions.

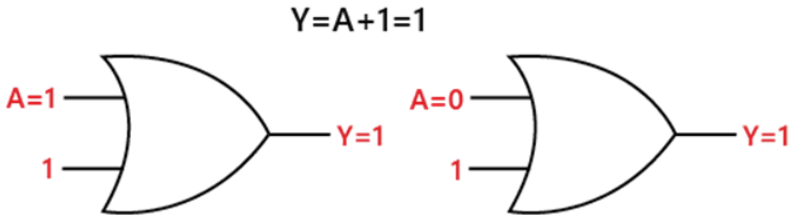
1.	A+0=A	**7.**	A.A=A
2.	A+1=1	**8.**	A.A'=0
3.	A.0=0	**9.**	A''=A
4.	A.1=A	**10.**	A+AB=A

5.	A+A=A	**11.**	A+A'B=A+B
6.	A+A'=1	**12.**	(A+B)(A+C)=A+BC

Rule 1: A + 0 = A

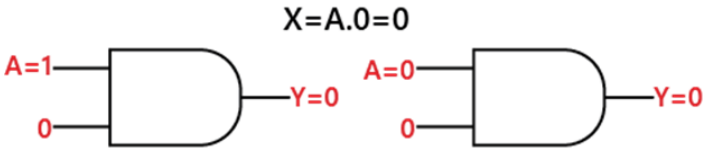


Rule 2: (A + 1) = 1



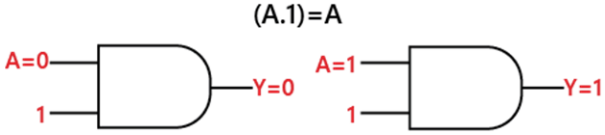
Rule 3: (A.0) = 0

Let's suppose; we have an input variable A whose value is either 0 or 1



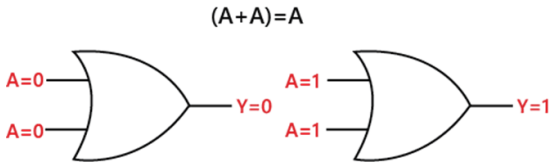
Rule 4: (A.1) = A

Let's suppose; we have an input variable A whose value is either 0 or 1. When we perform the AND operation with 1, the result will always be equal to the input variable. This rule states that an input variable ANDed with 1 is equal to the input variable always. Diagrammatically, this rule can be defined as:



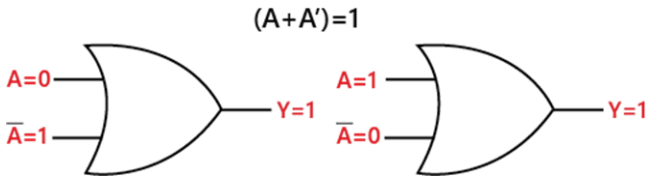
Rule 5: (A + A) = A

Let's suppose; we have an input variable A whose value is either 0 or 1.



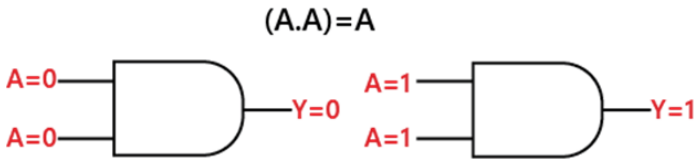
Rule 6: (A + A') = 1

Let's suppose; we have an input variable A whose value is either 0 or 1.



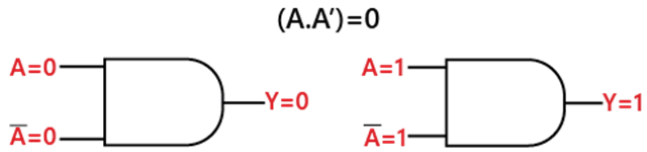
Rule 7: (A.A) = A

Let's suppose; we have an input variable A whose value is either 0 or 1



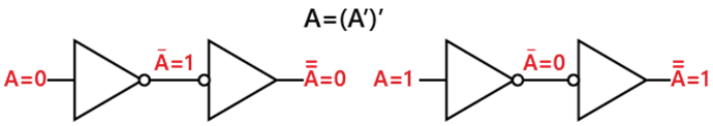
Rule 8: (A.A') = 0

Let's suppose; we have an input variable A whose value is either 0 or 1.



Rule 9: A = (A')'

This rule states that if we perform the double complement of the variable, the result will be the same as the original variable.



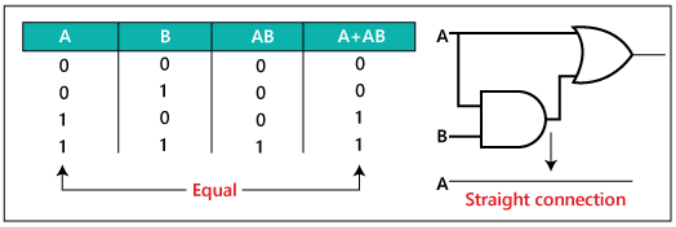
Rule 10: (A + AB) = A

We can prove this rule by using the rule 2, rule 4, and the distributive law as:

A + AB = A(1 + B) Factoring (distributive law)

A + AB = A.1 Rule 2: (1 + B)= 1

A + AB = A Rule 4: A .1 = A



Rule 11: A + AB = A + B

We can prove this rule by using the above rules as:

A + AB = (A + AB)+ AB Rule 10: A = A + AB

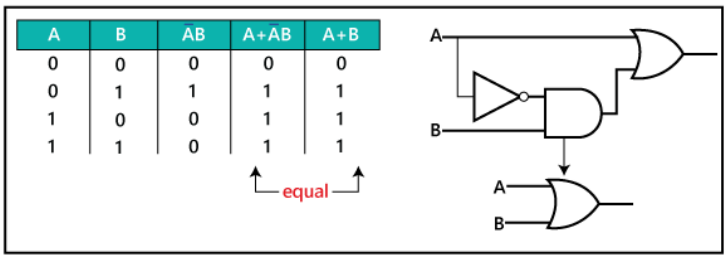
A+AB= (AA + AB)+ AB Rule 7: A = AA

A+AB=AA +AB +AA +AB Rule 8: adding AA = 0

A+AB= (A + A)(A + B) Factoring

A+AB= 1.(A + B) Rule 6: A + A = 1

A+AB=A + B Rule 4: drop the 1



Rule 12: (A + B)(A + C) = A + BC

We can prove this rule by using the above rules as:

(A + B)(A + C)= AA + AC + AB + BC Distributive law

(A + B)(A + C)= A + AC + AB + BC Rule 7: AA = A

(A + B)(A + C)= A(1 + C)+ AB + BC Rule 2: 1 + C = 1

(A + B)(A + C)= A.1 + AB + BC Factoring (distributive law)

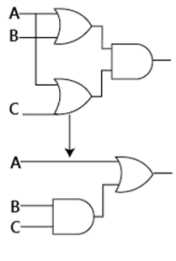
(A + B)(A + C)= A(1 + B)+ BC Rule 2: 1 + B = 1

(A + B)(A + C)= A.1 + BC Rule 4: A .1 = A

(A + B)(A + C)= A + BC

A	B	C	A+B	A+C	(A+B)(A+C)	BC	A+BC
0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0
0	1	0	1	1	0	0	0
0	1	1	1	1	1	1	1
1	0	0	1	1	1	0	1
1	0	1	1	1	1	0	1
1	1	0	1	1	1	0	1
1	1	1	1	1	1	1	1

equal



Example: Simplify the following expression

$$F = BC + B\bar{C} + BA$$

- Simplification

$$F = B(C + \bar{C}) + BA$$

$$F = B \cdot 1 + BA$$

$$F = B(1 + A)$$

$$F = B$$

Example: Simplify the following expression

$$F = A + \bar{A}B + \bar{A}\bar{B}C + \bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}\bar{C}\bar{D}E$$

- Simplification

$$F = A + \bar{A}(B + \bar{B}C + \bar{B}\bar{C}D + \bar{B}\bar{C}\bar{D}E)$$

$$F = A + B + \bar{B}C + \bar{B}\bar{C}D + \bar{B}\bar{C}\bar{D}E$$

$$F = A + B + \bar{B}(C + \bar{C}D + \bar{C}\bar{D}E)$$

$$F = A + B + C + \bar{C}D + \bar{C}\bar{D}E$$

$$F = A + B + C + \bar{C}(D + \bar{D}E)$$

$$F = A + B + C + D + \bar{D}E$$

$$F = A + B + C + D + E$$

$$F = A + \bar{A}B + \bar{A}\bar{B}C + \bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}\bar{C}\bar{D}E$$

Example: Show that the following equality holds

$$\overline{A(\bar{B}\bar{C} + BC)} = \bar{A} + (B + C)(\bar{B} + \bar{C})$$

- Simplification

$$\overline{A(\bar{B}\bar{C} + BC)} = \bar{A} + \overline{(\bar{B}\bar{C} + BC)}$$

$$= \bar{A} + (\overline{\bar{B}\bar{C}})(\overline{BC})$$

$$= \bar{A} + (B + C)(\bar{B} + \bar{C})$$

The minimized form of the logical expression $(\bar{A}\,\bar{B}\,\bar{C} + \bar{A}\,B\,\bar{C} + \bar{A}BC + AB\,\bar{C})$ is

$\bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}BC + \bar{A}B\bar{C}$

Combining first two terms

$\bar{A}\bar{C}(\bar{B} + B) + \bar{A}BC + AB\bar{C}$

$= \bar{A}\bar{C} + \bar{A}BC + AB\bar{C}$

$= \bar{A}(\bar{C} + BC) + AB\bar{C}$

$= \bar{A}(\bar{C} + C)(\bar{C} + B) + AB\bar{C}$

$= \bar{A}(\bar{C} + B) + AB\bar{C}$

$= \bar{A}\bar{C} + \bar{A}B + AB\bar{C}$

$= \bar{A}\bar{C} + B(\bar{A} + A\bar{C})$

$= \bar{A}\bar{C} + B(\bar{A} + A)(\bar{A} + \bar{C})$

$= \bar{A}\bar{C} + B(\bar{A} + \bar{C})$

$= \bar{A}\bar{C} + B\bar{C} + \bar{A}B$

The Boolean expression $AC + B\,\bar{C}$ is equivalent to

(a) $\bar{A}\,C + B\,\bar{C} + AC$

(b) $\bar{B}\,C + AC + B\,\bar{C} + \bar{A}\,C\,\bar{B}$

(c) $AC + B\,\bar{C} + \bar{B}\,C + ABC$

(d) $ABC + \bar{A}\,B\,\bar{C} + AB\,\bar{C} + A\,\bar{B}\,C$

Ans. (d)

$AC + B\bar{C}$

$= AC(B + \bar{B}) + B\bar{C}(A + \bar{A})$

$= ABC + A\bar{B}C + AB\bar{C} + \bar{A}B\bar{C}$

$= ABC + \bar{A}B\bar{C} + AB\bar{C} + A\bar{B}C$

If X = 1 in the logic equation

$[X + Z\{\bar{Y} + (\bar{Z} + X\,\bar{Y})\}]\,\{\bar{X} + \bar{Z}(X + Y)\} = 1$ then

(a) $Y = Z$

(b) $Y = \bar{Z}$

(c) $Z = 1$

(d) $Z = 0$

Ans. (d)

Given logic equation is

$[X + Z\{\overline{Y} + (\overline{Z} + X\,\overline{Y})\}]\,\{\overline{X} + \overline{Z}(X + Y)\} = 1$

$X = 1$, so the first term is $\{1 + \cdots\} = 1$

2^{nd} term is $\{0 + \overline{Z}(1 + Y)\} = \overline{Z}$

1. $\overline{Z} = 1$ *or* $Z = 0$

Simplify the Boolean expressions:

1- $A\overline{B} + A(\overline{B + C}) + B(\overline{B + C})$.

2- $[A\overline{B}(C + BD) + \overline{A}\,\overline{B}]C$

3- $\overline{A}BC + A\overline{B}\,\overline{C} + \overline{A}\,\overline{B}\,\overline{C} + A\overline{B}C + ABC$

De Morgan's Theorem

The first theorem De Morgan states

"The complement of a product of variables is equal to the sum of the complements of the variables"

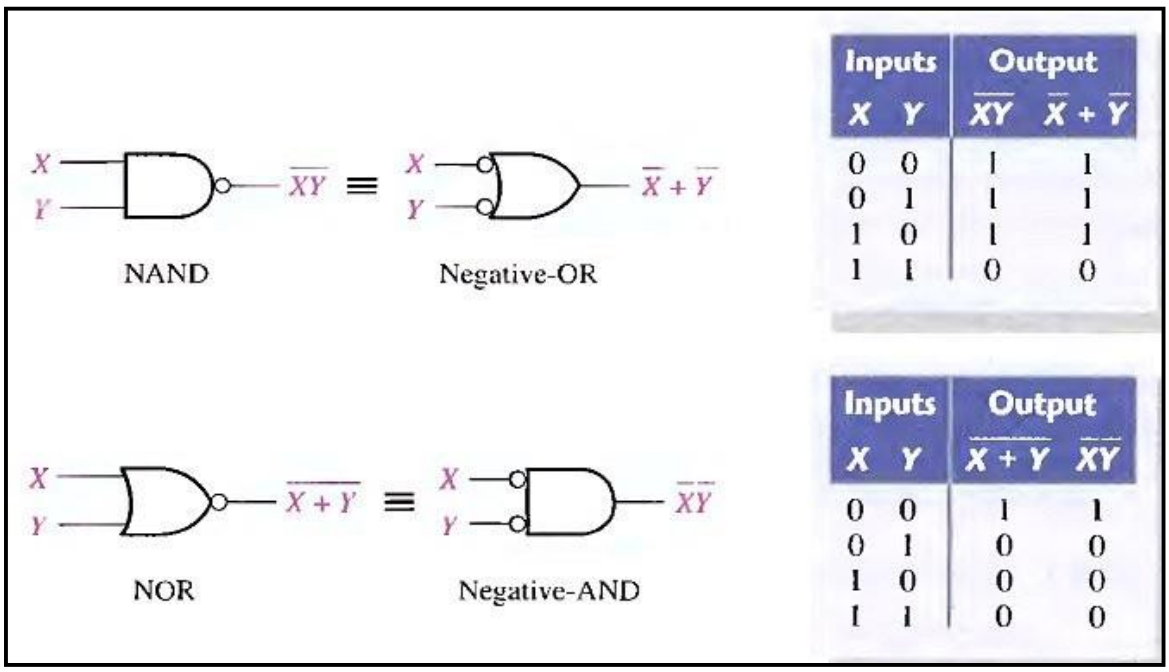
(AB)' = A'+B'

The second theorem of De Morgan states that The complement of two or more ANDed variables is equivalent to the OR of the complements of the individual variables.

(A+B)'= A'. B'

The formula for expressing this theorem for two variables is

$\overline{X + Y} = \overline{X}\,\overline{Y}$



Inputs		Output	
X	Y	$\overline{XY}$	$\overline{X} + \overline{Y}$
0	0	1	1
0	1	1	1
1	0	1	1
1	1	0	0

Inputs		Output	
X	Y	$\overline{X + Y}$	$\overline{X}\,\overline{Y}$
0	0	1	1
0	1	0	0
1	0	0	0
1	1	0	0

Gate equivalencies and the corresponding truth tables

Part – A

1. What do you meant by digital electronics?
2. Describe decimal number system.
3. Define base and weight of a decimal number system.
4. What are called MSD and LSD?
5. Mention the importance of Binary number system.
6. Describe binary number system.
7. Define nibble.
8. What the reason for using octal number system?
9. Describe octal number system.
10. Describe Hexa decimal number system.
11. What are advantages when we use hexadecimal numbers?
12. Write the steps involved to convert binary to decimal numbers.
13. Convert the following binary number into its equivalent decimal number: 111.101
14. Find the decimal equivalent of $(111001101)_2$
15. Convert 15 to its binary equivalent.
16. Convert 0.756 to its binary equivalent.
17. Find the binary equivalent of the following number: $(34.8)_{10}$
18. Convert the octal 276 to decimal number system.
19. Convert the following octal number into decimal number $(420.23)_8$.

20. Convert the decimal number to Octal number: 225
21. Convert the $(0.331)_{10}$ into Octal number.
22. Convert the decimal number $(775.224)_{10}$ into octal umber.
23. Convert $(53)_8$ to binary number.
24. Convert $(0.246)_8$ to binary number.
25. Convert the binary number (11011)2 to octal number.
26. Convert the decimal number to octal number. $(0.01101)_2$
27. Convert the decimal number into octal number. $(11100111.0110)_2$
28. Convert the hexadecimal number to decimal number. $(F7A4)_{16}$
29. What is 1's and 2's complement? What are the advantages?
30. Write a short note about binary coded system.
31. What are the advantages and disadvantages in 8421 code or weighted code?
32. What is excess-3 code or non-weighted code?

PART – B

1. (a)What are 1's and 2's complement? What is the advantage of these numbers?
2. (a)Subtract the following numbers using 1's and 2's complement.

   (i) (11011001)2 to (10001110)2 (ii) (1110111)2 to (1010101)2
3. (a) Explain BCD code with its suitable example.

   (b) Convert the following

   (i) (713)8 into binary (ii) (713)8 into decimal (iii) (713)8 into hexadecimal.
4. Write a short note on Binary number and Hexadecimal number

   (a) Convert the following hexadecimal to binary and verify it (FA9)16, (62.19)16, (6FA.2F)16
5. (a) What are weighted and non weighted codes? Give examples.

   (b) Convert these binary numbers to hexadecimal numbers. (i) 0011 0111 (ii) 1111 0101 0110

   (c) Convert hexadecimal 2F59 to its decimal equivalent.
6. Perform the following decimal addition using 8421 code addition.

   (i) 575.56 + 466.25 ii) 856.12 + 369.35

7. Write a short note on

   a. ASCII and excess-3 code.

   b. Using 1's complement method, Subtract $(0\ 1\ 1\ 0\ 1)_2$ from $(1\ 1\ 0\ 1\ 1)_2$

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SCHOOL OF SCIENCE AND HUMANITIES

DEPARTMENT OF PHYSICS

UNIT – V - Digital and Analog Electronics – SPH1216

UNIT 5 - Analysis & design of Combinational Logic

Switching equations, canonical logic forms, sum of product & product of sums, Karnaugh maps, two, three and four variable Karnaugh maps, Introduction to combinational circuits, code conversions, decoder, encoder, priority encoder, multiplexers as function generators, binary adder, substractor, BCD adder, Binary comparator, arithmetic logic units.

UNIT - 5

STANDARD AND CANONICAL FORMS

STANDARD FORMS OF BOOLEAN EXPRESSIONS

All Boolean expressions, regardless of their form, can be converted into either of two standard forms: the sum-of-products form or the product-of- sums form. Standardization makes the evaluation, simplification, and implementation of Boolean expressions much more systematic and easier.

The Sum-of-Products (SOP) Form

When two or more product terms are summed by Boolean addition,the resulting expression is a sum-of-products (SOP). Some examples are:

AB + ABC

$ABC + \overline{C}DE + \overline{B}\overline{C}\overline{D}$

AB + BCD + AC

Also, an SOP expression can contain a single-variable term, as inA + ABC + $\overline{B}$CD. $\overline{\ }$

In an SOP expression a single overbar cannot extend over more than one variable.

Example

Convert each of the following Boolean expressions to SOP form:

(a) AB + B(CD + EF)

(b) (A + B)(B + C + D)

(c) $\overline{\overline{(A + B)} + C}$

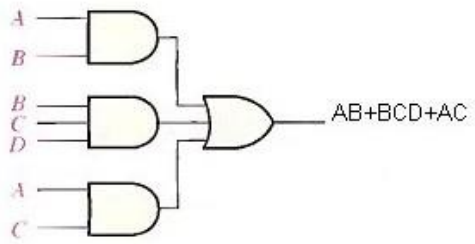


Fig. Implementation of the SOP expression AB + BCD + AC.

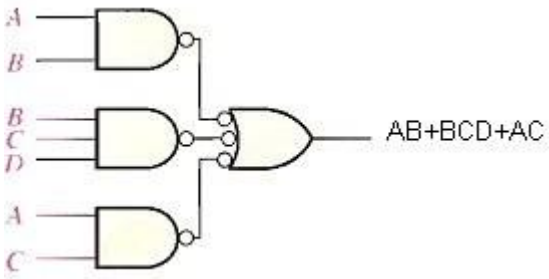


Fig. NAND/NAND implementation is equivalent to the AND/OR.

The Standard SOP Form

So far, you have seen SOP expressions in which some of the product terms do not contain all of the variables in the domain of the expression. For example, the expression $A\bar{B}C + A\bar{B}D + ABC\bar{D}$ has a domain made up of the variables A, B, C. and D. However, notice that the complete set of variables in the domain is not represented in the first two terms of the expression; that is, D or D is missing from the first term and C or C is missing from the second term.

A standard SOP expression is one in which all the variables in the domain appear in each product term in the expression. For example, $\bar{A}BC\bar{D} + AB\bar{C}\bar{D} + A\bar{B}CD$ is a standard SOP expression.

Converting Product Terms to Standard SOP:

Each product term in an SOP expression that does not contain all the variables in the domain can be expanded to standard SOP to include all variables in the domain and their complements. As stated in the following steps, a nonstandard SOP expression is converted into standard form using Boolean algebra rule 6 ($A + \overline{A} = 1$) from Table 4-1: A variable added to its complement equals 1.

Step 1. Multiply each nonstandard product term by a term made up of the sum of a missing variable and its complement. This results in two product terms. As you know, you can multiply anything by 1 without changing its value.

Step 2. Repeat Step 1 until all resulting product terms contain all variables in the domain in either complemented or uncomplemented form. In converting a product term to standard form, the number of product terms is doubled for each missing variable.

Example

Convert the following Boolean expression into standard SOP form:

$A\overline{B}C + A\overline{B} + ABC\overline{D}$

Solution

The domain of this SOP expression A, B, C, D. Take one term at a time. The first term, ABC, is missing variable D or $\overline{D}$, so multiply the first term by $(D + \overline{D})$ as follows:

$A\overline{B}C = A\overline{B}C(D + \overline{D}) = A\overline{B}CD + A\overline{B}C\overline{D}$

In this case, two standard product terms are the result.

The second term, $A\overline{B}$, is missing variables C or $\overline{C}$ and D or $\overline{D}$, so first multiply the second term by $C + \overline{C}$ as follows:

$A\overline{B} = A\overline{B}(C + \overline{C}) = A\overline{B}C + A\overline{B}\overline{C}$

The two resulting terms are missing variable D or $\overline{D}$, so multiply both terms by $(D + \overline{D})$ as follows:

$A\overline{B}C(D + \overline{D}) + A\overline{B}\overline{C}(D + \overline{D})$

$= \overline{A}\,\overline{B}CD + A\overline{B}CD + A\overline{B}\overline{C}D + A\overline{B}\overline{C}\overline{D}$

In this case, four standard product terms are the result.

The third term, $ABC\overline{D}$, is already in standard form. The complete standard SOP form of the original expression is as follows:

$$A\overline{B}C + AB + ABC\overline{D} = ABC\overline{D} + ABCD + \overline{A}BCD + ABCD + \overline{A}BC\overline{D} + ABCD + ABCD$$

The Product-of-Sums (POS) Form

A sum term was defined before as a term consisting of the sum (Boolean addition) of literals (variables or their complements). When two or more sum terms are multiplied, the resulting expression is a product-of-sums (POS). Some examples are

$(A + B)(A + \overline{B} + C)$

$(A + \overline{B} + \overline{C})(C + \overline{D} + E)(B + C + D)$

$(A + B)(A + B + C)(A + C)$

A POS expression can contain a single-variable term, as in

$A(A + B + C)(B + C + D)$.

In a POS expression, a single overbar cannot extend over more than one variable; however, more than one variable in a term can have an overbar. For example, a POS expression can have the term $\overline{A} + \overline{B} + \overline{C}$ but not $\overline{A + B + C}$.

Implementation of a POS Expression simply requires ANDing the outputs oftwo or more OR gates. A sum term is produced by an OR operation and the product of two or more sum terms is produced by an AND operation. Fig.(4-0) shows for the expression (A + B)(B + C + D)(A + C). The output X ofthe AND gate equals the POS expression.

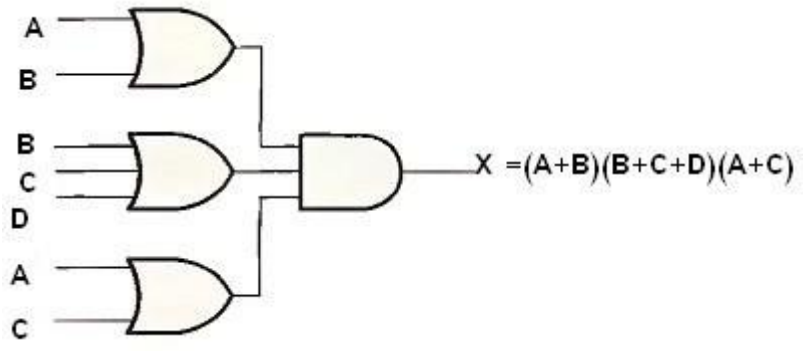


Fig.(4-20)

The Standard POS Form

So far, you have seen POS expressions in which some of the sum terms do not contain all of the variables in the domain of the expression. For example, the expression

$$(A + B + C)\,(A + B + \overline{D})\,(A + \overline{B} + \overline{C} + D)$$

has a domain made up of the variables A, B, C, and D. Notice that the complete set of variables in the domain is not represented in e first two terms of the expression; that is, D or $\overline{D}$ is missing from the first term and C or $\overline{C}$ is missing from the second term.

A standard POS expression is one in which all the variables in the domain appear in each sum term in the expression. For example,

$(\overline{A} + \overline{B} + C + D)(A + \overline{B} + C + D)(A + B + C + D)$

is a standard POS expression. Any nonstandard POS expression (referred to simply as POS) can be converted to the standard form using Boolean algebra.

Converting a Sum Term to Standard POS

Each sum term in a POS expression that does not contain all the variables in the domain can be expanded to standard form to include all variables in the domain and their complements. As stated in the following steps, a nonstandard POS expression is converted into standard form using Boolean algebra rule 8 ($A\,\overline{A} = 0$) from Table 4-1:

Step 1. Add to each nonstandard product term a term made up of the product of the missing variable and its complement. This results in two sum terms. As you know, you can add 0 to anything without changing its value.

Step 2. Apply rule 12 from Table 4-1: $A + BC = (A + B)(A + C)$

Step 3. Repeat Step 1 until all resulting sum terms contain all variables in the domain in either complemented or noncomplemented form.

Example

Convert the following Boolean expression into standard POS form:

$(\overline{A} + B + C)(\overline{B} + C + \overline{D})(A + \overline{B} + \overline{C} + D)$

Solution

The domain of this POS expression is A, B, C, D. Take one term at a time. The first term, A + B + C, is missing variable D or D, so add DD and apply rule 12 as follows:

$A + B + C = A + B + C + DD = (A + B + C + D)(A + B + C + D)$

The second term, $\overline{B} + C + D$, is missing variable A or A, so add AA and apply rule 12 as follows:

$\overline{B} + C + \overline{D} = \overline{B} + C + \overline{D} + A\overline{A} = (A + \overline{B} + C + \overline{D})(\overline{A} + \overline{B} + C + \overline{D})$

The third term, $A + B + C + \overline{D}$, is already in standard form. The standard POS form of the original expression is as follows:

$(\overline{A} + B + C)(\overline{B} + C + \overline{D})(A + \overline{B} + \overline{C} + D) = (\overline{A} + B + C + D)(\overline{A} + B + C + \overline{D})(A + \overline{B} + C + \overline{D})(A + \overline{B} + C + D)(A + B + C + \overline{D})$

Examples:-

1. Identify each of the following expressions as SOP, standard SOP, POS, or standard POS:
   (a) $AB + \overline{A}BD + \overline{A}C\overline{D}$ (b) $(A + \overline{B} + C)(A + B + \overline{C})$
   (c) $\overline{A}BC + AB\overline{C}$ (d) $A(A + \overline{C})(A + B)$
2. Convert each SOP expression in Question 1 to standard form.
3. Convert each POS expression in Question 1 to standard form.

CANONICAL FORMS OF BOOLEAN EXPRESSIONS

With one variable x & $\overline{x}$.

With two variables $\overline{x}\,\overline{y}$, $x\,\overline{y}$, $\overline{x}\,y$ and $x\,y$.

With three variables $\overline{x}\,\overline{y}\,\overline{z}$, $\overline{x}\,\overline{y}\,z$, $\overline{x}\,y\,\overline{z}$, $\overline{x}\,y\,z$, $x\,\overline{y}\,\overline{z}$, $x\,\overline{y}\,z$, $x\,y\,\overline{z}$ & $x\,y\,z$.

These eight AND terms are called minterms.

n variables can be combined to form 2^n minterms.

x	Y	z	minterm	designation	maxterm	designation

0	0	0	$\overline{x}\,\overline{y}\,\overline{z}$	m_0	$x+y+z$	M_0
0	0	1	$\overline{x}\,\overline{y}\,z$	m_1	$x+y+\overline{z}$	M_1
0	1	0	$\overline{x}\,y\,\overline{z}$	m_2	$x+\overline{y}+z$	M_2
0	1	1	$\overline{x}\,y\,z$	m_3	$x+\overline{y}+\overline{z}$	M_3
1	0	0	$x\,\overline{y}\,\overline{z}$	m_4	$\overline{x}+y+z$	M_4
1	0	1	$x\,\overline{y}\,z$	m_5	$\overline{x}+y+\overline{z}$	M_5
1	1	0	$x\,y\,\overline{z}$	m_6	$\overline{x}+\overline{y}+z$	M_6
1	1	1	$x\,y\,z$	m_7	$\overline{x}+\overline{y}+\overline{z}$	M_7
			(AND terms)		(OR terms)	

Note that each maxterm is the complement of its correspondingminterm and vice versa.

For example the function F

x	y	z	F
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

$F = \overline{x}\,\overline{y}\,\overline{z} + \overline{x}\,y\,\overline{z} + x\,\overline{y}\,\overline{z}$

$zF = m_1 + m_4 + m_7$

Any Boolean function can be expressed as a sum of minterms (sum of products **SOP**) or product of maxterms (product of sums **POS**).

$\overline{F} = \overline{x}\,\overline{y}\,\overline{z} + \overline{x}\,y\,\overline{z} + \overline{x}\,y\,z + x\,\overline{y}\,z + x\,y\,\overline{z}$

$\overline{\quad} =$

The complement of $\overline{F} = F = F$

$F = (x + y + z)\ (x + y + z)\ (x + \overline{y} + z)\ (x + y + z)\ (x + y + z)F = M_0\, M_2\, M_3\, M_5\, M_6$

Example

Express the Boolean function $F = A + \overline{B}C$ in a sum of minterms (SOP).

Solution

The term A is missing two variables because the domain of F is (A, B, C)$A = A(B + B) = AB + A\overline{B}$ because $B + \overline{B} = 1$

$\overline{B}C$ missing A, so

$\overline{B}C(A + \overline{A}) = A\overline{B}C + \overline{A}\overline{B}C$

$AB(C + \overline{C}) = ABC + AB\overline{C}$

$AB(C + C) = ABC + ABC$

$F = ABC + ABC + ABC + ABC + \overline{A}BC + ABC$

Because A + A = A

$F = ABC + ABC + ABC + ABC + ABC$

$F = m_7 + m_6 + m_5 + m_4 + m_1$

In short notation

$F(A, B, C) = \Sigma(1, 4, 5, 6, 7)$

$\overline{F}(A, B, C) = \Sigma(0, 2, 3)$

The complement of a function expressed as the sum of minterms equalto the sum of minterms missing from the original function.

Truth table for $F = A + \overline{B}C$

	A	B	C	$\overline{B}$	BC	F
0	0	0	0	1	0	0
1	0	0	1	1	1	1
2	0	1	0	0	0	0
3	0	1	1	0	0	0
4	1	0	0	1	0	1
5	1	0	1	1	1	1
6	1	1	0	0	0	1
7	1	1	1	0	0	1

Example

Express $F = xy + \overline{x}z$ in a product of maxterms form.

Solution

$F = xy + \overline{x}z = (xy + \overline{x})(xy + z) = (x + \overline{x})(y + \overline{x})(x + z)(y + z)$ remember $x + \overline{x} = 1$

$F = (y + \overline{x})(x + z)(y + z)$

$F = (\overline{x} + y + z\overline{z})(x + \overline{y}\overline{y} + z)(\overline{x}\overline{x} + y + z)$

$F = (x + y + z)(x + y + z)(x + y + z)(x + y + z)(x + y + z)(x + y + z)$

$F = (\overline{x} + y + z)(\overline{x} + y + \overline{z})(x + y + z)(x + \overline{y} + z)F = M_4 M_5 M_0 M_2$

$F(x, y, z) = \prod(0, 2, 4, 5)$

$\overline{F}(x, y, z) = \prod(1, 3, 6, 7)$

The complement of a function expressed as the product of maxtermsequal to the product of maxterms missing from the original function.

To convert from one canonical form to another, interchange the symbols Σ, $\prod$ and list those numbers missing from the original form.

$F = M_4 M_5 M_0 M_2 = m_1 + m_3 + m_6 + m_7$

$F(x, y, z) = \prod(0, 2, 4, 5) = \Sigma(1, 3, 6, 7)$

Example

Develop a truth table for the standard SOP expression $\overline{A}\overline{B}C + A\overline{B}\overline{C} + ABC$.

INPUTS A	B	C	OUTPUT X	PRODUCT TERM
0	0	0	0	
0	0	1	1	$\overline{A}\,\overline{B}C$
0	1	0	0	
0	1	1	0	
1	0	0	1	$A\overline{B}\,\overline{C}$
1	0	1	0	
1	1	0	0	
1	1	1	1	ABC

Converting POS Expressions to Truth Table Format

Reca11 that a POS expression is equal to 0 only if at least one of the sum terms is equal to 0. To construct a truth table from a POS expression, list all the possible combinations of binary values of the variables just as wasdone for the SOP expression. Next, convert the POS expression to standard form if it is not already. Finally, place a 0 in the output column (X) for each binary value that makes the expression a 0 and place a 1 for all the remainingbinary values. This procedure is illustrated in Example below:

Example

Determine the truth table for the following standard POS expression:

$$(A + B + C)(A + \overline{B} + C)(A + \overline{B} + \overline{C})(\overline{A} + B + \overline{C})(\overline{A} + \overline{B} + C)$$

Solution

There are three variables in the domain and the eight possible binary values are listed in the left three columns of. The binary values that make the sum terms in the expression equal to 0 are A+ B + C: 000; A + B + C: 010: A + B + C: 011; A + B + C: 101; and A + B + C: 110. For each of these binary

values, place a 0 in the output column as shown in the table. For each of the remaining binary combinations, place a 1 in the output column.

INPUTS			OUTPUT	
A	B	C	X	SUM TERM
0	0	0	0	$(A + B + C)$
0	0	1	1	
0	1	0	0	$(A + \overline{B} + C)$
0	1	1	0	$(A + \overline{B} + \overline{C})$
1	0	0	1	
1	0	1	0	$(\overline{A} + B + \overline{C})$
1	1	0	0	$(\overline{A} + \overline{B} + C)$
1	1	1	1	

KARNAUGH MAP MINIMIZATION

A Karnaugh map provides a systematic method for simplifying Boolean expressions and, if properly used, will produce the simplest SOP or POS expression possible, known as the minimum expression. As you have seen, the effectiveness of algebraic simplification depends on your familiarity with all the laws, rules, and theorems of Boolean algebra and on your ability to apply them. The Karnaugh map, on the other hand, provides a "cookbook" method for simplification.

A Karnaugh map is similar to a truth table because it presents all of the possible values of input variables and the resulting output for each value. Instead of being organized into columns and rows like a truth table, the Karnaugh map is an array of cells in which each cell represents a binary value of the input variables. The cells are arranged in a way so that simplification of

a given expression is simply a matter of properly grouping the cells. Karnaugh maps can be used for expressions with two, three, four. and five variables. Another method, called the Quine-McClusky method can be used for higher numbers of variables.

The number of cells in a Karnaugh map is equal to the total number of possible input variable combinations as is the number of rows in a truth table. For three variables, the number of cells is $2^3 = 8$. For four variables, the number of cells is $2^4 = 16$.

<u>The 3-Variable Karnaugh Map</u>

The 3-variable Karnaugh map is an array of eight cells. as shown in Fig.(5-1)(a). In this case, A, B, and C are used for the variables although other letters could be used. Binary values of A and B are along the left side (notice the sequence) and the values of C are across the top. The value of a givencell is the binary values of A and B at the left in the same row combinedwith the value of C at the top in the same column. For example, the cell in the upper left corner has a binary value of 000 and the cell in the lower right corner has a binary value of 101. Fig.(5-1)(b) shows the standard product terms that are represented by each cell in the Karnaugh map.

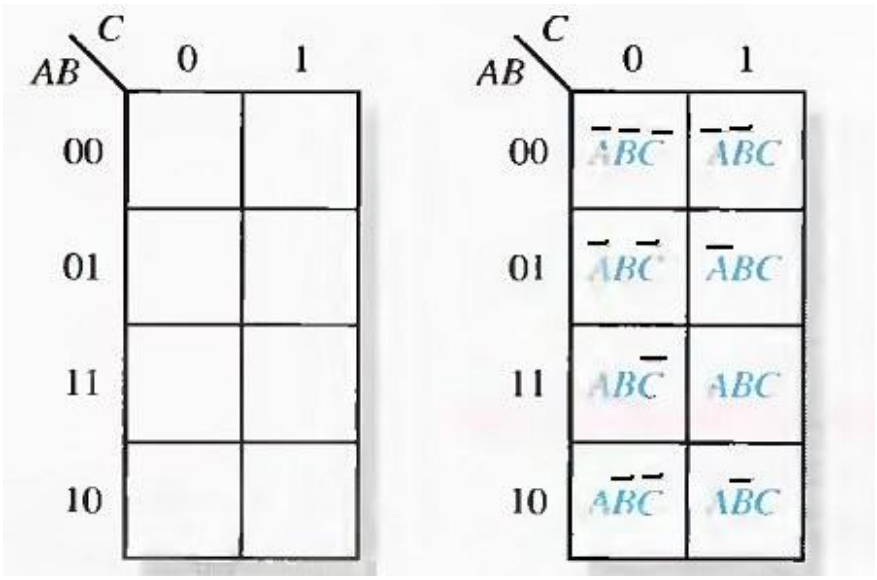
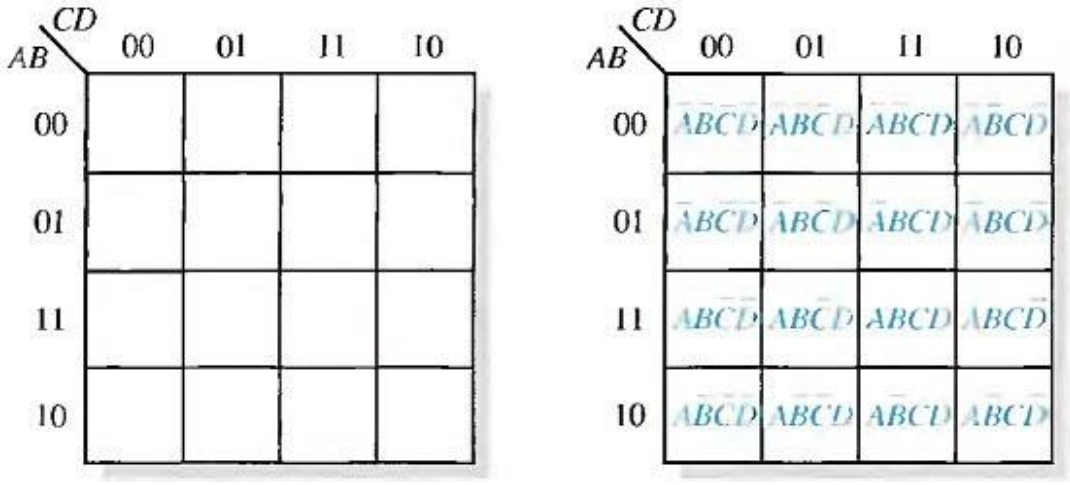


Fig.(5-1) A 3-variable Karnaugh map showing product terms.

<u>The 4-Variable Karnaugh Map</u>

The 4-variable Karnaugh map is an array of sixteen cells, as shown in Fig.(5-2)(a). Binary values of A and B are along the left side and the valuesof C and D are across the top. The value of a given cell is the binary valuesof A and B at the left in the same row combined with the binary values of C and D at the top in the same column. For example, the cell in the upper right corner has a binary value of 0010 and the cell in the lower right corner has a binary value of 1010. Fig.(5-2)(b) shows the standard product terms that arerepresented by each cell in the 4-variable Karnaugh map.



(a) (b)

Fig.(5-2) A 4-variable Karnaugh map.

Cell Adjacency

The cells in a Karnaugh map are arranged so that there is only a single-variable change between adjacent cells. Adjacency is defined by a single-variable change. In the 3-variable map the 010 cell is adjacent to the 000 cell, the 011 cell, and the 110 cell. The 010 cell is not adjacent to the 001 cell, the 111 cell, the 100 cell, or the 101 cell.

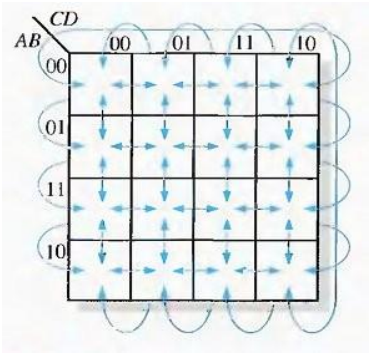


Fig.(5-3) Adjacent cells on a Karnaugh map are those that differ by only one variable. Arrows point between adjacent cells.

KARNAUGH MAP SOP MINIMIZATION

For an SOP expression in standard form, a 1 is placed on the Karnaugh map for each product term in the expression. Each 1 is placed in a cell corresponding to the value of a product term. For example, for the product term ABC, a 1 goes in the 10l cell on a 3-variable map.

Example

Map the following standard SOP expression on a Karnaugh map:

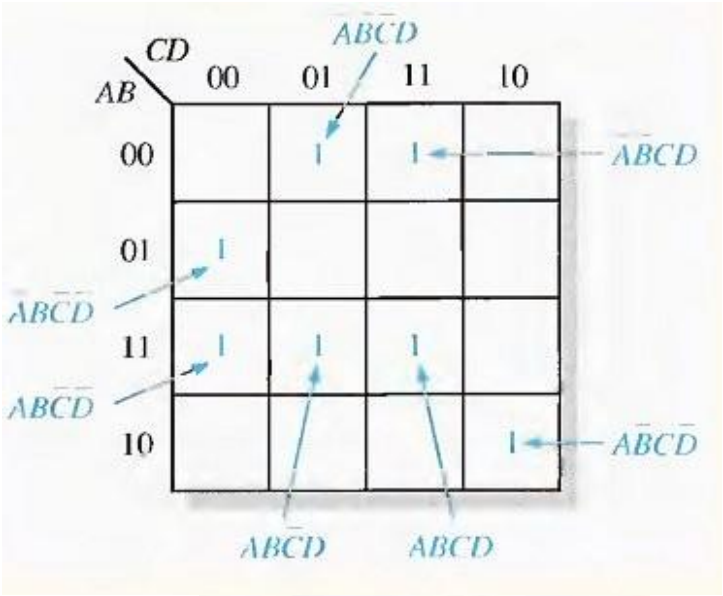
see Fig.(5-4).

Example

Map the following standard SOP expression on a Karnaugh map:

$$\overline{A}\,\overline{B}CD + \overline{A}B\overline{C}\,\overline{D} + AB\overline{C}D + ABCD + AB\overline{C}\,\overline{D} + \overline{A}\,\overline{B}\,\overline{C}D + A\overline{B}C\overline{D}$$

See Fig.(5-5).



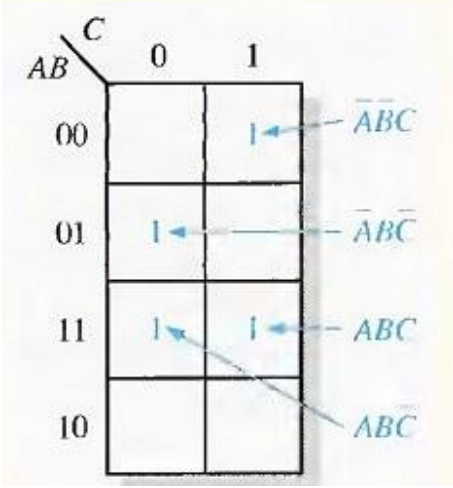


Fig.(5-4)

Fig.(5-5)

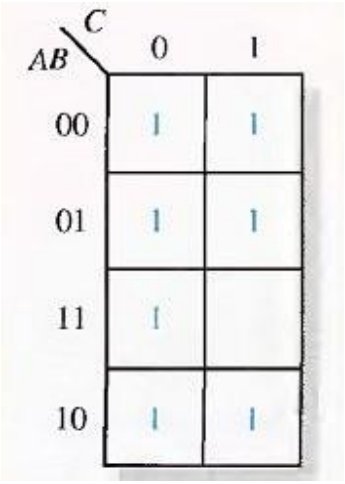
Example

Map the following SOP expression on a Karnaugh map: $\bar{A} + A\bar{B} + AB\bar{C}.$

Solution

The SOP expression is obviously not in standard form because each product term does not have three variables. The first term is missing two variables, the second term is missing one variable, and the third term is standard. First expand the terms numerically as follows:

$\overline{A}$	$+ A\overline{B}$	$+ AB\overline{C}$
000	100	110
001	101	
010		
011		



Example

Map the following SOP expression on a Karnaugh map:

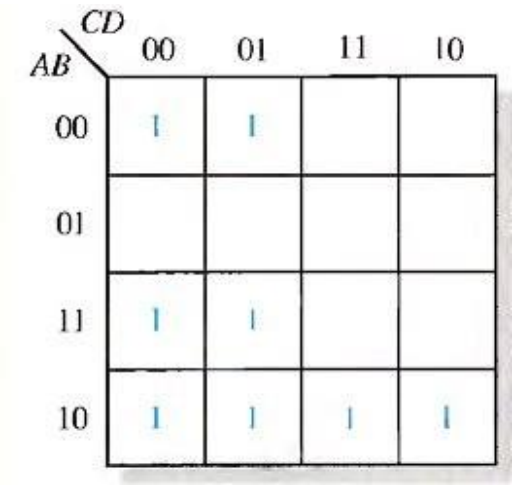
$$\overline{B}\,\overline{C} + A\overline{B} + AB\overline{C} + A\overline{B}C\overline{D} + \overline{A}\,\overline{B}\,\overline{C}D + A\overline{B}CD$$

Solution

The SOP expression is obviously not in standard form because each product term does not have four variables.

$\overline{B}\,\overline{C}$	$A\overline{B}$	$+ AB\overline{C}$	$+ A\overline{B}C\overline{D}$	$+ \overline{A}\,\overline{B}\,\overline{C}D$	$+ A\overline{B}CD$
0000	1000	1100	1010	0001	1011
0001	1001	1101			
1000	1010				
1001	1011				

Map each of the resulting binary values by placing a 1 in the appropriate cell of the 4- variable Karnaugh map.



Karnaugh Map Simplification of SOP Expressions

Grouping the 1s, you can group 1s on the Karnaugh map according to the following rules by enclosing those adjacent cells containing 1s. The goal is to maximize the size of the

groups and to minimize the number of groups.

- A group must contain either 1, 2, 4, 8, or 16 cells, which are all powers of two. In the case of a 3-variable map, 2^3 = 8 cells is the maximum group.
- Each cell in a group must be adjacent to one or more cells in that same group.
- Always include the largest possible number of 1s in a group in accordance with rule 1.
- Each 1 on the map must be included in at least one group. The 1s already in a group can be included in another group as long as the overlapping groups include noncommon 1s.

Example:

Group the 1s in each of the Karnaugh maps in Fig.(5-6).

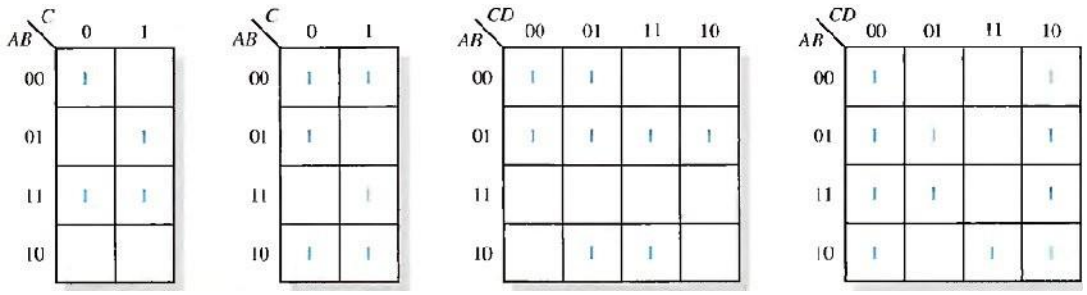


Fig.(5-6)

Solution:

The groupings are shown in Fig.(5-7). In some cases, there may be more than one way to group the 1s to form maximum groupings.

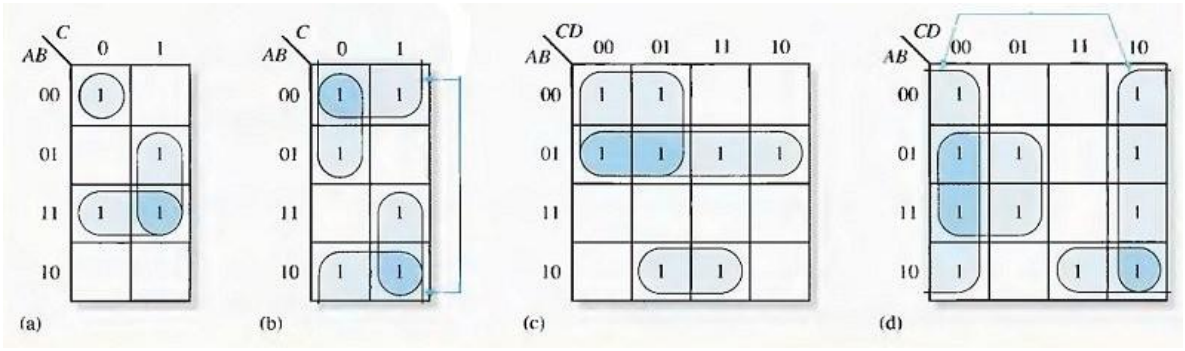


Fig.(5-7)

Determine the minimum product term for each group.

a. For a 3-variable map:

(1) A l-cell group yields a 3-variable product term

(2) A 2-cell group yields a 2-variable product term

(3) A 4-cell group yields a 1-variable term

(4) An 8-cell group yields a value of 1 for the expression

b. For a 4-variable map:

(1) A 1-cell group yields a 4-variable product term

(2) A 2-cell group yields a 3-variable product term

(3) A 4-cell group yields a 2-variable product term

(4) An 8-cell group yields a 1-variable term

(5) A 16-cell group yields a value of 1 for the expression

Example:

Determine the product terms for each of the Karnaugh maps in Fig.(5-7) and write the resulting minimum SOP expression.

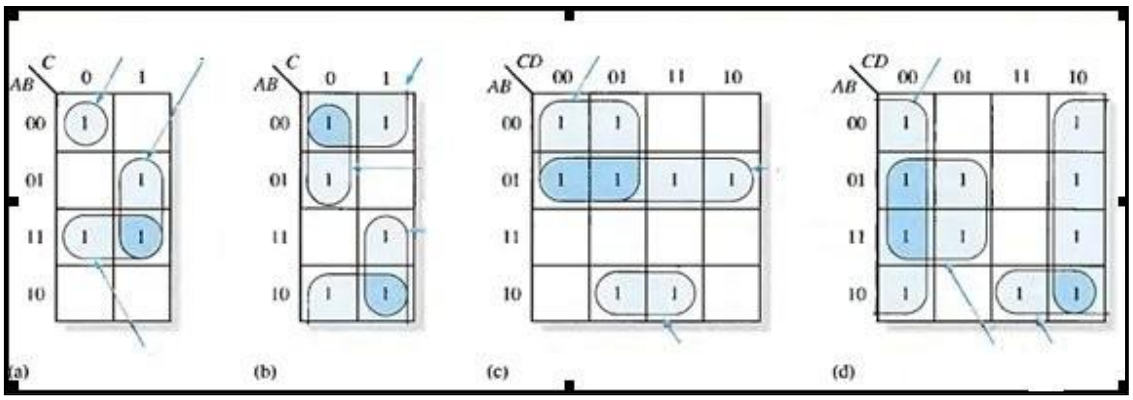


Fig.(5-8)

Solution:

The resulting minimum product term for each group is shown in Fig.(5-8).

The minimum SOP expressions for each of the Karnaugh maps in the figure are:

(a) $AB+BC+\overline{ABC}$

(b) $\overline{B} + A\,C + \overline{AC}$

(C) $AB + \overline{AC} + \overline{ABD}$

(d) $\overline{D} + \overline{ABC} + \overline{BC}$

Example: Use a Karnaugh map to minimize the following standard SOP expression:

$$\overline{A}\overline{B}\overline{C} + \overline{A}B\overline{C} + \overline{A}BC + A\overline{B}\overline{C} + A\overline{B}C$$

Example: Use a Karnaugh map to minimize the following SOP expression:

$$\overline{B}\,\overline{C}\,\overline{D} + \overline{A}\overline{B}\overline{C}\,\overline{D} + A\overline{B}\overline{C}\,\overline{D} + \overline{A}\,\overline{B}CD + A\overline{B}CD + \overline{A}\,\overline{B}C\overline{D} + \overline{A}BC\overline{D} + ABC\overline{D} + A\overline{B}C\overline{D}$$

"Don't Care" Conditions

Sometimes a situation arises in which some input variable combinations are not allowed. For example, recall that in the BCD code there are six invalid combinations: 1010, 1011, 1100, 1101, 1110, and 1111. Since these unallowed states will never occur in an application involving the BCD code, they can be treated as "don't care" terms with respect to their effect on the output. That is, for these "don't care" terms either a 1 or a 0 may be assigned to the output: it really does not matter since they will never occur.

The "don't care" terms can be used to advantage on the Karnaugh map. Fig.(5-9) shows that for each "don't care" term, an X is placed in the cell. When grouping the 1 s, the Xs can be treated as 1s to make a larger grouping or as 0s if they cannot be used to advantage. The larger a group, the simpler the resulting term will be.

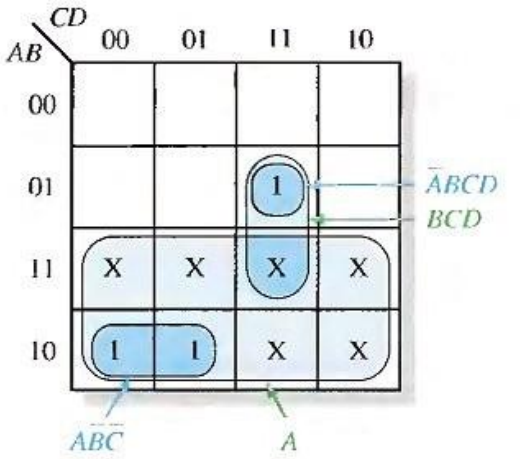
The truth table in Fig.(5-9)(a) describes a logic function that has a 1 output only when the BCD code for 7,8, or 9 is present on the inputs. If the "don't cares" are used as 1s, the resulting expression for the function is A + BCD, as indicated in part (b). If the "don't cares" are not used as 1s, the resulting

expression is ABC + ABCD: so you can see the advantage of using "don't care" terms to get the simplest expression.

Inputs A B C D	Output Y
0 0 0 0	0
0 0 0 1	0
0 0 1 0	0
0 0 1 1	0
0 1 0 0	0
0 1 0 1	0
0 1 1 0	0
0 1 1 1	1
1 0 0 0	1
1 0 0 1	1
1 0 1 0	X
1 0 1 1	X
1 1 0 0	X
1 1 0 1	X
1 1 1 0	X
1 1 1 1	X

(a) Truth table

Don't cares



(b) Without "don't cares" $Y = A\bar{B}\bar{C} + \bar{A}BCD$
With "don't cares" $Y = A + BCD$

Fig.(5-9)

KARNAUGH MAP POS MINIMIZATION

In this section, we will focus on POS expressions. The approaches are much the same except that with POS expressions, 0s representing the standard sum terms are placed on the Karnaugh map instead of 1s.

For a POS expression in standard form, a 0 is placed on the Karnaugh map for each sum term in the expression. Each 0 is placed in a cell corresponding to the value of a sum term. For example, for the sum term $A + B + \overline{C}$, a 0goes in the 0 1 0 cell on a 3-variable map.

When a POS expression is completely mapped, there will be a number of 0s on the Karnaugh map equal to the number of sum terms in the standard POS expression. The cells that do not have a 0 are the cells for which the expression is 1. Usually, when working with POS expressions, the 1s are left off. The following steps and the illustration in Fig.(5-10) show the mapping process.

Step 1. Determine the binary value of each sum term in the standard POS expression. This is the binary value that makes the term equal to 0.

Step 2. As each sum term is evaluated, place a 0 on the Karnaugh map in the corresponding cell.

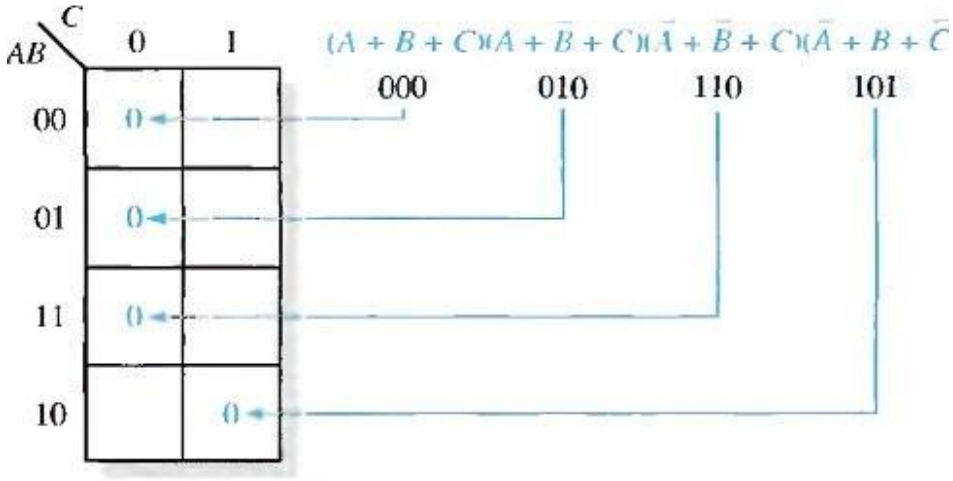


Fig.(5-10)

Example of mapping a standard POS expression.

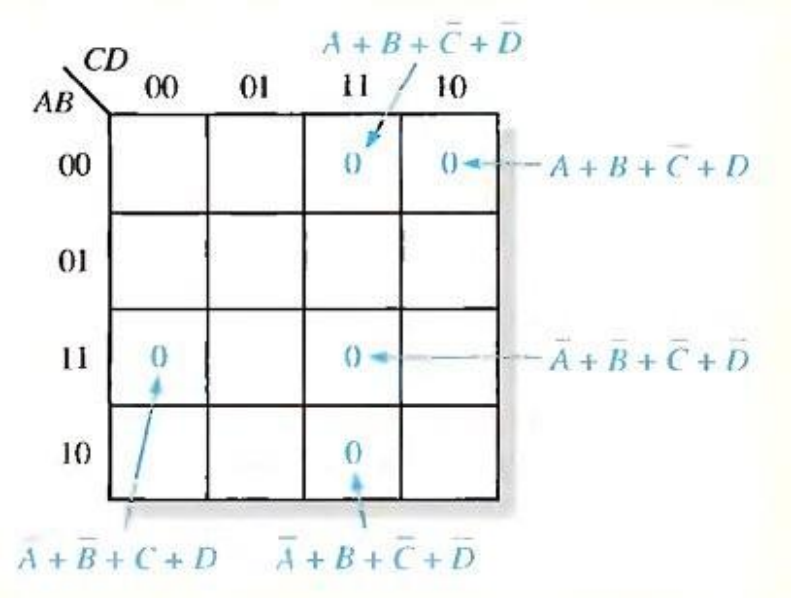
Example:

Map the following standard POS expression on a Karnaugh map:

$$(\bar{A} + \bar{B} + C + D)(\bar{A} + B + \bar{C} + \bar{D})(A + B + \bar{C} + D)(\bar{A} + \bar{B} + \bar{C} + \bar{D})(A + B + \bar{C} + \bar{D})$$

Solution:

$$(\bar{A} + \bar{B} + C + D)(\bar{A} + B + \bar{C} + \bar{D})(A + B + \bar{C} + D)(\bar{A} + \bar{B} + \bar{C} + \bar{D})(A + B + \bar{C} + \bar{D})$$
$$1100 \qquad 1011 \qquad 0010 \qquad 1111 \qquad 0011$$



Karnaugh Map Simplification of POS Expressions

The process for minimizing a POS expression is basically the same as for an SOP expression except that you group 0s to produce minimum sum terms instead of grouping 1s to produce minimum product terms. The rules for grouping the 0s are the same as those for grouping the 1s that you learned before.

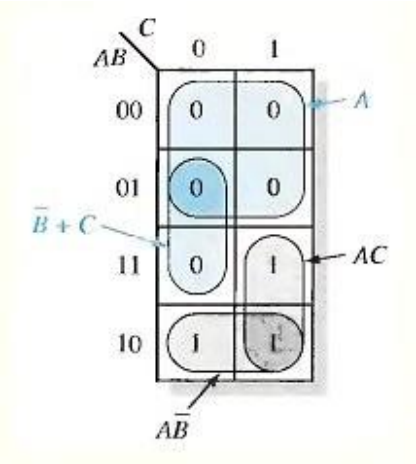
Example:

Use a Karnaugh map to minimize the following standard POS expression:

Also, derive the equivalent SOP expression.

$$(A + B + C)(A + B + \overline{C})(A + \overline{B} + C)(A + \overline{B} + \overline{C})(\overline{A} + \overline{B} + C)$$

Solution:

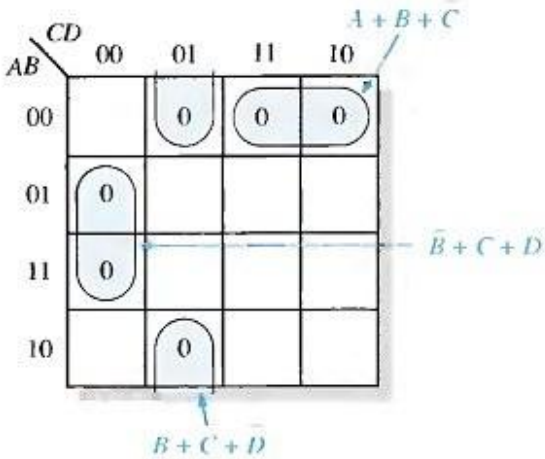


Example: Use a Karnaugh map to minimize the following POS expression:

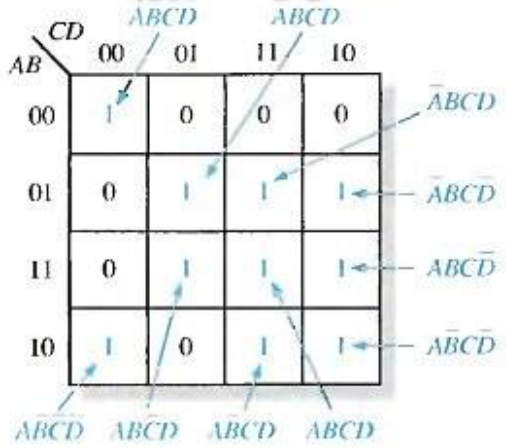
$$(B + C + D)(A + B + \overline{C} + D)(\overline{A} + B + C + \overline{D})(A + \overline{B} + C + D)(\overline{A} + \overline{B} + C + D)$$

Example: Using a Karnaugh map, convert the following standard POS expression into a minimum POS expression, a standard SOP expression, and a minimum SOP expression.

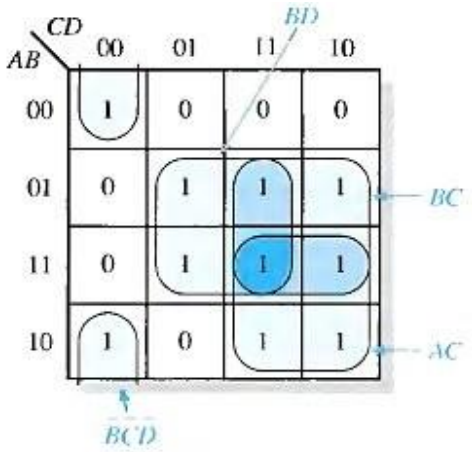
$$(\overline{A} + \overline{B} + C + D)(A + \overline{B} + C + D)(A + B + C + \overline{D})$$
$$(A + B + \overline{C} + \overline{D})(\overline{A} + B + C + \overline{D})(A + B + \overline{C} + D)$$



(a) Minimum POS: $(A + B + C)(\overline{B} + \overline{C} + D)(B + C + \overline{D})$



(b) Standard SOP:
$\overline{A}\overline{B}\overline{C}\overline{D} + \overline{A}\overline{B}C\overline{D} + \overline{A}\overline{B}CD + \overline{A}B\overline{C}\overline{D} + AB\overline{C}\overline{D} + A\overline{B}\overline{C}\overline{D} +$
$A\overline{B}\overline{C}\overline{D} + A\overline{B}C\overline{D} + A\overline{B}CD + ABCD$



(c) Minimum SOP: $AC + BC + BD + \bar{B}\bar{C}\bar{D}$

FIVE-VARIABLE KARNAUGH MAPS

Boolean functions with five variables can be simplified using a 32-cell Karnaugh map. Actually, two 4-variable maps (16 cells each) are used to construct a 5-variable map. You already know the cell adjacencies within each of the 4- variable maps and how to form groups of cells containing 1s to simplify an SOP expression. All you need to learn for five variables is the cell adjacencies between the two 4-variable maps and how to group those adjacent 1s.

A Karnaugh map for five variables (ABCDE) can be constructed using two 4-variable maps with which you are already familiar. Each map contains 16 cells with all combinations of variables B, C, D, and E. One map is for A = 0 and the other is for A = 1, as shown in Fig.(5-11).

Cell Adjacencies

You already know how to determine adjacent cells within the 4-variable map. The best way to visualize cell adjacencies between the two 16-cel1 maps is to imagine that the A = 0 map is placed on top of the A = 1 map. Each cell in the A = 0 map is adjacent to the cell directly below it in the A =1 map, see Fig.(5-12).

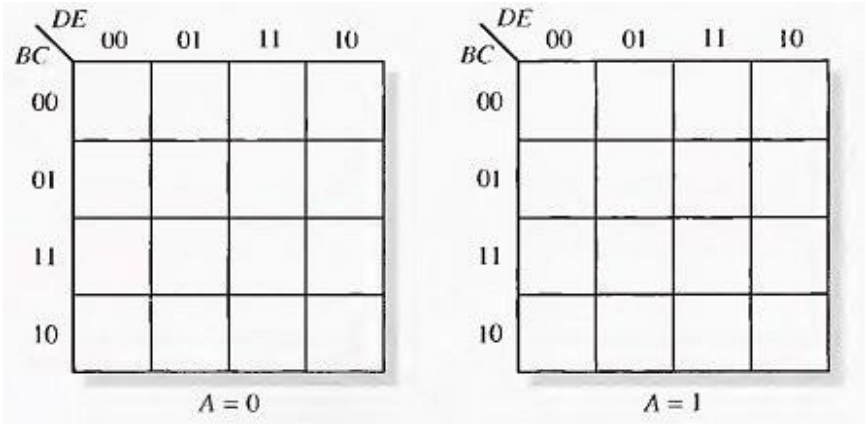
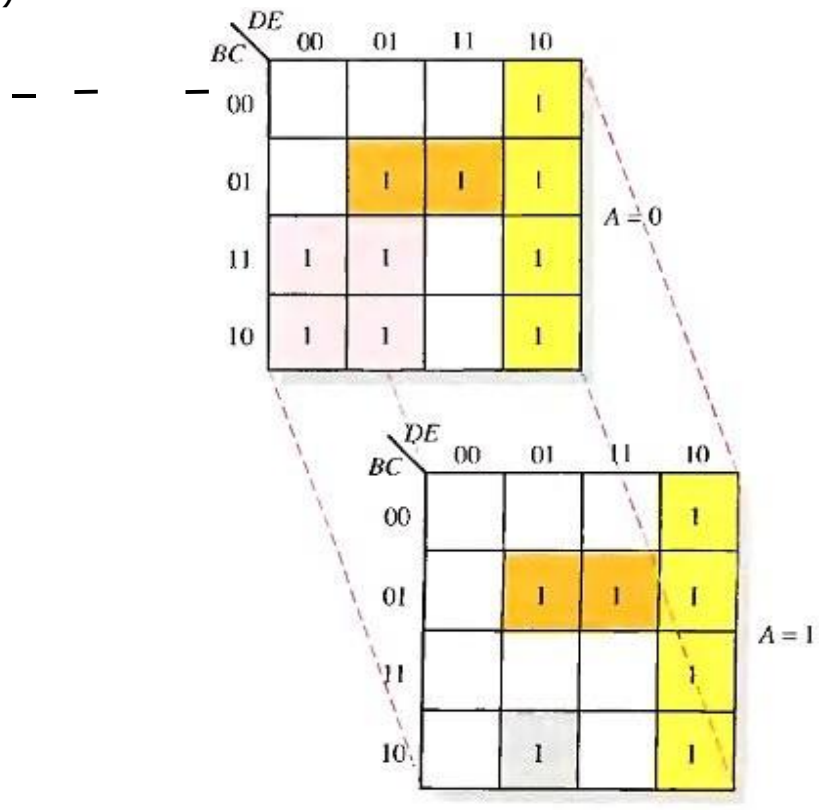


Fig.(5-11)

Fig.(5-12)



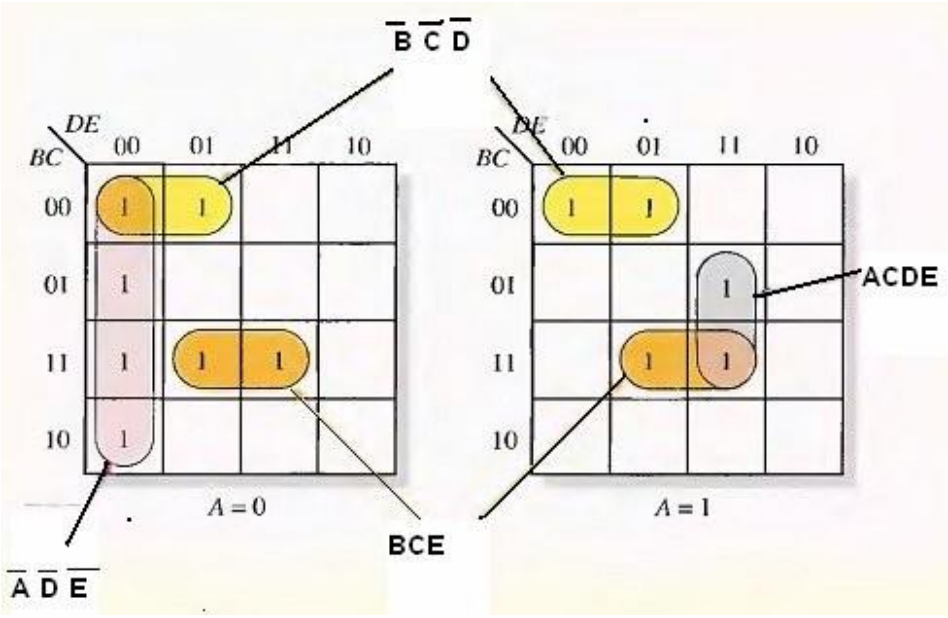
The simplified SOP expression yieldsx

= DE + BCE + ABD + BC DE

xample:

Use a Karnaugh map to minimize the following standard SOP 5-variable expression:

$$X = \bar{A}\bar{B}\bar{C}\bar{D}\bar{E} + \bar{A}\bar{B}\bar{C}D\bar{E} + \bar{A}B\bar{C}\bar{D}\bar{E} + \bar{A}B\bar{C}D\bar{E} + \bar{A}B\bar{C}\bar{D}E + \bar{A}B\bar{C}DE$$
$$+ \bar{A}BCDE + A\bar{B}\bar{C}\bar{D}\bar{E} + A\bar{B}\bar{C}D\bar{E} + A\bar{B}C\bar{D}E + ABC\bar{D}E + ABCDE + A\bar{B}CDE$$



$$X = \bar{A}D\bar{E} + \bar{B}\bar{C}\bar{D} + BCE + ACDE$$

Half Adder

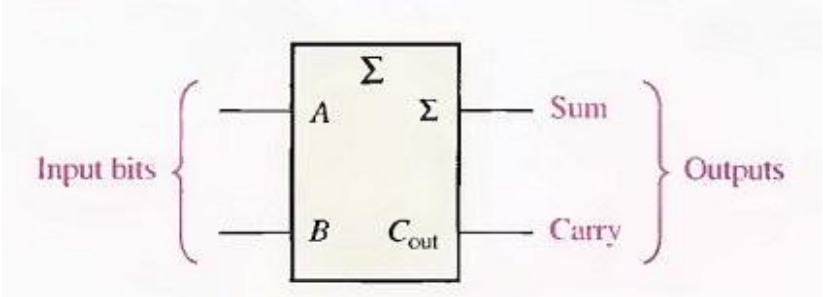


Fig.Logic symbol for a half-adder.

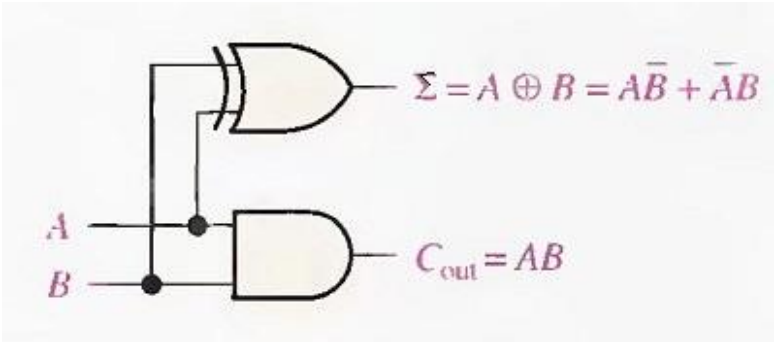


Fig. Half-adder logic diagram.Table

A	B	C_{out}	Σ
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

The Full-Adder

The second category of adder is the full-adder. The full-adder accepts two input bits and an input carry and generates a sum output and an output carry.

The basic difference between a full-adder and a half-adder is that the full-adder accepts an input carry. A logic symbol for a full-adder is shown in Fig., andthe truth table in Table shows the operation of a full-adder.

Table

A	B	C_{in}	C_{out}	Σ
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

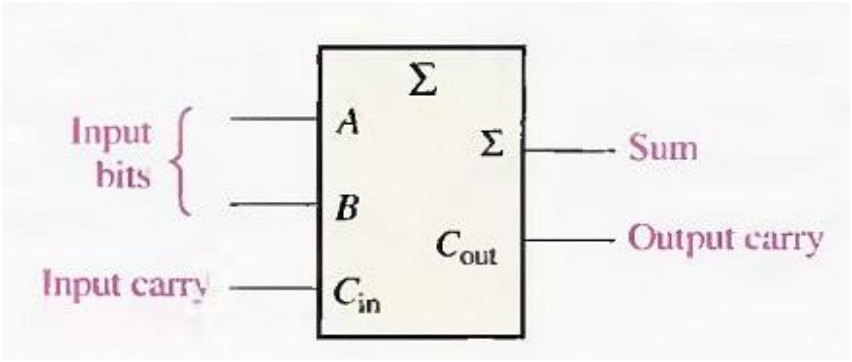


Fig. Logic symbol for a full-adder.

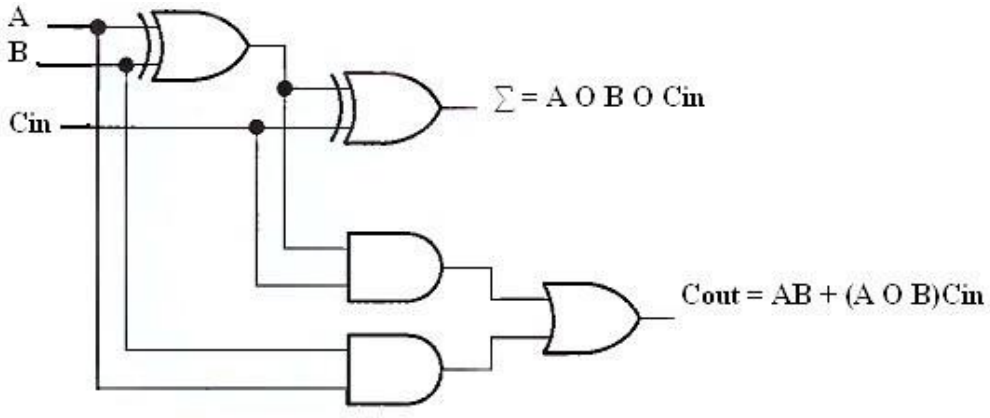


Fig. Complete logic circuit for a full-adder.

$\sum = A \oplus B \oplus C_{in}$

$C_{out} = AB + (A \oplus B)C_{in}$

Notice in Fig. there are two half-adders, connected as shown in the blockdiagram of Fig., with their output carries ORed.

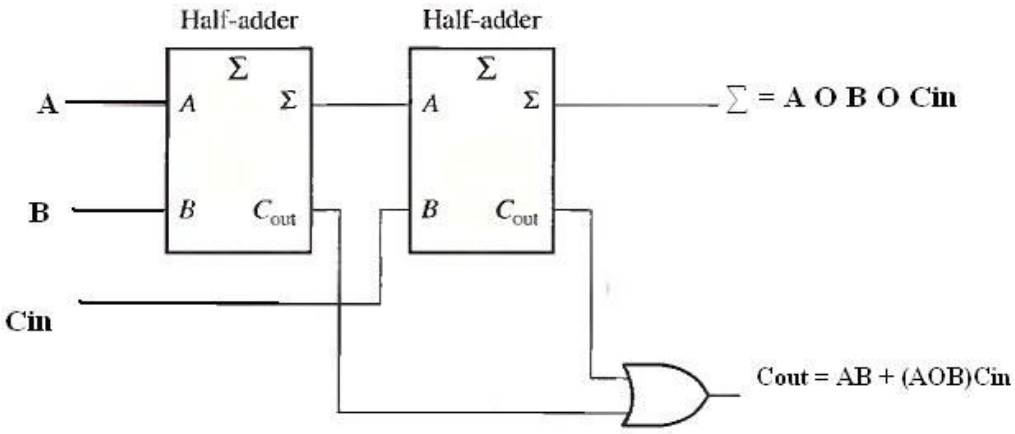


Fig. Arrangement of two half-adders to form a full-adder.

Example: For each of the three full-adders in Fig., determine the outputs forthe inputs shown.

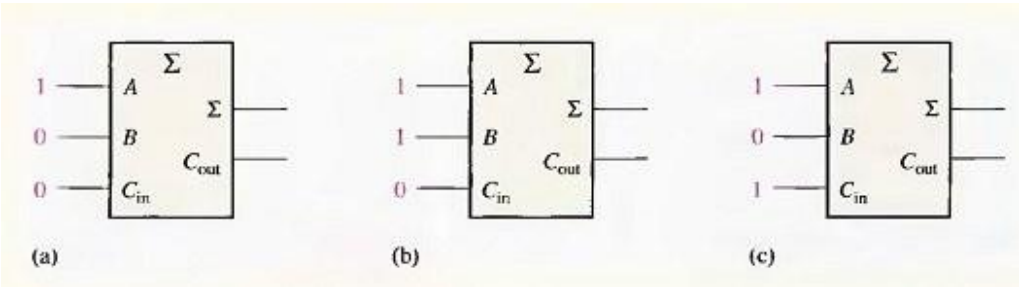
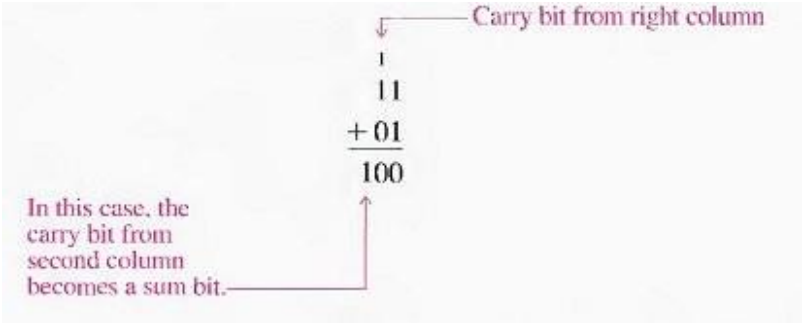


Fig.

PARALLEL BINARY ADDERS

As you saw in Section , a single full-adder is capable of adding two 1-bit numbers and an input carry. To add binary numbers with more than one bit, you must use additional full-adders. When one binary number is added to another, each column generates a sum bit and a 1 or 0 carry bit to the next column to the left, as illustrated here with 2-bit numbers.



To add two binary numbers, a full-adder is required for each bit in the numbers. So for 2-bit numbers, two adders are needed; for 4-bit numbers, four adders are used; and so on. The carry output of each adder is connected to the carry input of thenext higher-order adder, as shown in Fig. for a 2-bit adder. Notice that either a half-adder can be used for the least significant position or the carry input of a full-adder can be made 0 (grounded) because there is no carry input to the least significant bit position.

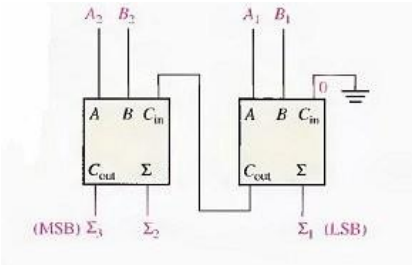


Fig.Block diagram of a basic 2-bit parallel adder using two full-adders.

Example: Determine the sum generated by the 3-bit parallel adder in Fig.(7-8) and show the intermediate carries when the binary numbers 101 and 011 are being added.

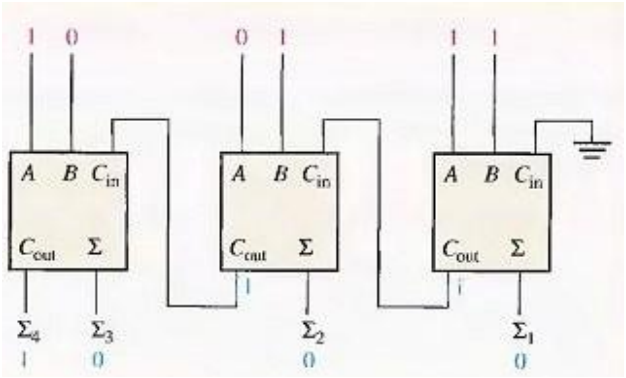


Fig.

Four-Bit Parallel Adders

A group of four bits is called a nibble. A basic 4-bit parallel adder is implemented with four full-adder stages as shown in Fig.(7-9). Again, the LSBs (A1 and B1) in each number being added go into the right-most full-adder: the higher-order bitsare applied as shown to the successively higher-order added, with the MSBs (Aand B) in each number being applied to the left-most full-adder. The Carry outputof each adder is connected to the carry input of the next higher-order adder as indicated. These are called internal carries.

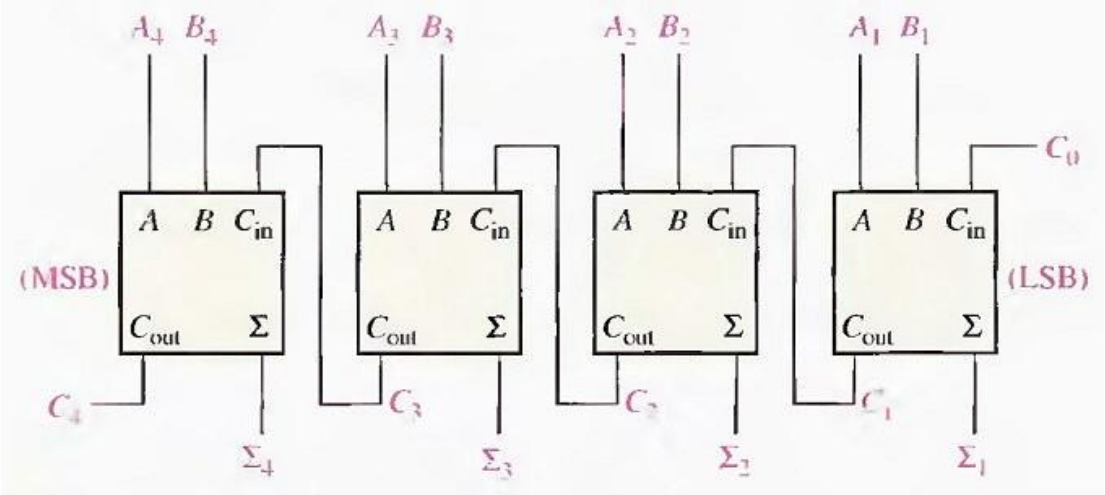


Fig.

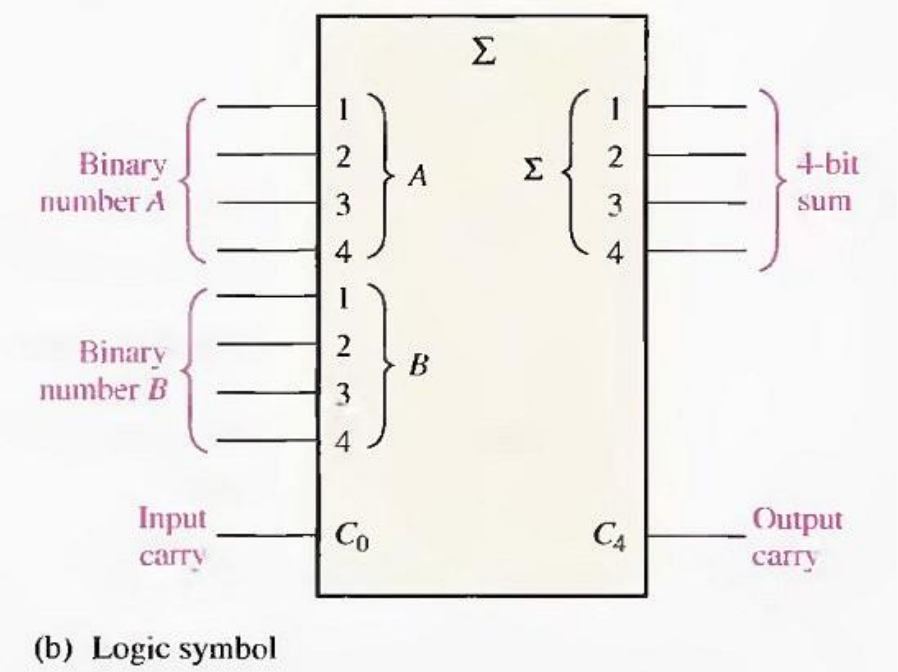


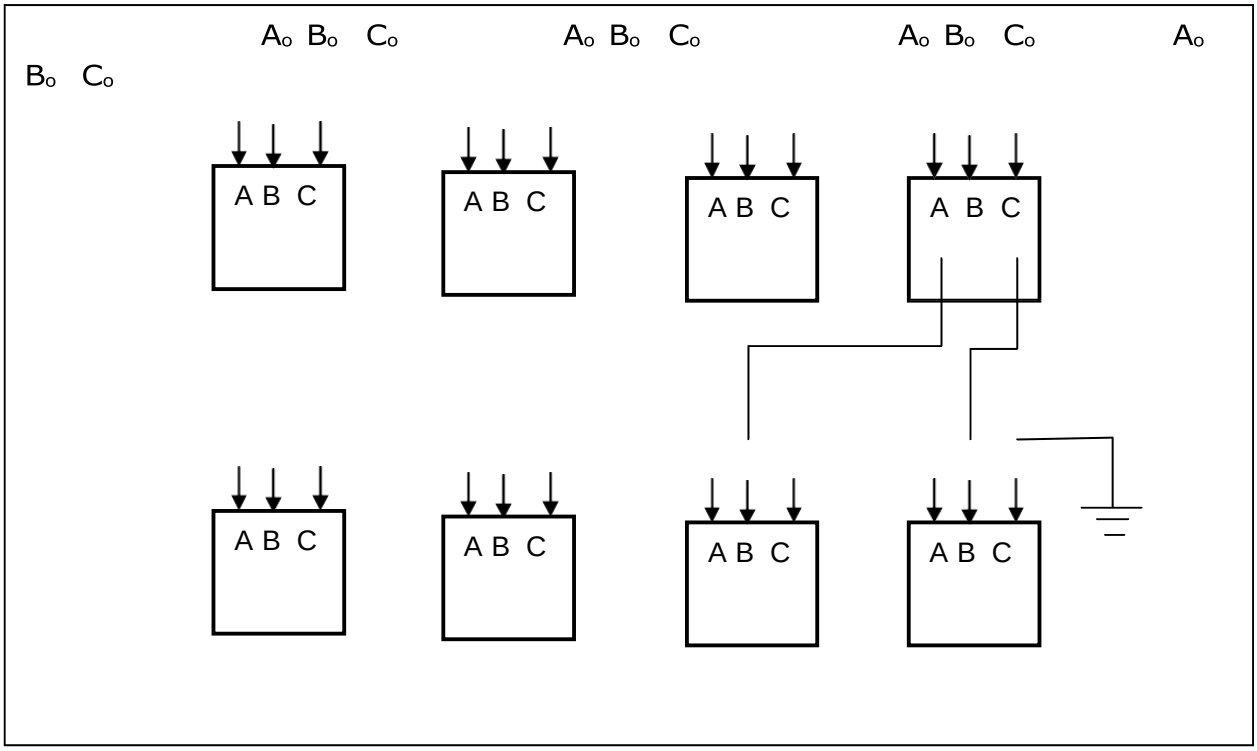
Fig. A 4-bit parallel adder.

Carry Save Adder (CSA)

A method for adding three or more numbers at a time is called carry-save addition.This process is illustrated in Example below:

Example:

	00011	A
	00001	B
+	**01001**	C
	01011	sum, excluding carries
+	**0001**	carries shifted left one place
	01101	final sum



COMPARATORS

The basic function of a comparator is to compare the magnitudes of two binary quantities to determine the relationship of those quantities. In its simplest form, a comparator circuit determines whether two numbers are equal.

Equality

The exclusive-OR gate can be used as a basic comparator because its output is a 1if the two input bits are not equal and a 0 if the input bits are equal. Fig.(7-11) shows the exclusive-OR gate as a 2-bit comparator.

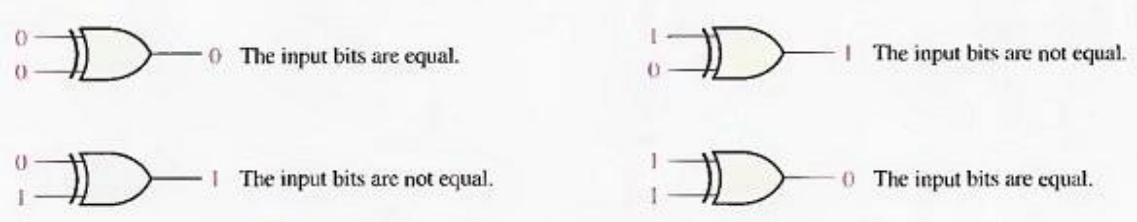


Fig. Basic comparator
operation.

In order to compare binary numbers containing two bits each, an additional exclusive- OR gate is necessary. The two least significant bits (LSBs) of the two numbers are compared by gate G1. and the two most significant bits (MSBs) are compared by gate G2, as shown in Fig. If the two numbers are equal, their corresponding bits are the same, and the output of each exclusive-OR gate is a 0. If the corresponding sets of bits are not equal,a 1 occurs on that exclusive-OR gate output.

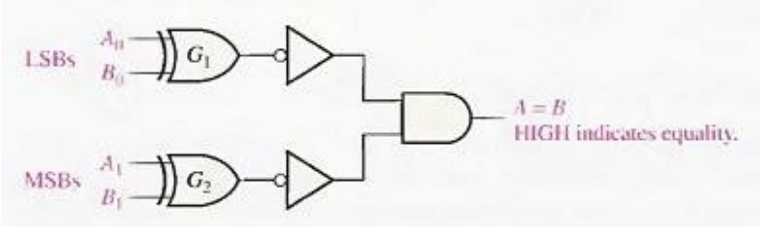


Fig. Logic diagram for equality comparison of two 2-bit numbers.

Inequality

In addition to the equality output, many IC comparators provide additional outputs that indicate which of the two binary numbers being compared is the larger. That is, there is an output that indicates when number A is greater than number B (A >B) and an output that indicates when number A is less than number B (A < B), as shown in the logic symbol for a 4-bit comparator in Fig.

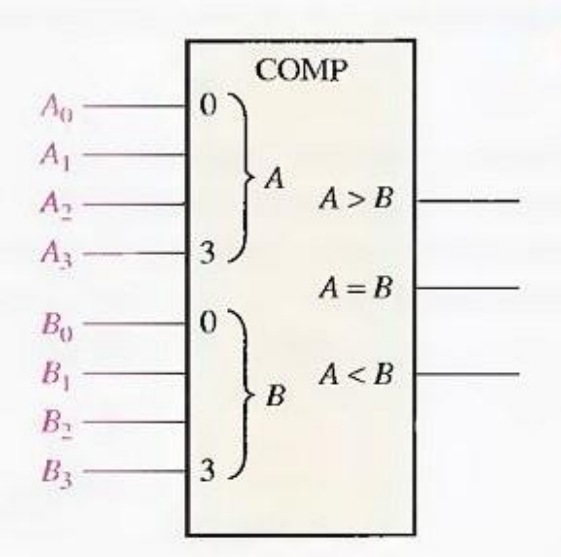


Fig.Lo gic symbol for a 4-bit comparator with inequality indication.

To determine an inequality of binary numbers A and B, you first examine thehighest-order bit in each number. The following conditions are possible:

1. If A3 = 1 and B3 = 0, number A is greater than number B.
2. If A3 = 0 and B3 = 1 number A is less than number B.
3. If A3 = B3, then you must examine the next lower bit position for an inequality.